CCSTA53N30

N-Type, ThinPak™

Preliminary Data Sheet

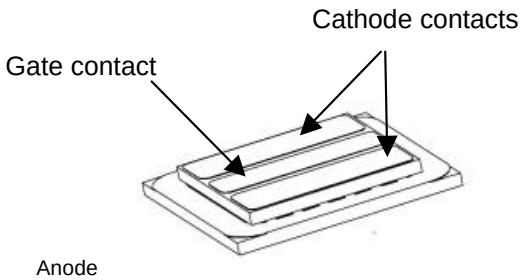
Description

This current controlled Solidtron (CCS) discharge switch is an n type Thyristor in a high performance ThinPak™ package. The device gate is similar to that found on a traditional GTO Thyristor.

The CCS features the high peak current capability and low On-state voltage drop common to SCR thyristors combined with high di/dt capability. This semiconductor is intended to be a solid state replcement for spark or gas type devices commonly used in pulse power applications.

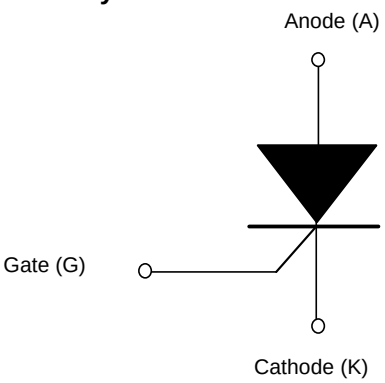
The ThinPak™ Package is a perforated, metalized ceramic substrate attached to the silicon using 302°C solder. All exterior metal surfaces are tinned with 63pb/37sn solder providing the user with a circuit ready part. It's small size and low profile make it extremely attractive for high di/dt applications where stray series inductance must be kept to a minimum.

Package



ThinPak™

Schematic Symbol



Features

- 3000V Peak Off-State Voltage
- 5 kA Repetitive Ipk Capability
- 25 KA/uS di/dt Capability
- Low On-State Voltage
- Low trigger current
- Low Inductance Package

Absolute Maximum Ratings

	SYMBOL	VALUE	UNITS
Peak Off-State Voltage	V_{DRM}	3	kV
Peak Reverse Voltage	V_{RRM}	-5	V
Off-State Rate of Change of Voltage Immunity*	dv/dt	1	kV/uSec
Continuous Anode Current at Tj = 125 °C	I_{A110}	50	A
Repetitive Peak Anode Current (Pulse Width=10uSec)	I_{ASM}	5.0	kA
Nonrepetitive Peak Anode Current (Pulse Width=10uSec)	I_{ASM}	8	kA
Rate of Change of Current	dI/dt	25	kA/uSec
Peak Gate Current (1 uS)	IGpk	50	A
Max. Reverse Gate-Cathode Voltage	V_{GR}	-9	V
Maximum Junction Temperature	T_{JM}	125	°C
Maximum Soldering Temperature (Installation)		260	°C

This **SILICON POWER** product is protected by one or more of the following U.S. Patents:

5,521,436	5,446,316	5,105,536	5,209,390	4,958,211	5,206,186	4,857,983	5,082,795	4,644,637
5,585,310	5,557,656	5,777,346	5,139,972	5,111,268	5,757,036	4,888,627	4,980,741	4,374,389
5,248,901	5,564,226	5,446,316	5,103,290	5,260,590	5,777,346	4,912,541	4,941,026	4,750,666
5,366,932	5,517,058	5,577,656	5,028,987	5,350,935	5,995,349	5,424,563	4,927,772	4,429,011
5,497,013	4,814,283	5,473,193	5,304,847	5,640,300	4,801,985	5,399,892	4,739,387	5,293,070
5,532,635	5,135,890	5,166,773	5,569,957	5,184,206	4,476,671	5,468,668	4,648,174	

Preliminary Data Sheet - Product Status : First Production : This data sheet contains preliminary data . Supplementary data will be published at a later date. Silicon Power reserves the right to make changes at any time without notice.

* Requires a 10 ohm gate to cathode shorting resistor.

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Performance Characteristics T_J=25°C unless otherwise specified

Parameters	Symbol	Test Conditions		Measurements Min.	Typ.	Max.	Units
Anode to Cathode Breakdown Voltage	V_{DR}	V_{GK}=0, I_A=1mA		3			kV
Anode-Cathode Off-State Current	I_D	V_{GK}=0V, V_{AK}=3000V	T_J=25°C		<30	100	uA
			T_J=125°C		80	250	uA
Turn-On Threshold Current	$V_{GK(TH)}$	V_{AK}=V_{GK}, I_{AK}=1mA , see Note 1			5		mA
Gate-Cathode Leakage Current	$I_{GK(lkg)}$	V_{GK}=0V, see Note 1				20	uA
Anode-Cathode On-State Voltage	V_T	I_T=400A	T_J=25°C		3.8		V
		Ig = 500 mA	T_J=125°C		4.9		V
Turn-on Delay Time	$t_{D(ON)}$	6 uF Capacitor discharge			150		ns
Pk Rate of Change of Current (measured)	dI/dt	V_{AK} = 2.1 kV	T_J=25°C		4		kA/us
Peak Anode Current	I_P	R_{gk} = 10 ohms			4		kA
		Gate di/dt =100 A/us					

Notes:

1. Measurements made with a 10 Ohm shorting resistor connected between the gate and cathode.
2. Case Exterior Assummed to be 0.002" of 63sn/37pb solder applied directly to cathode bond area of thinPak.

Typical Performance Curves (unless otherwise specified)

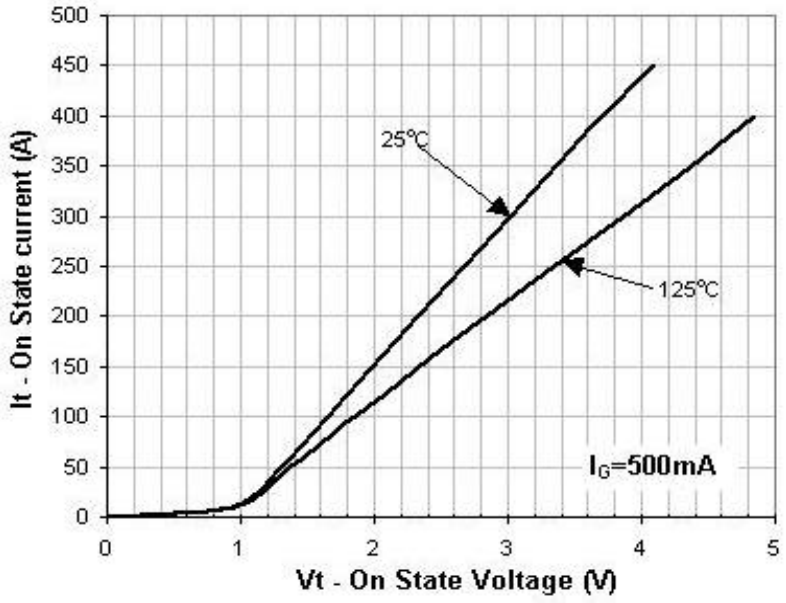


Figure 1.

Measured Low current On-State Characteristics.

Typical Performance Curves (Continued)

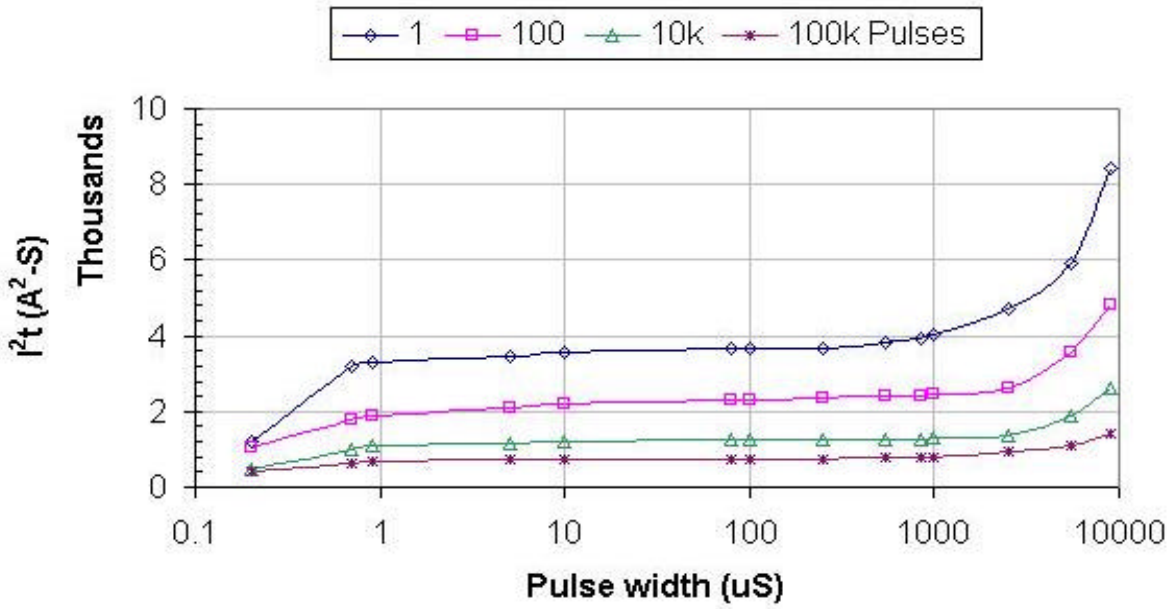
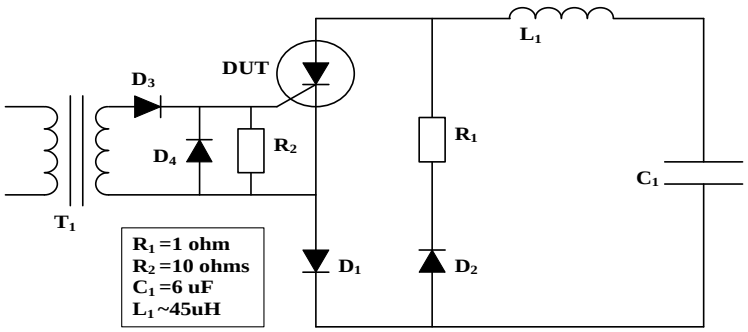
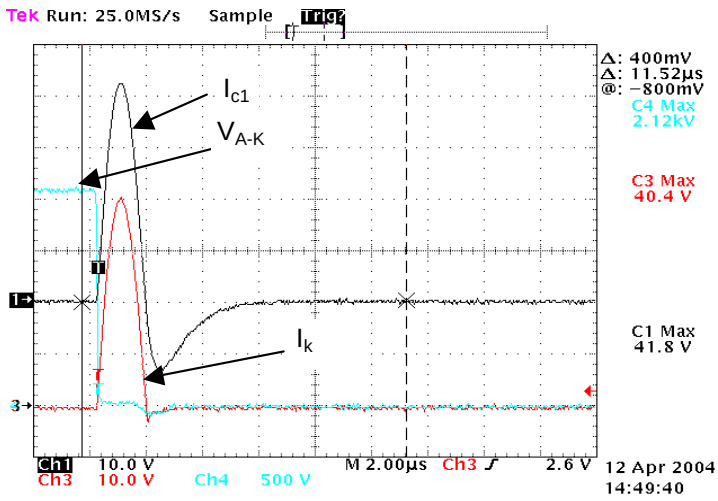


Figure 3. Predicted I^2t data for various number of discharge cycles. Pulses are assumed rectangular. The device junction temperature T_J is assumed to be at 25°C before each discharge event.

Test Circuit





- $L_{SERIES(TOTAL)}$ can be caculated using equation 1 / (f 2π)²C where f = frequency of I_K when using CCSTA53N30 for circuit set up and calibration.

- The waveform shown is representative of one produced using the test circuit shown where the DUT is the CCSTA53N30 Solidtron. The C1 capacitor voltage in this example was at 2.1kV. I_k peaked at 4kA at 1us and the peak gate current Ig is 1A.

Figure 4. Typical test circuit and waveforms.

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Application Notes

1. The CCSTA53N30 uses an undersized ceramic "lid" which exposes the sensitive junction termination edge (JTE) of the device. The user is required to encapsulate the device in an encapsulant prior to applying high voltage. This prevents debris and contaminants from compromising the JTE.

2. Use of a seperate gate return path instead of the cathode power contact is recomended to minimize the effects of rapidly changing Anode-Cathode currents.

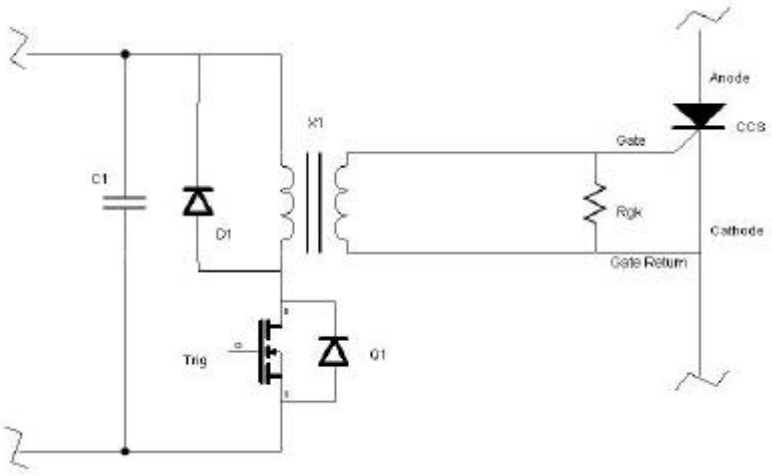


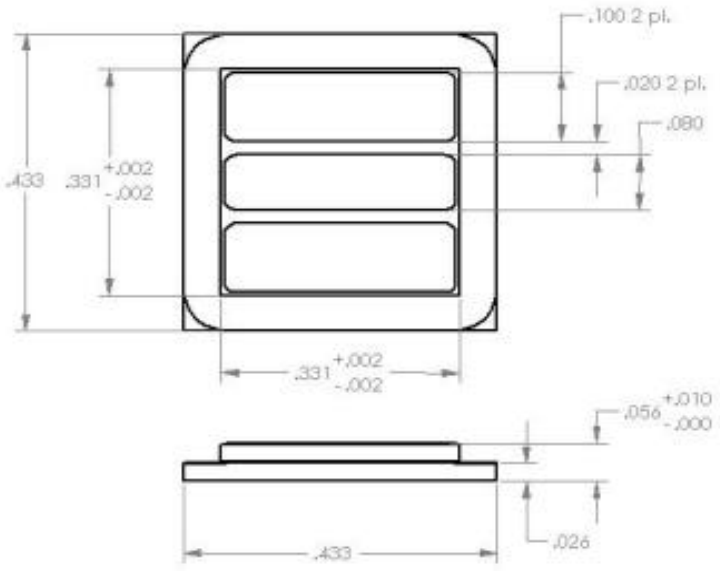
Figure 5. A suggested gate drive circuit.

3. For applications that require high voltage blocking for an extended period of time at high temperature (>85°C), it is recomended that the device V_{DR} be derated to 2kV.

4. Shorting resistor R_{GK} is application specific. It can control the gate drive requirements and some device properties. However, R_{GK} = 10 Ohms satisfies most application requirements.

Package Dimensions

(All units in Inches)



Packaging and Handling

1. All metal surfaces are tinned using 63pb/37sn solder.

2. Installation reflow temperature should not exceed 260°C or internal package degradation may result.

3. Package may be cooled from either top or bottom.

4. Proper handling procedures must be observed to prevent electrostatic discharge which may result in permanent damage to the gate of the device.