

010519

# Am9342-Am54/74182

## Look-Ahead Carry Generator

### Distinctive Characteristics:

- Provides look-ahead carries across a group of four ALU's
- Capability of multi-level look-ahead for high-speed arithmetic operation over large word lengths
- Typical carry propagation delay of 13 ns
- 100% reliability assurance testing in compliance with MIL STD 883.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Available in highly reliable molded epoxy, hermetic dual-in-line or Hermetic flat package.

### FUNCTIONAL DESCRIPTION

The Am54/74182 is a high-speed look-ahead carry generator which accepts up to four pairs of active LOW carry propagate and carry generate signals and an active HIGH carry input and provides anticipated active HIGH carries across four groups of binary adders. The device also has active LOW carry propagate and carry generate outputs which may be used for further levels of look-ahead.

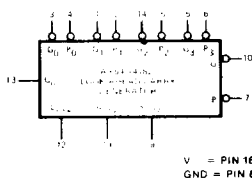
The Am54/74182 is generally used with the Am54/74181 arithmetic logic unit to provide look-ahead over word lengths of more than four bits.

The look-ahead carry generator can be used with binary ALUs in an active LOW or active HIGH input operand mode by reinterpreting the carry functions. The connections to and from the ALU to the look-ahead carry generator are identical in both cases.

The logic equations provided at the outputs are:

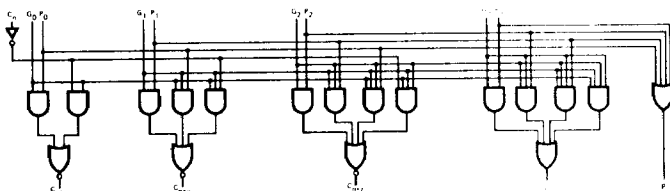
$$\begin{aligned} C_n + x &= G_0 + P_0 C_0 \\ C_n + y &= G_1 + P_1 G_0 + P_1 P_0 C_0 \\ C_n + z &= G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0 \\ G &= G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 \\ P &= P_3 P_2 P_1 P_0 \end{aligned}$$

### LOGIC SYMBOL



V<sub>CC</sub> = PIN 16  
GND = PIN 8

### LOGIC DIAGRAM

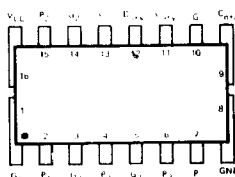


### Am54/74182 Am9342 ORDERING INFORMATION

Package Type	Temperature Range	Am54/74182 Order Number	9342 Order Number
Molded DIP	0°C to +75°C	SN74182N	Am9342C
Hermetic DIP	0°C to +75°C	SN74182J	U6N934259X
Hermetic DIP	-55°C to +125°C	SN54182J	U7B934251X
Hermetic Flat Pak	0°C to +125°C	SN54182S	U4L 934251X
Dice	0°C to +125°C	SN54182D	UXX9342XXD

Note: This package will contain units which meet both 0°C to +75°C and -55°C to +125°C temperature ranges.

### CONNECTION DIAGRAM Top View



NOTE: PIN 1 is marked for orientation.

**MAXIMUM :** IGS (Above which the useful life may be impaired)

Storage Tempe

Temperature (Ambient) Under Bias

-65°C to +150°C

Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous

-55°C to +125°C

DC Voltage Applied to Outputs for High Output State

-0.5 V to +7 V

DC Input Voltage

-0.5 V to +V<sub>CC</sub> max

Output Current, Into Outputs

-0.5 V to +5.5 V

DC Input Current

30 mA

-30 mA to +5.0 mA

**ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (Unless Otherwise Noted)

Am74182, Am634258X T<sub>A</sub> = 0°C to +75°C V<sub>CC</sub> = 5.0 V ± 5%  
 Am54182, Am634251X T<sub>A</sub> = -55°C to +125°C V<sub>CC</sub> = 5.0 V ± 10%

Parameters	Description	Test Conditions	Min	Typ (Note 1)	Max	Units
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = MIN., I <sub>OH</sub> = -0.8 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.4	2.9		Volts
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = MIN., I <sub>OL</sub> = 16.0 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>		0.2	0.4	Volts
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I <sub>IL</sub> (Note 2)	Unit Load Input LOW Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = 0.4 V		-1.0	-1.6	mA
I <sub>IH</sub> (Note 2)	Unit Load Input HIGH Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = 2.4 V		10	40	μA
	Input HIGH Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = 5.5 V			1.0	mA
I <sub>SC</sub>	Output Short Circuit Current	V <sub>CC</sub> = MAX., V <sub>OUT</sub> = 0.0 V	-40		-100	mA
I <sub>CC</sub>	Power Supply Current	V <sub>CC</sub> = MAX All outputs LOW	Am54182	45	65	mA
		Am74182	45	72		
		V <sub>CC</sub> = MAX All outputs HIGH	Am54182	27		mA
		Am74182	27			

Notes: 1) Typical limits are at V<sub>CC</sub> = 5.0 V, 25°C ambient and maximum loading.

2) Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

**SWITCHING CHARACTERISTICS** V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, N = 10 (C<sub>L</sub> = 15 pF, R<sub>L</sub> = 400 Ω)

Parameter	From (Input)	To (Output)	Test Figure	Test Conditions	Min	Typ	Max	Units
t <sub>pd+</sub>	C <sub>n</sub>	C <sub>n+</sub>	2	P <sub>0</sub> = P <sub>1</sub> = P <sub>2</sub> = 0 V G <sub>0</sub> = G <sub>1</sub> = G <sub>2</sub> = 4.5 V		12	17	ns
t <sub>pd-</sub>						15	22	
t <sub>pd+</sub>	P <sub>1</sub>	C <sub>n+</sub>	3	P <sub>1</sub> = 0 V (j < i) C <sub>n</sub> = G <sub>0</sub> = G <sub>1</sub> = G <sub>2</sub> = 4.5 V		8	12	ns
t <sub>pd-</sub>						9	13	
t <sub>pd+</sub>	G <sub>1</sub>	C <sub>n+</sub>	3	G <sub>1</sub> = 0 V (j < i) C <sub>n</sub> = P <sub>0</sub> = P <sub>1</sub> = P <sub>2</sub> = 4.5 V		8	12	ns
t <sub>pd-</sub>						9	13	
t <sub>pd+</sub>	P <sub>1</sub>	G <sub>0</sub> or P <sub>2</sub>	2	P <sub>1</sub> = 0 V (j < i) C <sub>n</sub> = G <sub>0</sub> = G <sub>1</sub> = G <sub>2</sub> = 4.5 V		12	17	ns
t <sub>pd-</sub>						15	22	
t <sub>pd+</sub>	G <sub>1</sub>	G <sub>0</sub>	2	G <sub>1</sub> = 0 V (j < i) C <sub>n</sub> = P <sub>0</sub> = P <sub>1</sub> = P <sub>2</sub> = 4.5 V		12	17	ns
t <sub>pd-</sub>						15	22	

## DEFINITION OF TERMS

### SUBSCRIPT TERMS:

**H** HIGH, applying to a HIGH logic level or when used with  $V_{CC}$  to indicate high  $V_{CC}$  value.

**I** Input.

**L** LOW, applying to LOW logic level or when used with  $V_{CC}$  to indicate low  $V_{CC}$  value.

**O** Output.

### FUNCTIONAL TERMS:

**C<sub>n</sub>** Active HIGH Carry In to the n'th ALU.

**C<sub>n+1</sub>** Active HIGH Carry Out to the (n+1)th ALU;  $l = x, y, z$ .

**FANOUT** The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

**$\bar{G}$**  Active LOW Carry Generate over the  $\bar{F}_i, \bar{G}_i$  inputs. This output is used with  $\bar{P}$  at the next level of look-ahead.

**$\bar{G}_i$**  Active LOW Carry Generate inputs to the look-ahead generator;  $i = 0, 1, 2, 3$ .

**$\bar{P}$**  Active LOW Carry Propagate output over the  $\bar{P}_i, \bar{G}_i$  inputs. This output is used with  $\bar{G}$  at the next level of look-ahead.

**$\bar{P}_i$**  Active LOW Carry Propagate Inputs to the look-ahead generator;  $i = 0, 1, 2, 3$ .

### OPERATIONAL TERMS:

**I<sub>IL</sub>** Forward input load current, for unit input load.

**I<sub>OH</sub>** Output HIGH current, forced out of output in  $V_{OH}$  test.

**I<sub>OL</sub>** Output LOW current, forced into the output in  $V_{OL}$  test.

**I<sub>IH</sub>** Reverse input current with  $V_{OH}$  applied to input.

**Negative Current** Current flowing out of the device.

**Positive Current** Current flowing into the device.

**V<sub>IH</sub>** Minimum logic HIGH input voltage.

**V<sub>IL</sub>** Maximum logic LOW input voltage.

**V<sub>OH</sub>** Minimum logic HIGH output voltage with output HIGH current  $I_{OH}$  flowing out of output.

**V<sub>OL</sub>** Maximum logic LOW output voltage with output LOW current  $I_{OL}$  into output.

### SWITCHING TERMS:

**t<sub>pd+</sub>** The propagation delay from a LOW to HIGH  $C_{i+1}, C_{i+2}, C_{i+3}, \bar{G}$  or  $\bar{P}$  output transition to a LOW to HIGH  $C_{i+1}, C_{i+2}, C_{i+3}, \bar{G}$  or  $\bar{P}$  output transition.

**t<sub>pd-</sub>** The propagation delay from a HIGH to LOW  $C_i$  or  $\bar{P}_i$  input transition to a HIGH to LOW  $C_{i+1}, C_{i+2}, C_{i+3}, \bar{G}$  or  $\bar{P}$  output transition.

## SWITCHING TIME TEST CIRCUIT & WAVEFORMS

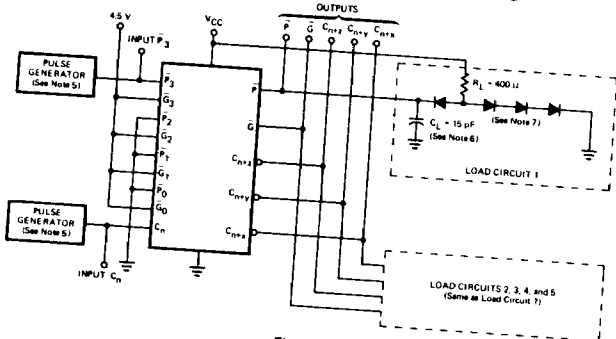


Figure 1

Note 5. The pulse generator has the following characteristic: Frequency = 1 MHz,  $Z_{out} \approx 50 \Omega$ , duty cycle = 50%.  
 6.  $C_L$  includes probe and jig capacitance.  
 7. All diodes are 1N5084.

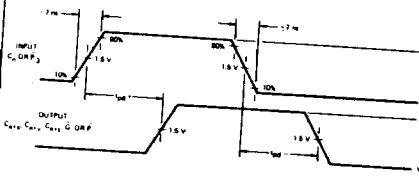


Figure 2

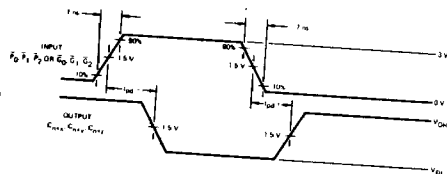
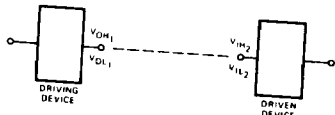
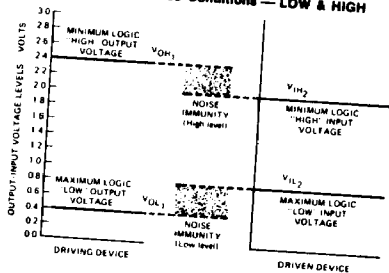


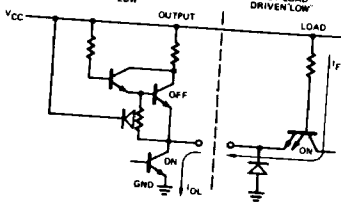
Figure 3

## INPUT/OUTPUT INTERFACE CONDITIONS

### Voltage Interface Conditions — LOW & HIGH



### Current Interface Conditions — LOW



### Current Interface Conditions — HIGH

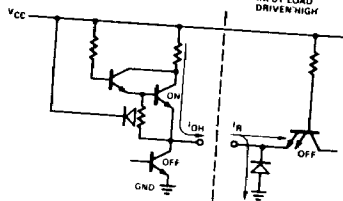
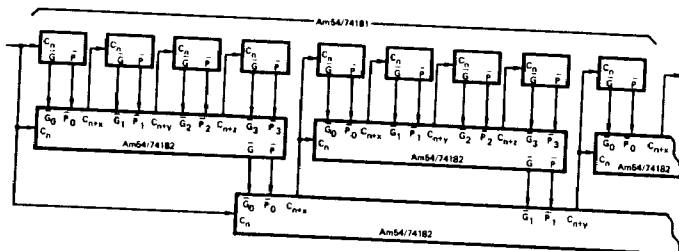


Figure 4



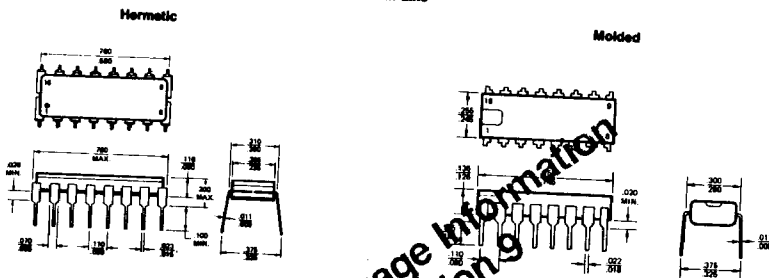
# Am54/74182 APPLICATION



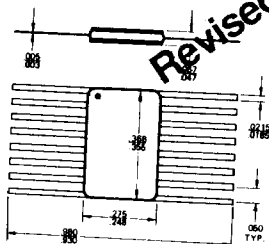
64-Bit ALU, Three Level Carry Look-Ahead

Figure 5

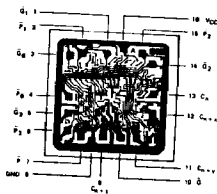
## PHYSICAL DIMENSIONS Dual-In-Line



## Flat Package



## Metalization and Pad Layout 68 x 68 Mils



**ADVANCED  
MICRO  
DEVICES INC.**  
901 Thompson Place  
Sunnyvale  
California 94086  
(408) 732-2400  
TWX: 910-339-9280  
TELEX: 34-6306

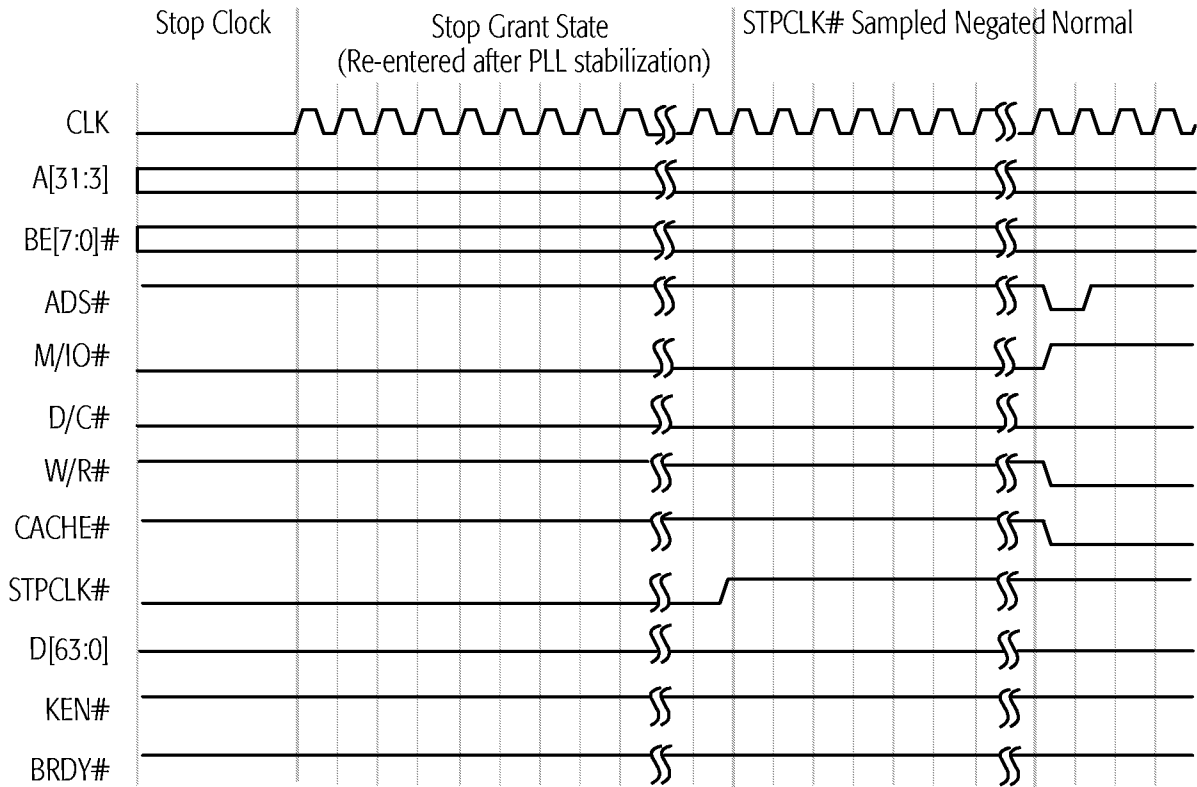


Figure 75. Stop Grant and Stop Clock Modes, Part 2

**INIT-Initiated  
Transition from  
Protected Mode to  
Real Mode**

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF\_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF\_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

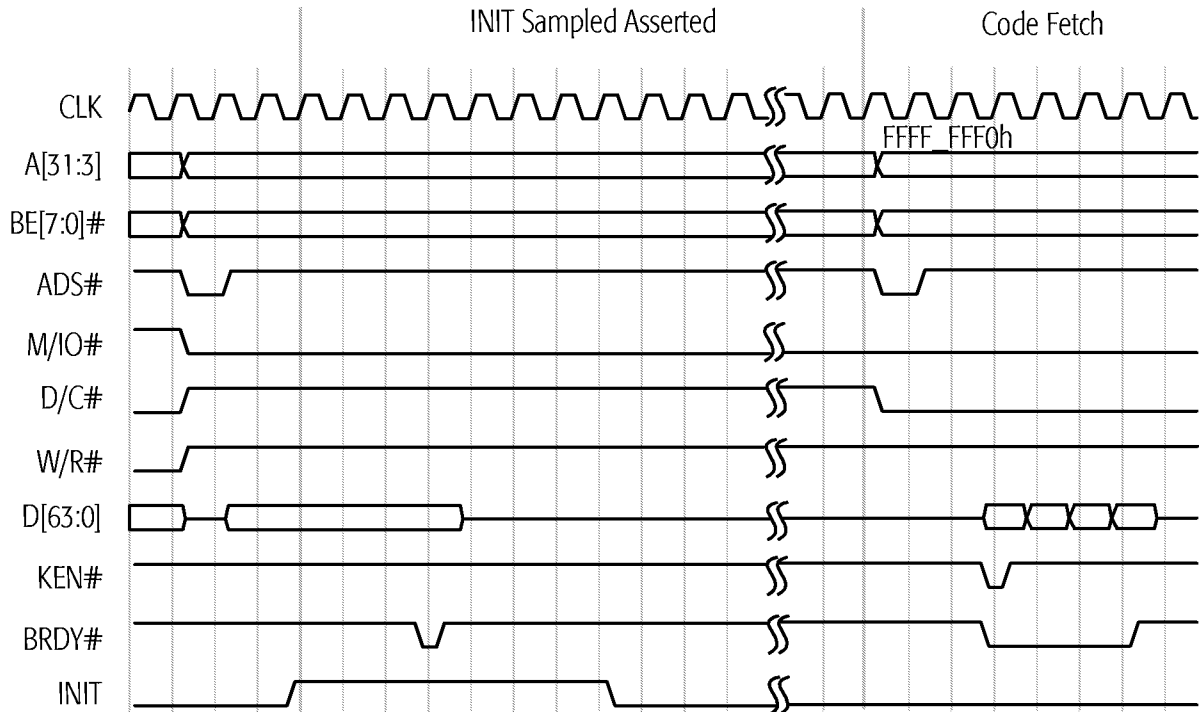


Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode



## 6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF\_FFF0h to start instruction execution.

### 6.1 Signals Sampled During the Falling Transition of RESET

- FLUSH#** FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF\_FFF0h to start instruction execution. (See “Built-In Self-Test (BIST)” on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See “Tri-State Test Mode” on page 218 and “FLUSH# (Cache Flush)” on page 103 for more details.)
- BF[2:0]** The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See “BF[2:0] (Bus Frequency)” on page 92 for the processor-clock to bus-clock ratios.)
- BRDYC#** BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See “BRDYC# (Burst Ready Copy)” on page 95 for more details.)

## 6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V<sub>CC</sub> reach specification. (See “CLK Switching Characteristics” on page 255 for clock specifications. See “Electrical Data” on page 247 for V<sub>CC</sub> specifications.)

During a warm reset while CLK and V<sub>CC</sub> are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

## 6.3 State of Processor After RESET

### Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

**Table 31. Output Signal State After RESET**

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACK#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	—	—

### Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.