2.0GHz Low Voltage Dual Modulus Prescaler

MC12031A
MC12031B

MECL PLL COMPONENTS

÷64/65, ÷128/129
LOW VOLTAGE
DUAL MODULUS PRESCALER

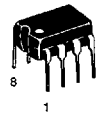
The MC12031 is a high frequency low voltage dual modulus prescaler used in phase–locked loop (PLL) applications. A high frequency input signal up to 2.0GHz is provided for cordless and cellular communication services such as DECT, PHS, and PCS. The MC12031 can be operated down to a minimum supply voltage of 2.7V required for battery operated portable systems.

The MC12031A can be used with CMOS synthesizer requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signal up to 2.0GHz in programmable frequency steps. The MC12031B can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

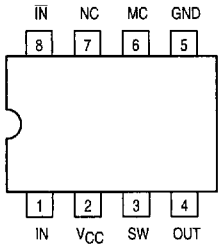
- 2.0GHz Toggle Frequency
- Supply Voltage 2.7V to 5.0Vdc
- Low Power 10.0mA Typical at V_{CC} = 2.7V
- Operating Temperature Range of –40 to +85°C
- The MC12031 is Pin and Functionally Compatible With the MC12022
- Short Setup Time (t_{set}) 8ns Typical at 2.0GHz
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL



P SUFFIX
PLASTIC PACKAGE
CASE 626–05

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–05

Pinout: 8–Lead Plastic (Top View)



For positive edge triggered synthesizers, order the MC12031A
For negative edge triggered synthesizers, order the MC12031B

FUNCTION TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H = V_{CC}; L = OPEN
MC: H = 2.0V to V_{CC}; L = GND to 0.8V

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage, Pin 2	–0.5 to +7.0	Vdc
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature Range	–65 to +150	°C
MC	Modulus Control Input, Pin 6	–0.5 to +6.5	Vdc
I_O	Maximum Output Current, Pin 4	10.0	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.0V; T_A = –40 to +85°C)

Symbol	Parameter		Min	Typ	Max	Unit
ft	Toggle Frequency (Sine Wave)		0.5	2.4	2.0	GHz
I_{CC}	Supply Current Output (Pin 2)	V_{CC} = 2.7V V_{CC} = 5.0V		10.0 13.0	12.5 16.0	mA
V_{IH1}	Modulus Control Input HIGH (MC)		2.0		V_{CC}+0.5V	V
V_{IL1}	Modulus Control Input LOW (MC)		GND		0.8	V
V_{IH2}	Divide Ratio Control Input HIGH (SW)		V_{CC}–0.5V	V_{CC}	V_{CC}+0.5V	V
V_{IL2}	Divide Ratio Control Input LOW (SW)		OPEN	OPEN	OPEN	—
V_{OUT}	Output Voltage Swing (Note 1)	C_L = 8pF; R_L = 1.2kΩ	0.8	1.2		V_{PP}
t_{set}	Modulus Setup Time MC to OUT @ 2000MHz			8	10	ns
V_{IN}	Input Voltage Sensitivity	500–2000MHz	100		1000	mV_{PP}
I_O	Output Current (Note 2)	V_{CC} = 2.7V, C_L = 8pF, R_L = 1.2kΩ V_{CC} = 5.0V, C_L = 8pF, R_L = 3.0kΩ		1.2 1.2	4.0 4.0	mA

1. Valid over voltage range 2.7 to 5.0V; R_L = 1.2kΩ @ V_{CC} = 2.7V; R_L = 3.0kΩ @ V_{CC} = 5.0V
2. Divide ratio of ÷64/65 @ 2.0GHz

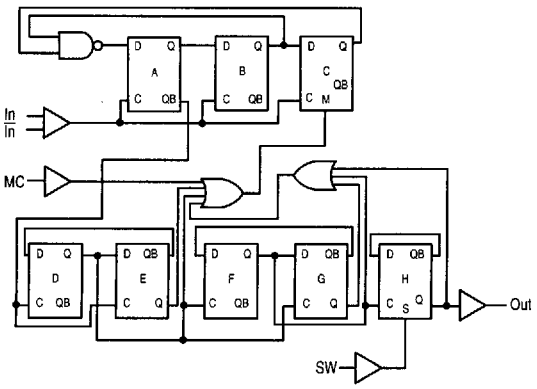
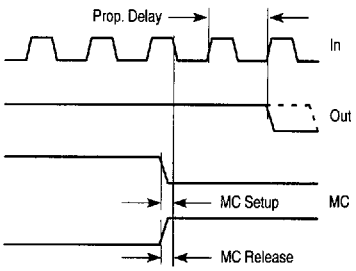
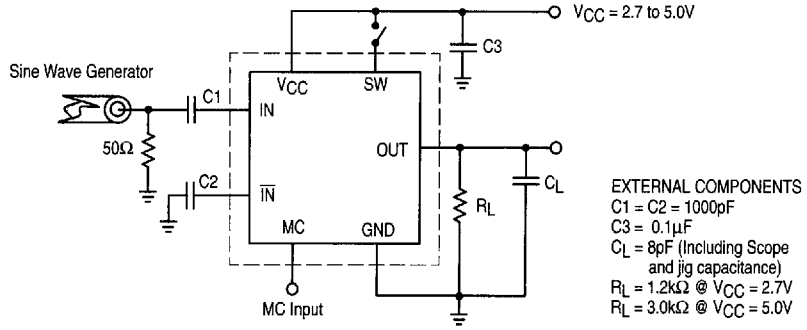


Figure 1. Logic Diagram (MC12031A)



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 2. Modulus Setup Time



EXTERNAL COMPONENTS
C1 = C2 = 1000pF
C3 = 0.1μF
C_L = 8pF (Including Scope and jig capacitance)
R_L = 1.2kΩ @ V_{CC} = 2.7V
R_L = 3.0kΩ @ V_{CC} = 5.0V

Figure 3. AC Test Circuit

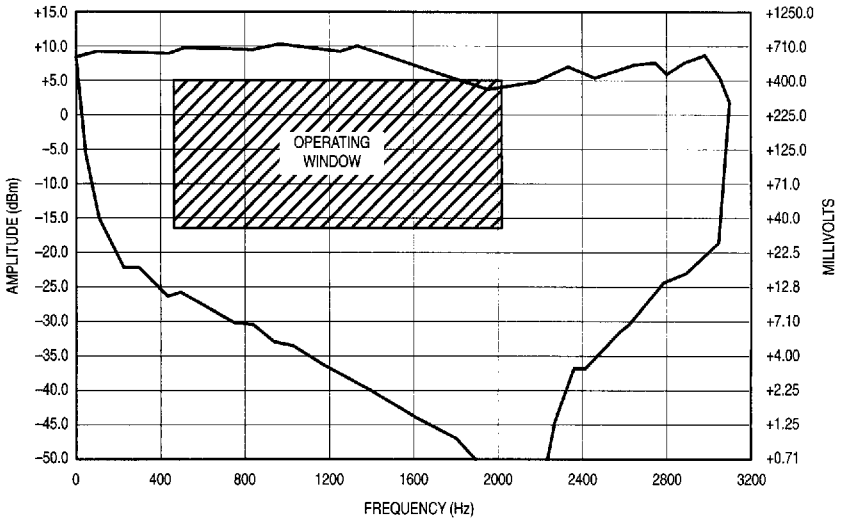


Figure 4. Input Signal Amplitude versus Input Frequency
Divide Ratio = 64; V_{CC} = 5.0V; T_A = 25°C

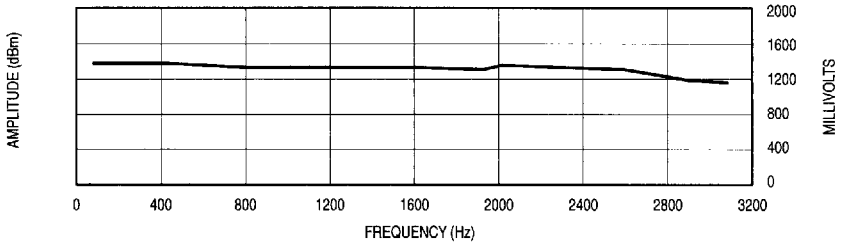


Figure 5. Output Amplitude versus Input Frequency

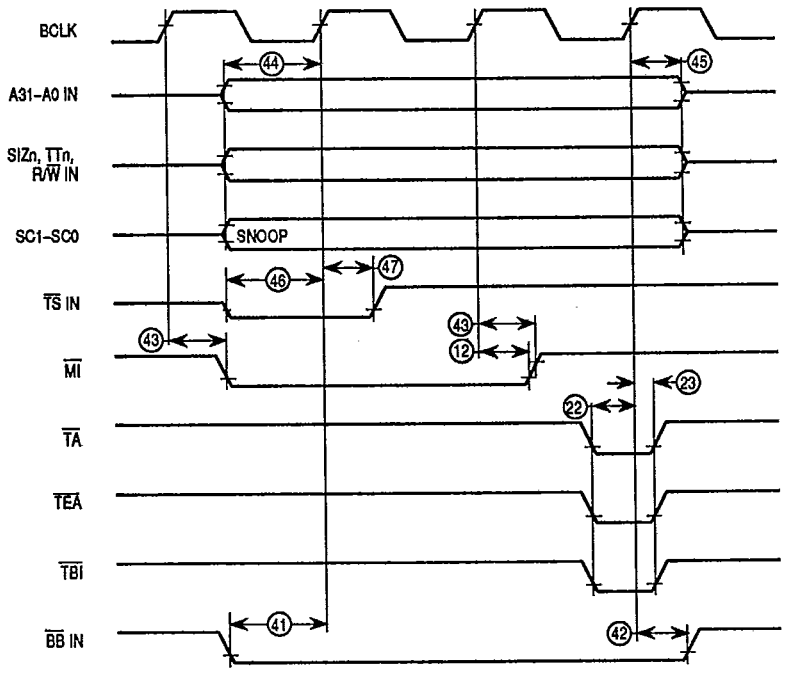


Figure 11-5. Snoop Miss Timing

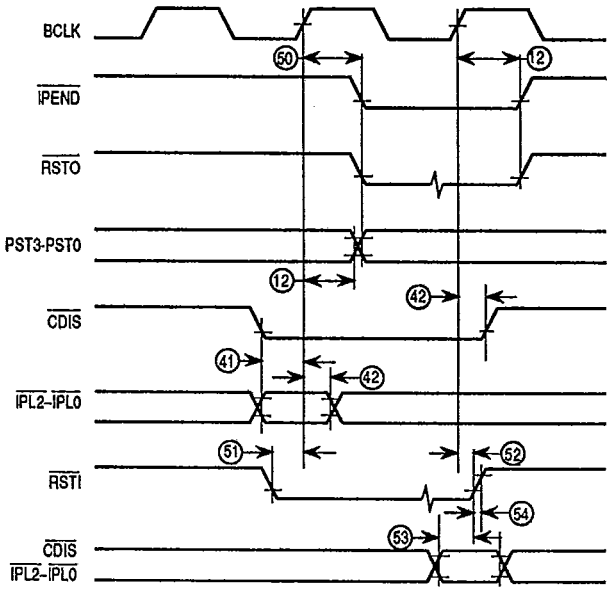


Figure 11-6. Other Signal Timing

SECTION 12
ORDERING INFORMATION AND MECHANICAL DATA

This section contains the pin assignments and package dimensions of the MC68EC040. In addition, detailed information is provided to be used as a guide when ordering.

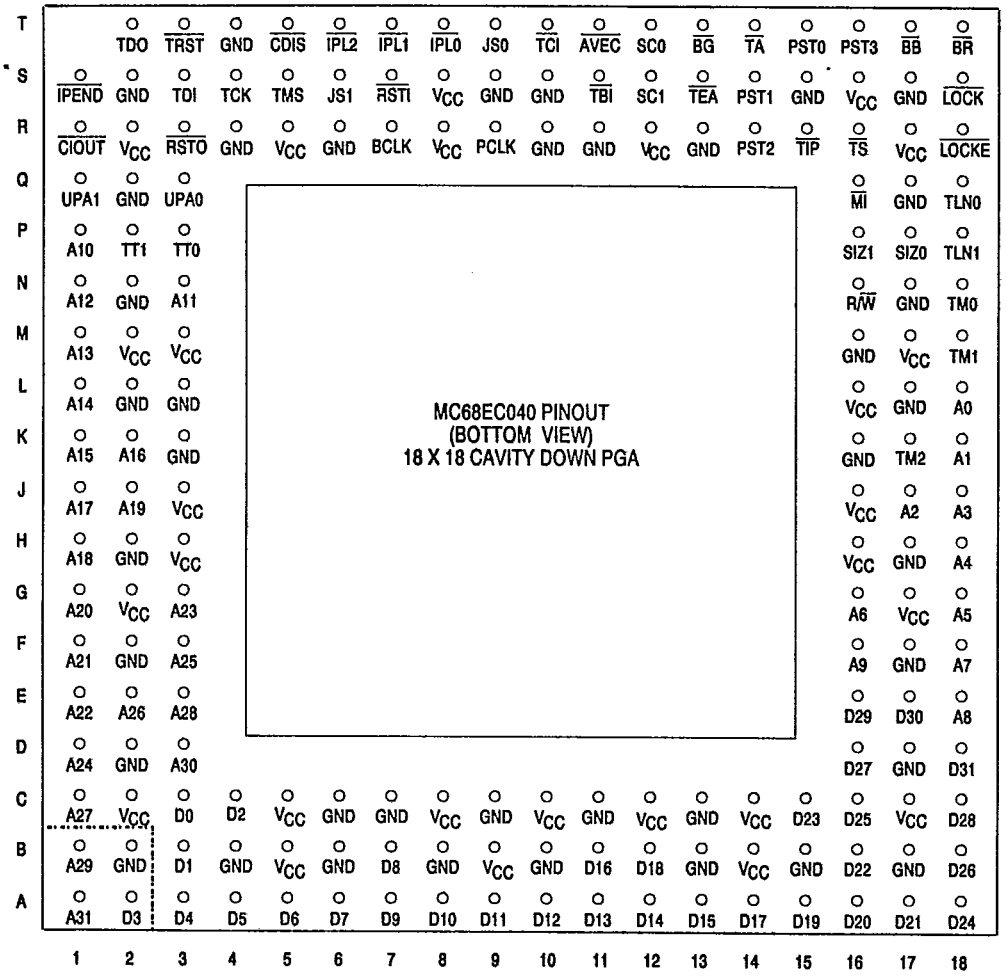
12.1 ORDERING INFORMATION

The following table provides ordering information pertaining to the package type frequency, temperature and Motorola order number for the MC68EC040.

Package Type	Frequency (MHz)	Temperature	Order Number
Pin Grid Array R Suffix	20.0	TBD	MC68EC040R20
Pin Grid Array R Suffix	25.0	TBD	MC68EC040R25
Pin Grid Array R Suffix	33.33	TBD	MC68EC040R33

12.2 PIN ASSIGNMENTS

The MC68EC040 is available in an 179-pin package. The following figure shows the pin assignment of the MC68EC040.

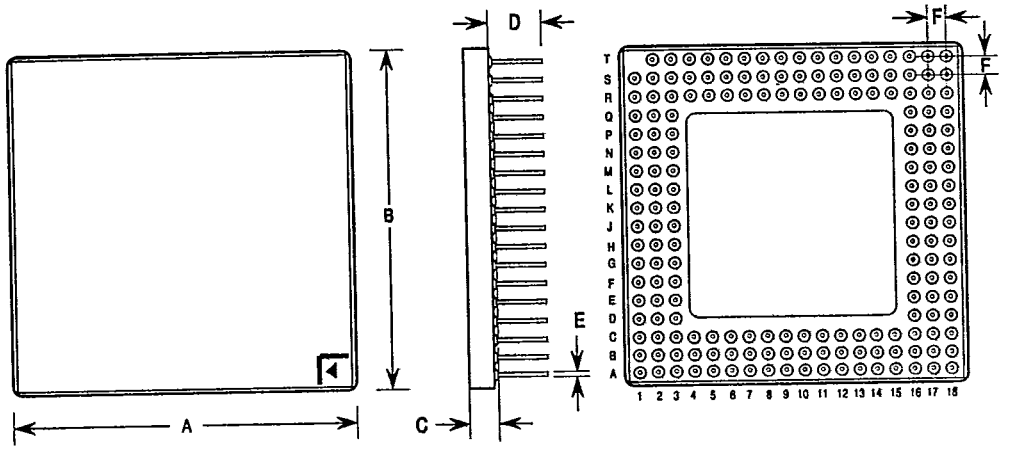


	GND	V_{CC}
PLL	S9, R6, R10	R8, S8
Internal Logic	C6, C7, C9, C11, C13,K3, K16, L3, M16, R4,R11, R13, S10, S10,T4	C5, C8, C10, C12, C14,H3, H16, J3, J16, L16,M3, R5, R12
Output Drivers	B2, B4, B6, B8, B10,, B13, B15, B17, D2, D17,F2, F17, H2, H17, L2,L17, N2, N17, Q2, Q17,S2, S15, S17	B5, B9, B14, C2, C17, G2, G17, M2, M17, R2, R17, S16

12.3 MECHANICAL DATA

The following figure provides the package dimensions for the MC68EC040.

Case To Be Determined



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	46.863	47.625	1.845	1.875
B	46.863	47.625	1.845	1.875
C	2.3876	2.9464	.094	.116
D	4.318	4.826	.170	.190
E	0.44	0.55	0.017	0.022
F	2.54 BSC		0.100 BSC	

12

APPENDIX A
M68000 FAMILY SUMMARY

This Appendix summarizes the characteristics of the microprocessors in the M68000 Family. The M68000PM/AD, *M68000 Programmer's Reference Manual* includes more detailed information on the M68000 Family differences.

Attribute	68000	68008	68010	68020	68030	68040	EC000	EC020	EC030	EC040
Data Bus Size (Bits)	16	8	16	8, 16, 32	8, 16, 32	32	16	8, 16, 32	8, 16, 32	32
Address Bus Size (Bits)	24	20	24	32	32	32	24	24	32	32
Instruction Cache (In Bytes)	—	—	3[1] (Words)	256	256	4096	—	256	256	4096
Data Cache (In Bytes)	—	—	—	—	256	4096	—	—	256	4096

NOTE 1: The MC68010 supports a 3-word cache for the loop mode.

Virtual Interfaces

MC68010, MC68020, MC68030, MC68EC020	Virtual Memory/Machine
M68040, MC68LC040	Virtual Memory
MC68010, MC68020, MC68030, MC68040,MC68LC040	Provide Bus Error Detection, Fault Recovery
MC68030, MC68040, MC68LC040	On-Chip MMU

Coprocessor Interface

MC68000, MC68008, MC68010, MC68EC000, MC68EC040, MC68LC040	Emulated in Software
MC68020, MC68030, MC68EC020, MC68EC030	In Microcode
MC68040	Emulated in Software (On-Chip Floating-Point Unit)

Word/Long Word Data Alignment

MC68000, MC68008, MC68010, MC68EC000	Word/Long Data, Instructions, and Stack Must be Word Aligned
MC68020, MC68030, MC68040, MC68EC020, MC68EC030, MC68EC040, MC68LC040	Only Instructions Must be Word Aligned (Data Alignment Improves Performance)