Preliminary Datasheet

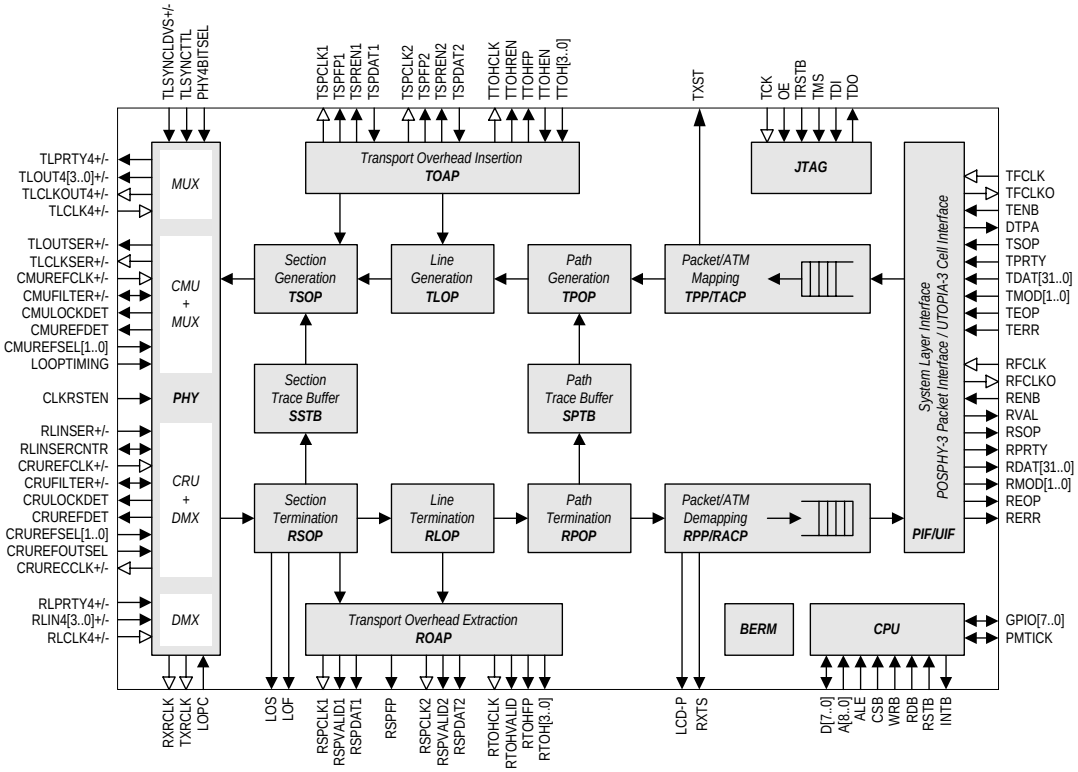
VSC9142

STS-48c Packet/ATM Over SONET/SDH Device
With Integrated Mux/Demux and Clock and Data Recovery

Features

- Dual Mode STS-48c/STM-16c to Packet/ ATM Framing Device for User Network Interface and Network Node Interface Applications
- Integrated 2.5 Gbps Clock and Data Recovery and Serial Clock and Data Output with Power-Down Feature
- Selectable Reference Clock Frequencies and Sources for Transmit and Receive datapaths
- Terminates and Generates Full SONET/SDH Section, Line, and Path Layers
- Dedictated Ports for Section/Line Overhead Access (Extraction/Insertion)
- Extensive SONET/Packet/Cell Performance Monitoring Features
- Programmable Packet/Cell Filtering and Discarding Functionalities
- Industry Compliant Drop Side Packet/Cell Interface for Single-PHY Applications
- 4-bit OIF Compliant Line Interface to be used-for STS-192 applications
- +1.8V and +3.3V Power Supplies
- Compliant with SONET and SDH Requirements as Stated in ANSI T1.105, Bellcore GR-253-CORE and ITU-T G.707 Documents
- Compliant with PPP in HDLC-like Framing and Mapping into SONET/SDH as Defined in IETF RDFC 1619/1661/1662/2615

VSC9142 Block Diagram



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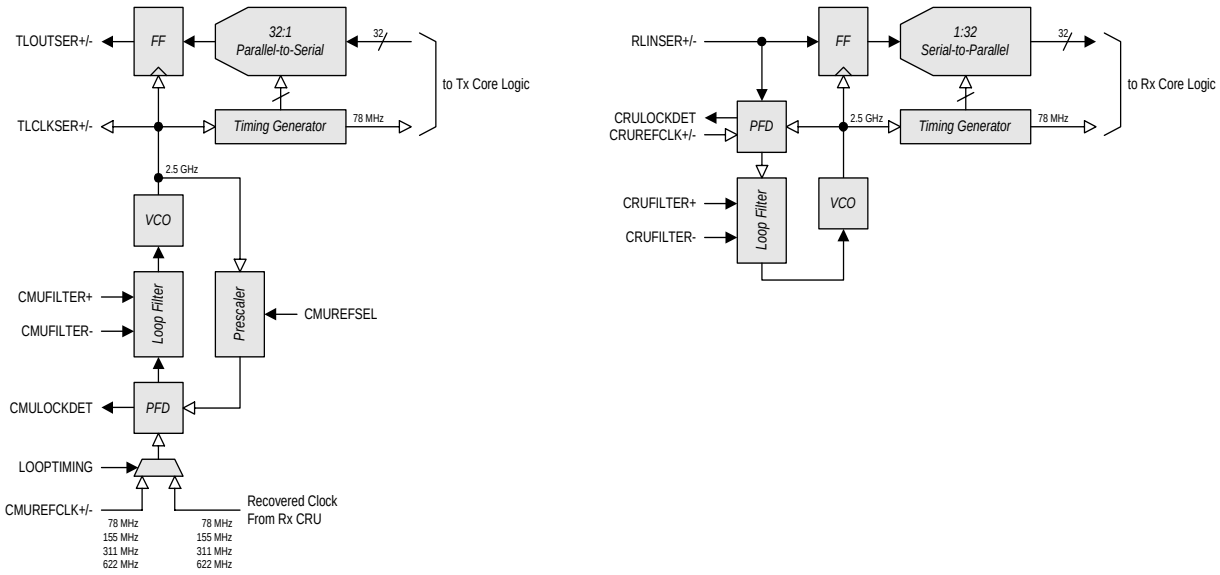
Integrated PHY Block Diagram



Functional Overview

The VSC9142 is a dual mode SONET/SDH to Packet/ATM framing device that integrates the physical layer components of 2.5 Gbps clock and data recovery and serialization/deserialization into a single device. In the Packet over SONET (POS) mode, this device can be used in equipment interconnecting IP/PPP/HDLC data over public or private SONET/SDH networks. Similarly, in the ATM over SONET (ATM) mode, this device can be used in equipment interconnecting ATM switches. In addition, the VSC9142 can be used in various applications involving LAPS (X.85/Y.1321) and Ethernet over SONET/SDH protocols.

Features of the VSC9142 include: Full insertion/extraction of the transport overhead, bit error rate and extensive SONET/packet/cell performance monitoring, packet/cell filtering and discarding functionalities, transmit and receive, JTAG TAP controller, and an 8-bit CPU interface with 8 general purpose I/O ports.

The high-speed component provides data and clock in the transmit direction, and selectable reference clock frequencies and sources for both the transmit and receive directions. The VSC9142 can facilitate both internal and external looptiming applications and also provides a 4-bit LVDS interface in both transmit and receive direction for use in STS-192 applications. When using the 4-bit interface, the serializing/deserializing blocks of the VSC9142 can be shut down for power savings.

This highly integrated device provides a complete low-power physical layer solution on a single chip for Packet/ATM over SONET/SDH at the STS-48 rate.

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Line Interface (PHY)

- A Loss of Optical Carrier (LOPC) input signal is provided for monitoring and alarm purposes.
- Selectable CMU Reference Clock for the transmit serial interface.
- Selectable CRU Reference Clock for the serial interface.
- CMU Lock Detect and Reference Detect indicators are available for the transmit serial interface.
- CRU Lock Detect and Reference Detect indicators are available for the receive serial interface.
- Internal and External Looptiming are avaliable between the CRU and the CMU.
- The CRU clock output can be selected to be the recovered clock from the incoming serial stream or from an external clock. This feature can be used for looptiming applications under LOS conditions.
- The serial interface or the 4-bit parallel interface can be selected using the PHY4BITSEL pin. Only one interface can be used at any time.
- Power-Down feature for the unused interface can be done by connecting the positive power supply pins of the unused block to GND. Both serial and 4-bit parallel interfaces can be both independently powered down.
- A parity bit, programmable for even/odd parity, is provided each for the incoming and outgoing parallel datapaths.
- TLSYNC is provided for the parallel interface and is used for STS-192 applications.
- A reference clock output derived from the receive clock input can be programmed to be 8kHz, 19MHz, 38MHz, or 78MHz frequency locked to the receive clock.
- A reference clock output derived from the transmit clock input can be programmed to be 8kHz, 19MHz, 38MHz, or 78MHz frequency locked to the transmit clock.

Receive Section Overhead Processor (RSOP)

- Two mechanisms for frame alignment are provided. One is based on searching for A1/A2 framing patterns and the other uses an external frame pulse (RLFP). The latter is intended for STS-192 applications.
- 12/24/48-bit A1/A2 framing patterns are supported.
- Out Of Frame (OOF) and Loss Of Frame (LOF) alarm condition are detected.
- The incoming data stream is optionally descrambled using the generating polynomial $1 + x^6 + x^7$ with a sequence length of 127.
- Section BIP-8 (B1) errors are detected and accumulated. Both individual and block mode accumulation of B1 error indications are supported.
- The incoming data stream, before descrambling, is monitored for absence of transitions or “all-zero patterns”. The Loss Of Signal (LOS) detection and termination criterias are programmable.

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- It is possible to force insertion of all "1" in the data stream, except for the Section overhead. The Line AIS (AIS-L) condition may be automatically inserted in case of LOS, LOF, or Loss of Optical Carrier (LOPC) alarm events.
- It is possible to extract the entire Section overhead through the Receive Overhead Access Port (ROAP).
- The J0, E1, F1, and D1-D3 bytes can be extracted from the Section overhead and inserted into bytes on the special purpose ports of the ROAP.

Receive Line Overhead Processor (RLOP)

- The Line Remote Defect Indication (RDI-L) and Line Alarm Indication Signal (AIS-L) alarms carried in the K2 byte are extracted and filtered. The filter constants are programmable.
- Line BIP-384 errors carried in the B2 bytes are detected and accumulated. Both individual and block mode accumulation of B2 errors are supported.
- Line REI error indications carried in the M1 byte are accumulated. Both individual and block mode accumulation of M1 error indications are supported.
- The Synchronization Status carried in the S1 byte is extracted and filtered. Unstable and mismatch alarms are supported. The filter constants are programmable.
- The Automatic Protection Switching (APS) bytes, K1 and K2, are extracted and filtered. Unstable alarm is supported. The filter constants are programmable.
- It is possible to extract the entire Line overhead through the ROAP.
- The D4-D12, S1, E2, K1-K2 bytes can be extracted from the Line overhead and inserted into bytes on the special purpose ports of the ROAP.

Receive Path Overhead Processor (RPOP)

- The H1 and H2 pointer bytes are detected and interpreted according to ANSI T1.105 and ITU-T G.707. The mechanism is programmable to support both SONET and SDH. Path Alarm Indication Signal (AIS-P) and Loss of Pointer (LOP-P) alarm declarations are provided. Several pointer functions are also provided for diagnostic purposes.
- The H1 and H2 pointer bytes are monitored for Concatenation Indication (CI). Loss of Pointer (LOPX) and AIS (AISX) alarm declarations are provided.
- Path BIP-8 errors carried in the B3 byte are detected and accumulated. Both individual and block mode accumulation of B3 errors are supported.
- Path REI error indications carried in the G1 byte are detected and accumulated. Up to 64000 individual errors can be detected per second. Both individual and block mode accumulation of Path REI error indications are supported.
- The Path RDI carried in the G1 byte is detected and programmable.
- The Signal Label carried in the C2 byte is detected, alarmed and is programmable.

Receive Packet Processor (RPP)

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- The byte value used to identify the HDLC Flag Sequence is programmable.
- The detection and discarding of invalid frames are programmable.
- The expected Control Escape byte value and the Octet Destuffing Masking byte are programmable.
- The expected Address and Control Field values are programmable.
- The Protocol Field declaration and processing is programmable.
- The Abort Sequence is detected in the incoming HDLC frames.
- The received Frame Check Sequence (FCS) field is verified. The FCS checksum is calculated using either a 16-bit, CRC-CCITT generating polynomial $1 + x^5 + x^{12} + x^{16}$, or a 32-bit, CRC-32 generating polynomial $1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$.
- The received data is descrambled with the self synchronizing scrambler (SSS) polynomial $1 + x^{43}$. Full and/or partial descrambling can be independently enabled/disabled.
- Long and short packet checking are provided and are programmable.
- Self Describing Padding is supported and programmable.
- The storage of the PPP Protocol Field in the Rx FIFO may be enabled/disabled.
- The size of the Rx FIFO size is 4095 words, which may accommodate storage for a total of 16380 PPP Protocol/Information Field bytes.
- The definition of received "errored" HDLC frames is programmable. For these errored HDLC frames two different procedures can be applied.
- A filtering function is provided to perform packet discartion and error marking based on a set of programmable labels. There are four programmable label matching triggers, and one compliment word matching trigger that functions the packet discard and TERR marking.
- The following statistics are provided in the performance monitoring 32-bit counters:
  - Received Aborted HDLC frames
  - Received FCS errored HDLC frames
  - Received Empty HDLC frames
  - Received HDLC frames where Address-and-Control-Field-Compression was found
  - Received Long packets
  - Received Short packets
  - Received Invalid Frames
  - Received bytes pre-octet destuffing
  - Received bytes post-octet destuffing
  - Received number of frames excluding Invalid Frames
  - Packets discarded by label filtering
  - Packets error-marked by label filtering
  - Packets stored in the Rx FIFO

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- Packets stored in the Rx FIFO that are error marked
- Packet bytes stored in the Rx FIFO
- Number of received PPP padding bytes

• The SPE Transparent Mode is provided to allow all of the SPE payload to pass directly to the Rx FIFO without further processing.

• A timestamp signal RXTS is provided to indicate when the first word of a packet is written into the Rx FIFO.

Receive ATM Cell Processor (RACP)

• Cell Delineation is provided using shortened cyclic code with a generating polynomial $1 + x + x^2 + x^8$. The coset polynomial $1 + x^2 + x^4 + x^8$ can be added to the calculated HEC check bits before comparison.

• Single-bit header error correction is supported. The dropping of cells during single or multiple error detection is programmable.

• The 48 byte information field is descrambled with a self-synchronizing descrambler polynomial $1 + x^{43}$. Descrambling can be enabled/disabled.

• Cells can be filtered based on a programmable cell header pattern in the GFC, PTI, or CLP fields.

• The number of correctable and uncorrectable HEC errors detected, and the number of cells written to the Rx FIFO are monitored.

• The Rx FIFO can accommodate storage of eight ATM cells.

Drop Side Interface (POS/ATM Interface)

• A parity bit, programmable for even/odd parity, is provided for each transmit and receive datapaths.

• The Drop Side Interface provides an industry compliant packet interface for POS operations.

• The packet interface supports word-level and packet-level transfer modes.

• The DTPA signal is provided to indicate the waterlevel of the Tx FIFO counted at word level and is programmable.

• It is possible to force reset/flush the contents in the Tx FIFO via the CPU interface.

• It is possible to force reset/flush the contents in the Rx FIFO via the CPU interface.

• The Drop Side Interface provides a Single-PHY UTOPIA-3 interface for ATM operations.

• Two formats of the ATM cells are supported: 52 byte cell or 56 byte cell containing the HEC.

• The UTOPIA-3 interface supports both word-level and cell-level flow control.

Transmit ATM Cell Processor (TACP)

• The ATM cells are mapped into the STS-48c SPE or equivalent SDH VC-16-16c. Programmable idle/unassigned cells are inserted into the cell stream.

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- The 48 byte information field is scrambled with a self-synchronizing descrambler polynomial $1 + x^{43}$. Scrambling can be enabled/disabled.
- The HEC generator performs a CRC-8 calculation over the first four header octets using the generating polynomial $1 + x + x^2 + x^8$. The coset polynomial $1 + x^2 + x^4 + x^6$ can be added to the result. The HEC is optionally inserted into the fifth octet of the header of cells read from the Tx FIFO.
- The Tx FIFO can accomodate storage of eight ATM cells.

Transmit Packet Processor (TPP)

- The inserted HDLC Flag Sequence byte and the minimum number of Flag Sequence bytes separating HDLC frames are programmable.
- The insertion of the Address and Control fields can be controlled by the HDLC Address-and-Control-Field-Compression mechanism.
- The Address Field inserted after the beginning Flag Sequence is programmable.
- The Control Field inserted after the the Address Field is programmable.
- The Frame Check Sequence (FCS) can be generated using either a 16-bit, CRC-CCITT generating polynomial $1 + x^5 + x^{12} + x^{16}$, or a 32-bit CRC-32 generating polynomial $1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$.
- Octet Stuffing, or “escaping”, can be applied after the FCS generation and partial scrambling, if enabled. The Control Escape byte and the Octet Stuffing Masking byte are programmable. The Asyc-Control-Character-Map (ACCM) can accommodate a maximum of 5 byte values. Each value can be individually enabled/disabled.
- The transmitted data is scrambled with a self-synchronizing scrambler (SSS) polynomial $1 + x^{43}$. Full and/or partial scrambling can be independently enabled/disabled.
- The PPP Protocol Field can be generated internally or extracted from the transmit FIFO. The size and value of the inserted Protocol Field are programmable when generated internally.
- The Tx FIFO is programmable in the range from 1 to 4095 words or 16380 bytes of data storage. All valid packet bytes stored in the Tx FIFO are read out and mapped into the PPP Protocol/Information Fields of generated PPP/HDLC frames.
- Two Tx PIF packet transfer modes are supported: packet transfer mode and word transfer mode.
- The TXF_ERR signal is provided to force insertion of errors into the FCS, or to force abort the transmitted HDLC frame.
- It is possible to force XOR'ing of the transmitted Address, Control or Protocol Fields with a programmable mask value via the CPU interface for diagnostic purposes.
- The following statistics are provided in the performance monitoring 32-bit counters:
  - Bytes read from Tx FIFO
  - Transmitted good HDLC frames (non-aborted, non-FCS errored)

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- Transmitted Aborted HDLC frames
- Transmitted FCS Errored HDLC frames
- Long packets read from Tx FIFO
- Short packets read from Tx FIFO
- Transmitted empty HDLC frames
- Bytes pre octet-stuffing (excluding Abort sequences)
- Bytes post octet-stuffing (excluding Abort sequences)

• The SPE Transparent Mode is provided to allow the Tx FIFO content to be passed directly into the SPE payload without further processing.

• A timestamp signal TXTS is provided to indicate when the first word of a packet is read from the Tx FIFO.

Transmit Path Overhead Processor (TPOP)

• The H1 and H2 pointer byte values are programmable to support both SONET and SDH. Several pointer functions are provided for diagnostics purposes. The remaining 47 H1 and H2 bytes are programmable.

• The Path BIP-8 is computed and placed in the B3 byte of the current frame. It is possible to insert B3 errors for diagnostic purposes.

• The number of Path BIP-8 errors detected in the Receive Path Overhead Processor (RPOP) is backreported as Path REI in the G1 byte. Both individual and block mode backreporting for G1 are supported.

• It is possible to enable/disable RDI-P insertion for each of the following alarms: LOS, LOF, AIS-L, AIS-P, LOP-P, TIM-P, UNEQ-P, LCD-P and PLM-P. Both the latest and earlier definitions of RDI-P are supported.

• The Path Signal Label (C2) byte value is programmable.

• The Path Trace (J1) byte value is programmable.

• The F2, H4, Z3, Z4, and Z5 bytes are programmable.

Transmit Line Overhead Processor (TLOP)

• It is possible to insert programmable sets of K1 and K2 bytes into the outgoing data stream.

• RDI-L can be automatically inserted during the detection of an LOS, LOF, or AIS-L alarm in the receive data stream.

• The Line BIP-384 code is computed and placed in the B2 bytes of the current frame. It is possible to insert B2 errors for diagnostics purposes.

• The number of Line BIP-384 errors detected in the Receive Line Overhead Processor (RLOP) is backreported as Line REI in the M1 byte. Up to 255 errors can be backreported per frame in individual mode. Both individual and block mode backreporting for M1 are supported. It is possible to insert M1 error indications for diagnostics purposes.

• The Synchronization Status value inserted in the S1 byte is programmable.

- Bytes input to the special purpose ports of the Transmit Overhead Access Port (TOAP) can be inserted into the D4-D12, E2, S1, K1 and K2 bytes of the outgoing Line overhead.
- All bytes in the line overhead that are reserved for national or future international standardization use can be overwritten with 0x00.
- The H1, H2, and H3 bytes from the Transmit Overhead Access Port (TOAP) can be inserted into the H1, H2, and H3 overhead bytes, or applied as an error mask to the H1, H2, and H3 overhead bytes.

Transmit Section Overhead Processor (TSOP)

- It is possible to forced insert all "1"s into the data stream, before scrambling, with the exception of the section overhead. The AIS-L condition can be automatically inserted through activity from the special purpose serial interfaces.
- The Section BIP-8 code is computed and can be placed in the B1 byte of the current frame. It is possible to insert B1 errors for diagnostics purposes.
- The A1 and A2 framing bytes can be inserted into the frame. It is also possible to introduce bit errors in the framing word.
- The J0 byte supports both SONET and SDH formats. The J0 byte can be programmed to a fixed value for interworking with older equipment implementing the C1 indentification byte.
- The Z0 growth bytes supports both SONET and SDH formats. The Z0 bytes can be programmed to carry the C1 identification bytes for interworking with older equipment.
- The outgoing data stream is optionally scrambled using the generating polynomial $1 + x^6 + x^7$ with a sequence length of 127.
- It is possible to force insert all “0”s in the outgoing data stream after scrambling for diagnostic purposes (LOS).
- Bytes input to the special purpose ports of the TOAP can be inserted into the D1-D3, E1, F1 and J0 bytes of the outgoing Section overhead.
- All bytes in the section overhead that are reserved for national or future international standardization use can be overwritten with 0x00.
- A frame pulse is provided for the outgoing data stream and is programmable.

Receive Overhead Access Port (ROAP)

- Two identical, but independent, special purpose ports are provided for the extraction of special purpose bytes from the SONET/SDH transport overhead and of certain SONET/SDH alarms specific to automatic protection switching (APS) applications.
- The entire section/line transport overhead can be extracted from the serial output port RTOH[3..0].

Transmit Overhead Access Port (TOAP)

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- Two identical, but independent, special purpose ports are provided for the insertion of special purpose bytes into the SONET/SDH transport overhead and of certain SONET/SDH alarms specific to automatic protection switching (APS) applications.
- The entire transport overhead is captured from the serial input ports TTOH[3..0]. The captured data can be selectively inserted into the corresponding overhead bytes of the transmitted SONET/SDH frame.

SONET/SDH Section Trace Buffers (SSTB)

- Three different Section Trace Message (J0) formats are supported in both transmit and receive directions: one byte (SONET) message, 16 byte (SDH) message, and 64 byte (SONET CLLI) message.
- The received section trace message is checked for persistency. A mismatch alarm is supported.

CPU Interface

- All configuration bits are both writeable and readable and can be accessed regardless of the device clock source status, except for the reset state. Configuration bits include selection bits, interrupt masking bits, and programmable counter/control values.
- Eight programmable General Purpose Input/Output (GPIO) ports are available for monitoring and controlling external signals. All GPIOs support bistable interrupts when configured as input ports.
- Clock activity monitors are implemented for all input clocks.

Bit Error Rate Monitoring

- Bit error rate monitoring is based on the Line BIP (B2) error code and is capable of measuring BERs down to 10^{-10}.
- There are four independent BER monitors with individual accumulation periods and alarm thresholds.
- A saturation threshold is implemented for each BER monitor to specify the maximum number of errors that can be accumulated per frame.
- The BER Signal Degrade (BER-SD) alarm is based on BER monitors 1 and 2.
- The BER Signal Fail (BER-SF) alarm is based on BER monitors 3 and 4.

JTAG

- Standard IEEE 1149.1 compliant JTAG interface.

Loopback Modes

- Equipment loopback is supported by looping the output from the Transmit Section Overhead Processor (TSOP), in the transmit direction, back to the input of the Receive Section Overhead Processor (RSOP), in the receive direction.
- Facility loopback is supported by looping the data received on the receive Line Side Interface back to the transmit Line Side Interface.
- Section loopback is supported by looping the output from the Recieve Section Overhead Processor (RSOP) in the receive direction back to the input of the Transmit Section Overhead Processor (TSOP), in the transmit direction.

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- Line loopback is supported by looping the output from the Recieve Line Overhead Processor (RLOP) in the receive direction back to the input of the Transmit Line Overhead Processor (TLOP), in the transmit direction.
- Drop side loopback is supported by looping the output from the Tx FIFO to the input of the Rx FIFO. This loopback is supported for both packet and ATM cell mode.

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AC Characteristics

Figure 1: Tx Serial Line Interface Timing Dependencies

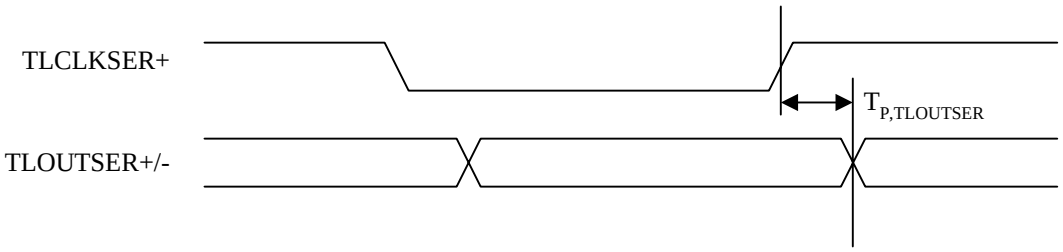

Table 1: Tx Serial Line Interface

Symbol	*Description*	*Min*	*Max*	*Unit*
$f_{TLCLKSER}$	TLCLKSER+/- clock frequency (nominal)	-	2488	MHz
$T_{dc, TLCLKSER}$	TLCLKSER+/- duty cycle	40	60	%
$T_{r/f, TLCLKSER}$	TLCLKSER+/- rise/fall time (20-80%)	-	120	ps
$T_{p, TLOUTSER}$	TLCLKSER+ rising edge to TLOUTSER+/- valid	-75	+75	ps
T_{JS}	Output Data Jitter RMS	-	4	ps
$T_{JS, Peak}$	Output Data Jitter Peak-to-Peak	-	40	ps
CMU Reference Clock Frequencies are 78 MHz, 155 MHz, 311 Mhz, and 622 MHz *Jitter tested to SONET specifications with 2ps RMS jitter on the Reference Clock*				

Figure 2: Rx Parallel Line Interface Timing Dependencies

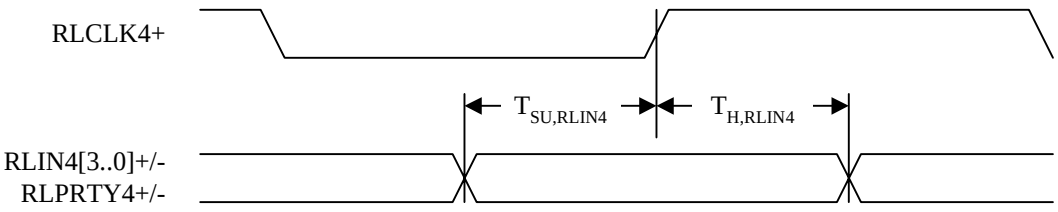

Table 2: Rx Parallel Line Interface

Symbol	*Description*	*Min*	*Max*	*Unit*
f_{RLCLK4}	RLCLK4+/- clock frequency (nominal)	-	622.08	MHz
$T_{dc, RLCLK4}$	RLCLK4+/- duty cycle	45	55	%

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Symbol	*Description*	*Min*	*Max*	*Unit*
$T_{r/f, RLCLK4}$	RLCLK4+/- rise/fall time (20-80%)	-	200	ps
$T_{jitter, RLCLK4}$	RLCLK4+/- cycle-to-cycle		100	ps
$T_{su, RLIN4}$	RLIN4[3..0]+/-, RLPRTY4+/- setup time to RLCLK4+ rising edge	+300	-	ps
$T_{h, RLIN4}$	RLIN4[3..0]+/-, RLPRTY4+/- hold time to RLCLK4+ rising edge	+300	-	ps

Figure 3: Tx Parallel Line Interface Timing Dependencies

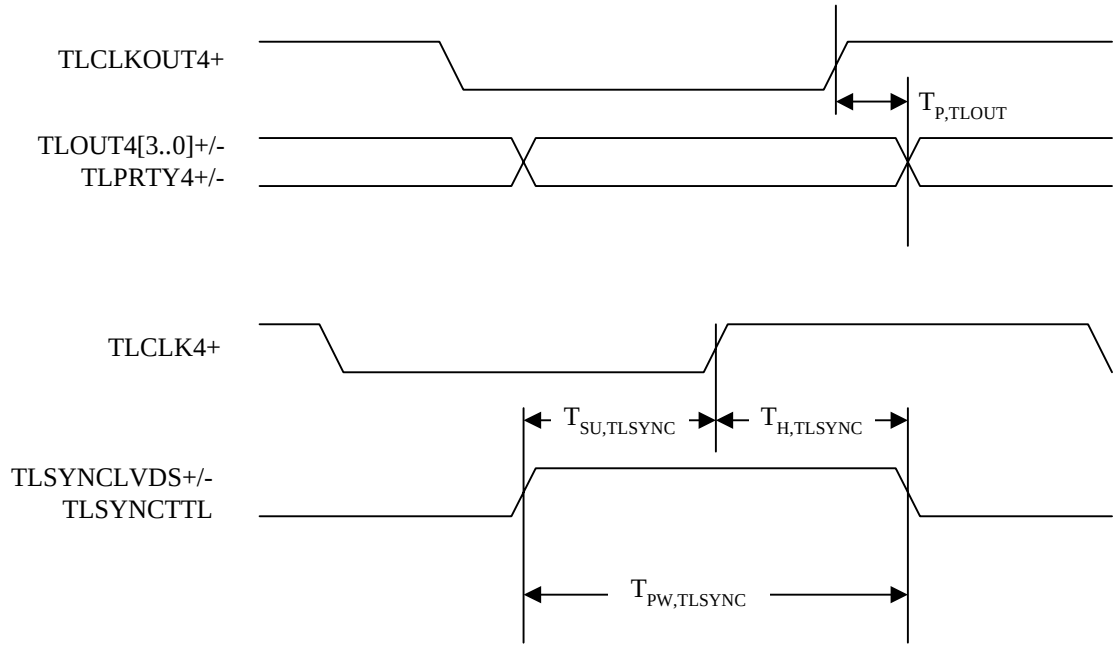

Table 3: Tx Parallel Line Interface

Symbol	*Description*	*Min*	*Max*	*Unit*
$f_{TLCLKOUT4}$	TLCLKOUT4+/- clock frequency (nominal)	-	622.08	MHz
$T_{dc, TLCLKOUT4}$	TLCLKOUT4+/- duty cycle	40	60	%
$T_{r/f, TLCLKOUT4}$	TLCLKOUT4+/- rise/fall time (20-80%)	-	200	ps
$T_{p, TLOUT}$	TLCLKOUT4+ rising edge to TLOUT4[3..0]+/-, TLPRTY4+/- valid	-200	+200	ps
f_{TLCLK4}	TLCLK4+/- clock frequency (nominal)	-	622.08	MHz
$T_{dc, TLCLK4}$	TLCLK4+/- duty cycle	45	55	%
$T_{r/f, TLCLK4}$	TLCLK4+/- rise/fall time (20-80%)	-	200	ps
$T_{jitter, TLCLK4}$	TLCLK4+/- cycle-to-cycle jitter		100	ps
$T_{su, TLSYNC}$	TLSYNC setup time to TLCLK4+ rising edge[1)]	300	-	ps

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Table 3: Tx Parallel Line Interface

$T_{h,\ TLSYNC}$	TLSYNC hold time from TLCLK4+ rising edge[1)]	300	-	ps
$T_{PW,TLSYNC}$	TLSYNC pulse width	8/ f_{TLCLK}	-	ns

1) TLSYNCLVDS may be asynchronous. In this case the pulse width needs to be at least 9 TLCLK periods when f_{TLCLK} is 622.08 MHz.
TLSYNCTTL is asynchronous. For proper sampling the pulse width needs to be at least 9 TLCLK periods when f_{TLCLK} is 622.08 MHz.

Figure 4: Rx Drop Interface Timing Dependencies

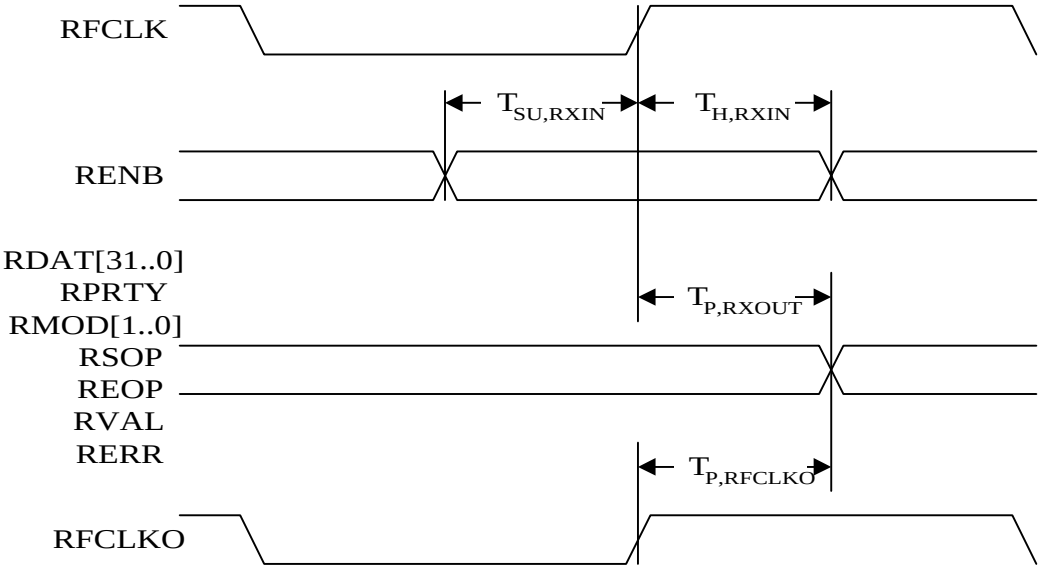

Table 4: Rx Drop Interface

Symbol	*Description*	*Min*	*Max*	*Unit*
f_{RFCLK}	RFCLK Clock Frequency (nominal)	50	104	MHz
dc_{RFCLK}	RFCLK Duty Cycle	40	60	%
$T_{R/F,\ RFCLK}$	RFCLK Rise/Fall Time	-	2.0	ns
dc_{RFCLKO}	RFCLKO Duty Cycle	dc_{RFCLK} - (1.0 ns x f_{RFCLK})%		%
$T_{SU,\ RXIN}$	RENB Setup Time to RFCLK Rising Edge	2.0	-	ns
$T_{H,\ RXIN}$	RENB Hold Time to RFCLK Rising Edge	0.5	-	ns
$T_{P,\ RXOUT}$	RFCLK Rising Edge to RDATA[31..0], RPRTY, RMOD[1..0], RSOP, REOP, RVAL and RERR Valid	1.0	6.0	ns [1)]
		0.5	4.2	ns [2)]
$T_{P,\ RFCLKO}$	RFCLKO Rising Edge RDAT[31..0], RPRTY, RMOD[1..0], RSOP, REOP, RVAL and RERR Valid	-0.5	-2.0	ns [3)]

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Table 4: Rx Drop Interface

Symbol	*Description*	*Min*	*Max*	*Unit*

1) *Output times are for 25 pF load.*
2) *Output times are for 5 pF load.*
3) *Output times are for 5 to 15 pF load.*

Figure 5: Tx Drop Interface Timing Dependencies

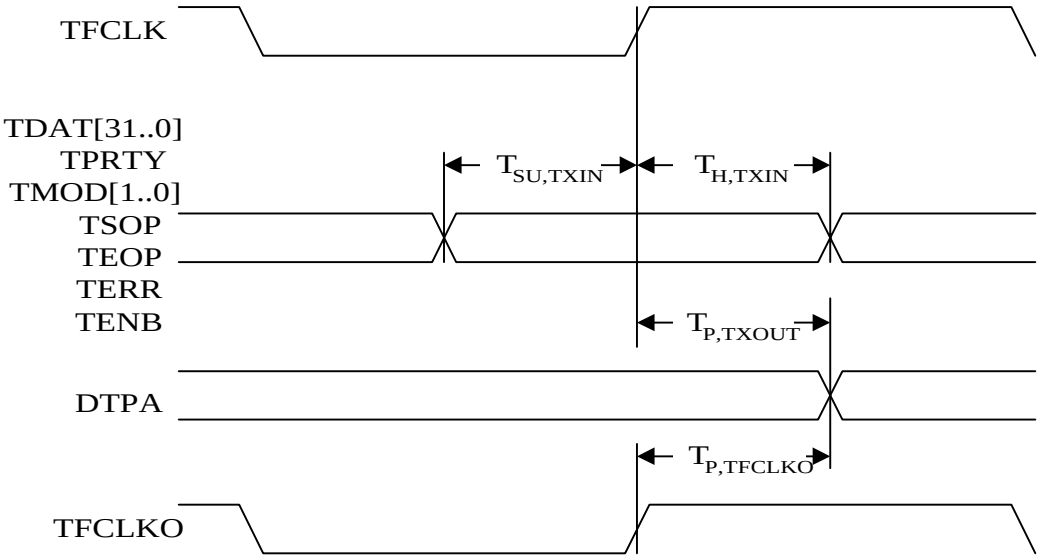

Table 5: Tx Drop Interface

Symbol	*Description*	*Min*	*Max*	*Unit*
f_{TFCLK}	TFCLK Clock Frequency	50	104	MHz
dc_{TFCLK}	TFCLK Duty Cycle	40	60	%
$T_{R/F, TFCLK}$	TFCLK Rise/Fall Time	-	2.0	ns
dc_{TFCLKO}	TFCLKO Duty Cycle	dc_{TFCLK} - (1.0 ns x f_{TFCLK})%		%
$T_{SU, TXIN}$	TDAT[31..0], TPRTY, TMOD[1..0], TSOP, TEOP, TERR and TENB Setup Time to TFCLK Rising Edge	2.0	-	ns
$T_{H, TXIN}$	TDAT[31..0], TPRTY, TMOD[1..0], TSOP, TEOP, TERR and TENB Hold Time to TFCLK Rising Edge	0.5	-	ns
$T_{P, TXOUT}$	TFCLK Rising Edge to DTPA Valid	1.0	6.0	ns 1)
		0.5	4.2	ns 2)
$T_{P, TFCLKO}$	TFCLKO Rising Edge to DTPA Valid.	-0.5	-2.0	ns 3)

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Table 5: Tx Drop Interface

Symbol	*Description*	*Min*	*Max*	*Unit*

1) Output times are for 25 pF load.
2) Output times are for 5 pF load.
3) Output times are for 5 to 15 pF load.

Figure 6: Rx Overhead Access Port Timing Dependencies

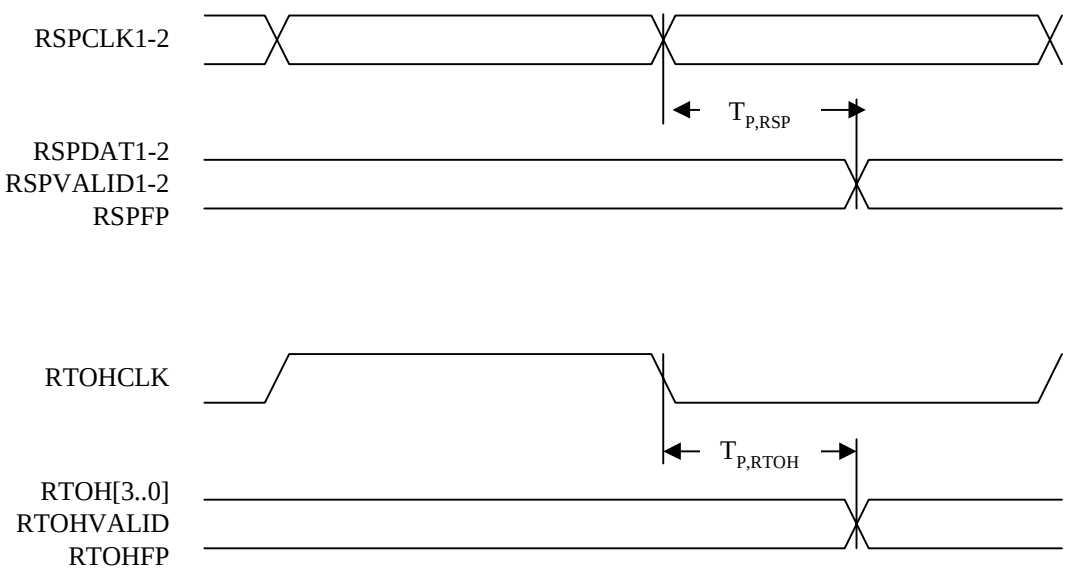

Table 6: Rx Overhead Access Port

Symbol	*Description*	*Min*	*Max*	*Unit*
f_{RSPCLK}	RSPCLK1-2 Clock Frequency (optionally gapped)	-	2.16	MHz
dc_{RSPCLK}	RSPCLK1-2 Duty Cycle	40	60	%
$T_{R/F, RSPCLK}$	RSPCLK1-2 Rise/Fall Time	-	2.0	ns
$T_{P, RSP}$	RSPCLK1-2 Rising/Falling Edge[2] to RSPDAT1-2, RSPVALID1-2, RSPFP Valid	-6.0	+15.0	ns
$f_{RTOHCLK}$	RTOHCLK Clock Frequency (nominal)	-	38.88	MHz
$dc_{RTOHCLK}$	RTOHCLK Duty Cycle	40	60	%
$T_{R/F, RTOHCLK}$	RTOHCLK Rise/Fall Time	-	2.0	ns
$T_{P, RTOH}$	RTOHCLK Rising/Falling Edge[3] to RTOH[0..3], RTOHVALID, RTOHFP Valid	-3.0	+7.0	ns

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Table 6: Rx Overhead Access Port

Symbol	*Description*	*Min*	*Max*	*Unit*
2) Active edge of clock is programmable for group of inputs for each independent port. *3) Active edge of clock is programmable for group of inputs.* *All output times are for 50 pF load.*				

Figure 7: Tx Overhead Access Port Timing Dependencies

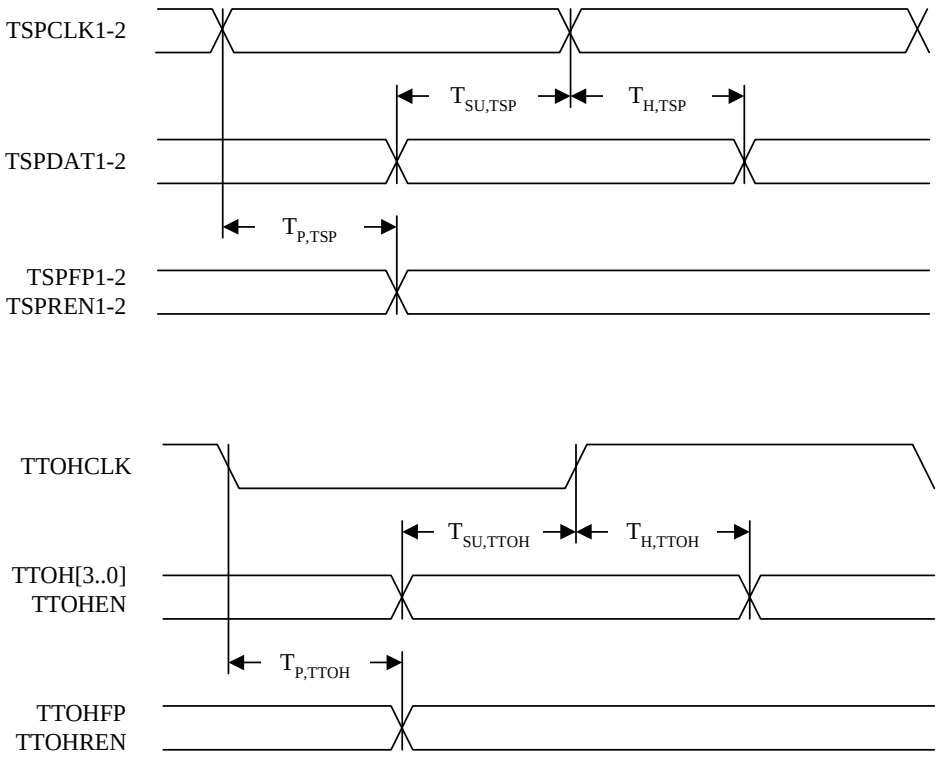

Table 7: Tx Overhead Access Port

Symbol	*Description*	*Min*	*Max*	*Unit*
f_{TSPCLK}	TSPCLK1-2 Clock Frequency (optionally gapped)	-	2.16	MHz
dc_{TSPCLK}	TSPCLK1-2 Duty Cycle	40	60	%
$T_{R/F, TSPCLK}$	TSPCLK1-2 Rise/Fall Time	-	2.0	ns
$T_{SU, TSP}$	TSPDAT1-2 Setup Time to TSPCLK1-2 Rising/Falling Edge[5)]	25.0	-	ns
$T_{H, TSP}$	TSPDAT1-2 Hold Time to TSPCLK1-2 Rising/Falling Edge[5)]	0	-	ns
$T_{P, TSP}$	TSPCLK1-2 Rising/Falling Edge[6)] to TSPREN1-2, TSPFP1-2 Valid	-10.0	+20.0	ns

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Table 7: Tx Overhead Access Port

Symbol	*Description*	*Min*	*Max*	*Unit*
$f_{TTOHCLK}$	TTOHCLK Clock Frequency (nominal)	-	38.88	MHz
$dc_{TTOHCLK}$	TTOHCLK Duty Cycle	40	60	%
$T_{R/F, TTOHCLK}$	TTOHCLK Rise/Fall Time	-	2.0	ns
$T_{SU, TTOH}$	TTOH[0..3], TTOHEN Setup Time to TTOHCLK Rising/Falling Edge[7)]	15.0	-	ns
$T_{H, TTOH}$	TTOH[0..3], TTOHEN Hold Time to TTOHCLK Rising/Falling Edge[7)]	-1.0	-	ns
$T_{P, TTOH}$	TTOHCLK Rising/Falling Edge[8)] to TTOHREN, TTOHFP Valid	-3.0	+7.0	ns

5) Active edge of clock is programmable for group of inputs for each independent port.
6) Active edge of clock is programmable for group of outputs for each independent port.
7) Active edge of clock is programmable for group of inputs.
8) Active edge of clock is programmable for group of outputs.
All output times are for 50 pF load.

Figure 8: JTAG Interface Timing Dependencies

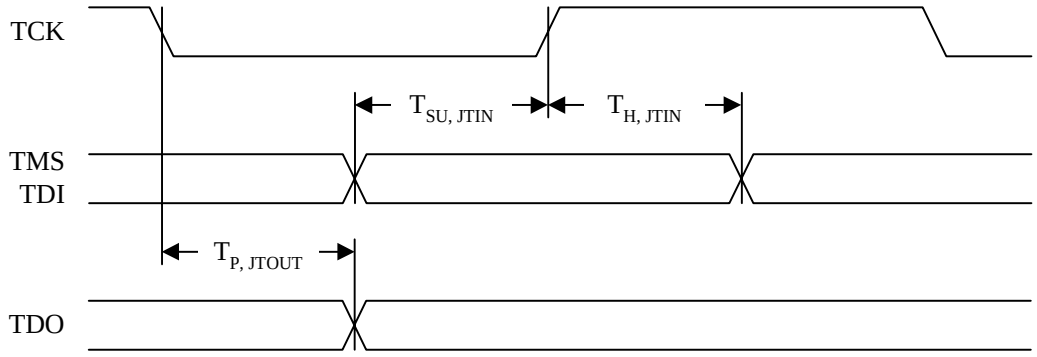

Table 8: JTAG Interface

Symbol	*Description*	*Min*	*Max*	*Unit*
f_{TCK}	TCK Frequency	-	1	MHz
dc_{TCK}	TCK Duty Cycle	40	60	%
$T_{SU, JTIN}$	TMS/TDI Setup Time to TCK Rising Edge	50	-	ns
$T_{H, JTIN}$	TMS/TDI Hold Time to TCK Rising Edge	50	-	ns
$T_{P, JOUT}$	TCK Falling Edge to TDO Valid	1.5	50	ns

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Figure 9: CPU Read Access Timing Dependencies

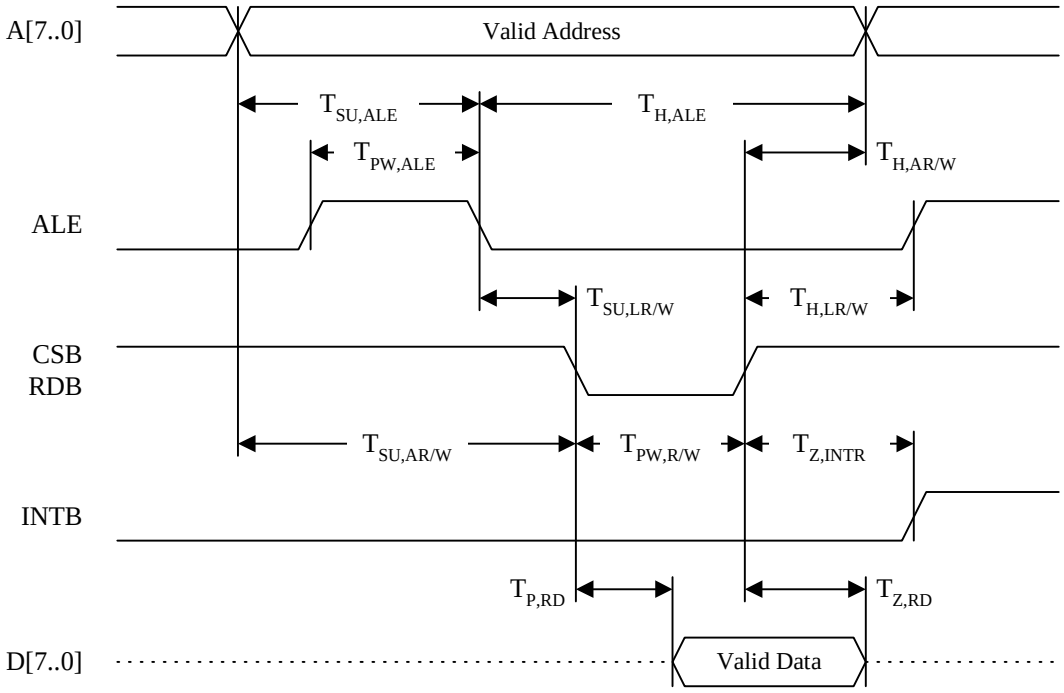

Figure 10: CPU Write Access Timing Dependencies

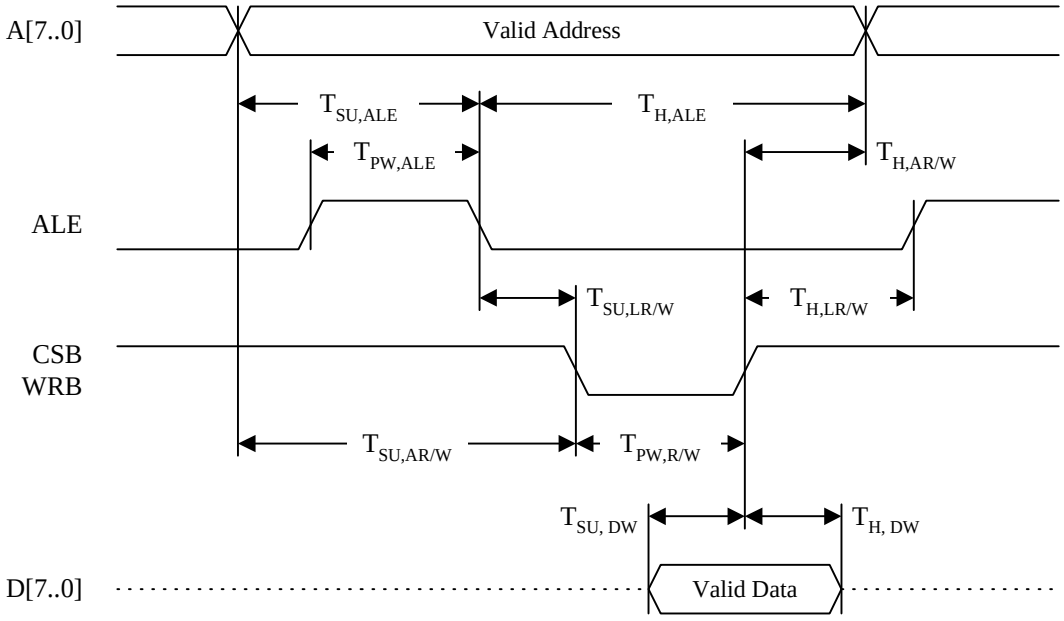

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Table 9: CPU Read/Write Access

Symbol	*Description*	*Min*	*Max*	*Unit*
$T_{SU, ALE}$	Address to Address Latch Setup Time	10	-	ns
$T_{H, ALE}$	Address to Address Latch Hold Time	10	-	ns
$T_{PW, ALE}$	Address Latch Pulse Width	20	-	ns
$T_{SU, LR/W}$	Latch to Valid Read/Write Setup Time	0	-	ns
$T_{H, LR/W}$	Latch to Valid Read/Write Hold Time	5	-	ns
$T_{SU, AR/W}$	Address to Valid Read/Write Setup Time	10	-	ns
$T_{H, AR/W}$	Address to Valid Read/Write Hold Time	10	-	ns
$T_{PW, R/W}$	Valid Read/Write Pulse Width	25	-	ns
$T_{SU, DW}$	Data to Valid Write Setup Time	20	-	ns
$T_{H, DW}$	Data to Valid Write Hold Time	10	-	ns
$T_{P, RD}$	Valid Read to Valid Data Propagation Delay	-	80	ns
$T_{Z, RD}$	Valid Read Negated to Output Tristate	1	25	ns
$T_{Z, INTH}$	Valid Read Negated to Interrupt Release/Pull-down	-	100	ns
$T_{PW, PMTICK, H/L}$	PMTICK High and Low Requirements	50	-	ns
All output times are for 100 pF load.				

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DC Characteristics

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage (TTL)	V_{DD33}-0.2	—	V	V_{DD}=Min , V_{DD33}=Min, I_{OH} = -0.2, -0.4, -0.6, -0.8, -1.2, -1.6 mA
V_{OH}	Output HIGH voltage (TTL)	V_{DD33}-0.5	—	V	V_{DD}=Min, V_{DD33}=Min, I_{OH} = -2, -4, -6, -8, -12, -16 mA
V_{OL}	Output LOW voltage (TTL)	—	0.2	V	V_{DD}=Min, V_{DD33}=Min, I_{OL} = 0.2 , 0.4, 0.6, 0.8, 1.2, 1.6 mA
V_{OL}	Output LOW voltage (TTL)	—	0.4	V	V_{DD}=Min, V_{DD33}=Min, I_{OL} =2 , 4, 6, 8, 12, 16 mA
V_{IH}	Input HIGH voltage (TTL)	2.0	V_{DD33} + 0.5	V	Guaranteed Logic HIGH Level
V_{IL}	Input LOW voltage (TTL)	-0.3	0.8	V	Guaranteed Logic LOW Level
I_{IH}	Input high current (TTL)	—	+/- 1	µA	V_{DD33}=Max, $V_{IH, MAX}$
I_{IL}	Input low current (TTL)	—	+/- 1	µA	V_{DD33}=Max, V_I=GND
$V_{OCM, LVDS}$	O/P Common Mode Range (LVDS)	0.90	1.50	V	100 ohms Termination Between True and Compliment Signals
$\Delta V_{OUT, LVDS}$	Differential Output Voltage (LVDS)	250	450	mV	100 ohms Termination Between True and Compliment Signals
$V_{ICM, LVDS}$	I/P Common Mode Range (LVDS)	0	2.40	V	
$\Delta V_{IN, LVDS}$	Differential Input Voltage (LVDS)	100	600	mV	
$I_{IP, LVDS}$	Input current (LVDS)	TBD	TBD	µA	TBD
$V_{OCM, PECL}$	O/P Common Mode Range (PECL)	0.90	1.35	V	100 ohm Termination Between True and Compliment Signals
$\Delta V_{OUT, PECL}$	Differential Output Voltage (PECL)	0.50	0.95	mV	100 ohms Termination Between true and Compliment Signals
$V_{ICM, PECL}$	I/P Common Mode Range (PECL)	1.40	V_{DD33} - 0.5	V	
$\Delta V_{IN, PECL}$	Differential Input Voltage (PECL)	0.10	1.20	V	
$I_{IP, PECL}$	Input current (PECL)	TBD	TBD	µA	TBD

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Power Dissipation

Parameter	*Description*	*(Typ)*	*(Max)*	*Units*
I_{33}	3.3V power supply current	368	435	mA
I_{18}	1.8V power supply current	730	875	mA
P_D	Power dissipation	2.5	3.0	W

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Absolute Maximum Ratings(1)

Power Supply Voltage (V_{DD}) Potential to GND ..... -0.5V to + 2.5V
Power Supply Voltage (V_{DD33}) Potential to GND ..... -0.5V to + 4.6V
DC Input Voltage (LVDS Inputs) ..... -0.5V to V_{DD33} + 0.5V
DC Input Voltage (PECL Inputs) ..... -0.5V to V_{DD33} + 0.5V
DC Input Voltage (TTL Inputs) ..... -0.5V to V_{DD33} + 0.5V
DC Output Voltage (LVDS Inputs) ..... -0.5V to V_{DD33} + 0.5V
DC Output Voltage (PECL Inputs) ..... -0.5V to V_{DD33} + 0.5V
DC Output Voltage (TTL Outputs) ..... -0.5V to V_{DD33} + 0.5V
Output Current (LVDS Outputs) ..... +/- 50mA
Output Current (PECL Outputs) ..... +/- 50mA
Output Current (TTL Outputs) ..... +/- 50mA
Case Temperature Under Bias ..... -55 ^{o}C to +125 ^{o}C
Storage Temperature ..... -65 ^{o}C to +150 ^{o}C
Maximum Input ESD (Human Body Model) ..... 2000 V

[1] *Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*

Recommended Operating Conditions

Power Supply Voltage (V_{DD33}) ..... +3.3V +/- 5%
Power Supply Voltage (V_{DD}) ..... +1.8V +/- 5%

Operating Temperature Range* (T) ..... -24^{o} to 90^{o}C

** Lower limit and upper limit of specifications are in ambient temperature with no air flow.*

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Package Pin Description

Signal	*Name*	*I/O*	*Type*	*Description*
RLINSER+/-	Serial Line Receive Data	I	PECL	Serial line data input.
RLINSERCNTR +/-	Serial Line Receive Data Center Tap	-	PECL	RLINSER+/- has a 100 ohms across on-chip termination with a center tap connection at 50 ohms.
CRUREFCLK+/-	CRU Reference Clock	I	PECL	Differential reference clock input to the CRU.
CRUREFDET	CRU Reference Clock Detect	O	TTL	Active high status pin to indicate condition of the CRU reference clock
CRULOCKDET	CRU Lock Detect	O	TTL	Active high status pin to indicate lock condition of the CRU reference clock.
CRUFILTER+/-	CRU Loop Filter	I	-	External CRU loop filter pins. The true loop filter pin is connected via 0.1uF capacitor to the complement loop filter pin.
CRUREFSEL[1..0]	CRU Reference Clock Select	I	TTL	Selects the frequency of the CRU reference clock to 622/311/155/78MHz
CRURECCLK+/-	CRU Recovered Clock	O	PECL	The recovered or reference clock (2.5 GHz) scaled to the frequency selected by CRUREFSEL[1..0].
RLIN4[3..0]+/-	Parallel Line Receive Data	I	LVDS	Parallel data bus for the incoming STS-48/STM-16 data stream. RLIN4[3] is the most signififcant bit. RLIN4[3]is the first arriving bit on the serial data stream and is sampled on the rising edge of RLCLK4.
RLCLK4+/-	Parallel Line Receive Clock	I	LVDS	Clock reference for the parallel line receive datastream carried in RLIN4[3..0]. The clock frequency is nominally 622MHz.
RLPRTY4+/-	Parallel Line Receive Parity	I	LVDS	Parity input (even/odd parity) for the parallel receive line datastream RLIN4[3..0]. RLPRTY4 is sampled on the rising edge of RLCLK4.
TLOUTSER+/-	Serial Line Transmit Data	O	PECL	Serial line data output.
TLCLKSER +/-	Serial Line Transmit Clock	O	PECL	Serial line clock output. It can be used to retiming the serial line data output.
CMUREFCLK +/-	CMU Reference Clock	I	PECL	Differential reference clock to the CMU.
CMUREFDET	CRU Reference Clock Detect	O	TTL	Active high status pin to indicate condition of the CMU reference clock
CMULOCKDET	CMU Lock Detect	O	TTL	Active high status pin to indicate lock condition of the CRU reference clock.

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Signal	*Name*	*I/O*	*Type*	*Description*
CMUFILTER+/-	CMU Loop Filter	I	-	External CMU loop filter pins. The true loop filter pin is connected via 0.1uF capacitor to the complement loop filter pin.
CMUREFSEL [1..0]	CMU Reference Clock Select	I	TTL	Selects the frequency of the CMU reference clock to 622/ 311/155/78MHz
TLOUT4[3..0]+/-	Parallel Line Transmit Data	O	LVDS	Parallel data bus for the outgoing STS-48/STM-16 data stream. TLOUT4[3] is the most significant bit. TLOUT4[3] is the first transmitted bit on the serial data stream. TLOUT4[3...0] is generated on the rising edge of the incoming TLCLK4.
TLCLK4+/-	Parallel Line Transmit Clock	I	LVDS	Clock reference for the parallel line transmit datastream carried in TLOUT4[3...0]. The clock is nominally 622 MHz.
TLCLKOUT4+/-	Parallel Line Transmit Looped Clock		LVDS	Looped TLCLK4 signal. The clock is nominally 622 MHz.
TLPRTY4+/-	Parallel Line Transmit Parity	O	LVDS	Parity output (even/odd parity) for the parallel line transmit datastream TLOUT4[3...0] is generated on the rising edge of the incoming TLCLK4.
TLSYNCLVDS+ /-	Synchronization (LVDS)	I	LVDS	TLSYNC is used for synchronously resetting the device transmit processor only. TLSYNC is intended for use in STS-192/STM-64 applications.
TLSYNCTTL	Synchronization (TTL)	I	TTL	TLSYNC is used for synchronously resetting the device transmit processor only. TLSYNC is intended for use in STS-192/STM-64 applications.
PHY4BITSEL	Interface Select	I	TTL	Selects between the serial interface and the 4-bit parallel interface. Only one interface can be used at any time.
LOOPTIMING	Internal Looptiming Enable	I	TTL	Enables looptiming from reference clock frequency of the receive data stream whether it is sourced from the recovered clock or the reference clock of the CRU.
CLKRSTEN	Clock Reset Enable	I	TTL	If CLKRSTEN is asserted, all primary clock outputs (TXRCLK, RXRCLK, RSPCLK1, RSPCLK2, RTOHCLK, TSPCLK1, TSPCLK2, and TTOHCLK) will halt during master reset. If CLKRSTEN is deasserted, all primary clock outputs will be running during device master reset.
RXRCLK	Receive Reference Clock	O	TTL	Reference clock derived from the receive line in a 78MHz/ 38MHz/19MHz/8kHz version.
TXRCLK	Transmit Reference Clock	O	TTL	Reference clock derived from transmit line in a 78MHz/ 38MHz/19MHz/8kHz version.

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Signal	*Name*	*I/O*	*Type*	*Description*
LOPC	Loss of Optical Carrier	I	TTL	LOPC is monitored and changes in the signal status may cause generation of an interrupt. This allows monitoring of optical failures via the device CPU interface. When LOPC is asserted, the receive processor is optionally clocked by the transmit clock (derived from TLCLK).
LOS	Loss Of Signal	O	TTL	Status signal indicating if Loss Of Signal (LOS) has been detected. The LOS status is also available in an internal status register bit. The signal is active high.
LOF	Loss Of Frame	O	TTL	Status signal indicating if Loss Of Frame (LOF) has been detected. The LOF status is also available in an internal status register bit. The signal is active high.
LCD-P	Loss of Cell Delineation	O	TTL	This signal is asserted when the cell delineation state machine is not in SYNC state. This alarm indication is also available via internal register access.
RSPFP	Receive Special Purpose Frame Pulse	O	TTL	Frame reference for special purpose serial output ports RSPDAT*x*. The frame pulse is a one clock cycle wide pulse coincident with the first bit on the serial data. Active high. RSPFP changes on the falling edge of RSPCLK*x*. *x* = [1,2].
RSPCLK1	Receive Special Purpose Clock 1	O	TTL	Clock reference for receive special purpose serial output port 1. The clock is a 2.16MHz, 50% duty-cycle signal (optionally gapped to match the bandwidth of RSPDAT1.
RSPDAT1	Receive Special Purpose Data 1	O	TTL	Data output for special purpose serial port 1. RSPDAT1 changes on the falling edge of RSPCLK1.
RSPVALID1	Receive Special Purpose Valid 1	O	TTL	Valid qualifier for special purpose serial port 1. RSPVALID1 is asserted (programmable level) when there is valid data on RSPDAT1. RSPVALID1 changes on the falling edge of RSPCLK1.
RSPCLK2	Receive Special Purpose Clock 2	O	TTL	Clock reference for receive special purpose serial output port 2. The clock is a 2.16MHz, 50% duty-cycle signal (optionally gapped to match the bandwidth of RSPDAT2.
RSPDAT2	Receive Special Purpose Data 2	O	TTL	Data output for special purpose serial port 2. RSPDAT2 changes on the falling edge of RSPCLK2.
RSPVALID2	Receive Special Purpose Valid 2	O	TTL	Valid qualifier for special purpose serial port 2. RSPVALID2 is asserted (programmable level) when there is valid data on RSPDAT2. RSPVALID2 changes on the falling edge of RSPCLK2.
RTOHCLK	Receive Transport Overhead Clock	O	TTL	Clock reference for the receive transport overhead port. The clock is a 38.88MHz, 50% duty-cycle signal.
RTOHVALID	Receive Transport Overhead Valid	O	TTL	Valid qualifier for the receive transport overhead port. RTOHVALID is asserted (programmable level) when there is valid data on RTOH[3..0]. RTOHVALID changes on the falling edge of RTOHCLK.

Signal	*Name*	*I/O*	*Type*	*Description*
RTOHFP	Receive Transport Overhead Frame Pulse	O	TTL	Frame reference for the receive transport overhead port. RTOHFP is a one clock cycle wide pulse coincident with the first bit(s) of the first A1 being output on RTOH[3..0]. RTOHFP changes on the falling edge of RTOHCLK.
RTOH[3..0]	Receive Transport Overhead Data	O	TTL	Data output for the receive transport overhead (section and line) bytes extracted from the incoming STS-48 signal. RTOH[3..0] changes on the falling edge of RTOHCLK. RTOH[3..0] carries the entire transport overhead in the order the overhead bytes are received. The most significant nibble (first received) is output first. RTOH[3] ismost significant bit.
TSPCLK1	Transmit Special Purpose Clock 1	O	TTL	Clock reference for the transmit special purpose serialport 1. The clock is a 2.16MHz, 50% duty-cycle signal (optionally gapped to match the bandwidth of TSPDAT1).
TSPFP1	Transmit Special Purpose Frame Pulse 1	O	TTL	Frame reference for the special purpose serial output port TSPDAT1. Mode 1 (TSPCLK1 continuous): The frame pulse is a one clock cycle wide pulse indicating the start of a new data stream on TSPDAT1. When TSPFP1 is asserted, the first bit of TSPDAT1 is sampled on the second rising edge thereafter. TSPFP1 changes on the falling edge of TSPCLK1. Mode 2 (TSPCLK1 gapped): The frame pulse is a one clock cycle wide pulse (variable width due to the gapped clock) indicating the start of a new data stream on TSPDAT1. When TSPFP1 is asserted, the first bit of TSPDAT1 is sampled on the second rising edge thereafter. TSPFP1 changes on the falling edge of TSPCLK1.
TSPREN1	Transmit Special Purpose Read Enable 1	O	TTL	Read enable signal for the TSPDAT1 data stream. The response latency from TSPREN1 is asserted until TSPDAT1 is sampled is programmable. TSPREN1 changes on the falling edge of TSPCLK1.
TSPDAT1	Transmit Special Purpose Data 1	I	TTL	Serial data input for transmit special purpose port 1. TSPDAT1 is sampled on the rising edge of TSPCLK1.
TSPCLK2	Transmit Special Purpose Clock 2	O	TTL	Clock reference for the transmit special purpose serialport 2. The clock is a 2.16MHz, 50% duty-cycle signal (optionally gapped to match the bandwidth of TSPDAT2).

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Signal	*Name*	*I/O*	*Type*	*Description*
TSPFP2	Transmit Special Purpose Frame Pulse 2	O	TTL	Frame reference for the special purpose serial output port TSPDAT2. Mode 1 (TSPCLK2 continuous): The frame pulse is a one clock cycle wide pulse indicating the start of a new data stream on TSPDAT2. When TSPFP2 is asserted, the first bit of TSPDAT2 is sampled on the second rising edge thereafter. TSPFP2 changes on the falling edge of TSPCLK2. Mode 2 (TSPCLK2 gapped): The frame pulse is a one clock cycle wide pulse (variable width due to the gapped clock) indicating the start of a new data stream on TSPDAT2. When TSPFP2 is asserted, the first bit of TSPDAT2 is sampled on the second rising edge thereafter. TSPFP2 changes on the falling edge of TSPCLK2.
TSPREN2	Transmit Special Purpose Read Enable 2	O	TTL	Read enable signal for the TSPDAT2 data stream. The response latency from TSPREN2 is asserted until TSPDAT2 is sampled is programmable. TSPREN2 changes on the falling edge of TSPCLK2.
TSPDAT2	Transmit Special Purpose Data 2	I	TTL	Serial data input for transmit special purpose port 2. TSPDAT2 is sampled on the rising edge of TSPCLK2.
TTOHCLK	Transmit Transport Overhead Clock	O	TTL	Clock reference for the transmit transport overhead port. The clock is a 38.88MHz, 50% duty-cycle signal.
TTOHFP	Transmit Transport Overhead Frame Pulse	O	TTL	Frame reference for the transmit transport overhead port. TTOHFP is a one clock cycle wide pulse indicating the start of a new data stream on TTOH[3..0]. The response latency from TTOHFP is asserted until the first bit on TTOH[3..0] is sampled is programmable (see TTOHREN). TTOHFP changes on the falling edge of TTOHCLK.
TTOHREN	Transmit Transport Overhead Read Enable	O	TTL	Read enable signal for the TTOH[3..0] data stream. The response latency from TTOHREN is asserted until TTOH[3..0] is sampled is programmable. TTOHREN changes on the falling edge of TTOHCLK.
TTOHEN	Transmit Transport Overhead Enable	I	TTL	Enable signal for the TTOH[3..0] data stream. If TTOHEN is asserted, the corresponding byte will be inserted in the corresponding transport overhead byte of the outgoing STS-48 data stream. Transport overhead for the entire STS-48 is input as 4-bit nibbles on the TTOH[3..0] port (see TTOH[3..0] description). If TTOHEN is asserted during the first nibble of an overhead byte, the corresponding overhead byte is enabled. Note: The transmit section and line processing blocks can selectively overwrite/modify overhead bytes inserted through the TTOH interface.

Signal	*Name*	*I/O*	*Type*	*Description*
TTOH[3..0]	Transmit Transport Ovehead Data	I	TTL	Data input for the transport overhead (section and line) bytes to be inserted in the outgoing STS-48 signal. TTOH[3..0] is sampled on the rising edge of TTOHCLK. TTOH[3..0] carries the entire STS-48 transport overhead in the order the overhead bytes are to be inserted. The most significant nibble (first received) is input first. TTOH[3] is the most significant bit.
D[7..0]	CPU Data	IO	TTL	Bidirectional data bus is used to transfer data for microcontroller read/write access to internal device registers.
A[8..0]	CPU Address	I	TTL	Address bus selects specific internal registers during register read/write access.
ALE	CPU Address Latch Enable	I	TTL	Controls internal latching of the address bus signals. When low the address bus A[8..0] is latched internal. When high the internal address bus latches are transparent. Thiswill allow for interfacing to a multiplexed address/data. The ALE signal has an internal pull-up resistor.
CSB	CPU Chip Select (active low)	I	TTL	Must always be asserted during register read/write access cycles. The CSB signal is used in conjunction with either the RDB or the WRB signal. The CSB signal has an internal pull-up resistor.
WRB	CPU Write Enable (active low)	I	TTL	Used for register write operations. The D[7..0] content is written into the by A[8..0] selected register when WRB and CSB are both asserted (low). The WRB signal has an internal pull-up resistor.
RDB	CPU Read Enable (active low)	I	TTL	Used for register read operations. The D[7..0] will driveregister content of the by A[8..0] selected register when RDB and CSB are both asserted (low). The RDB signal has an internal pull-up resistor.
INTB	CPU Interrupt (active low)	O	TTL	Asserted when an internal interrupt source is pending and the interrupt is unmasked (enabled). The INTB signal is deasserted when the interrupt pending bits have been cleared. The INTB is an open drain signal.
RSTB	Chip Reset (active low)	I	TTL	Asynchronous reset of the device. The device is held in a reset state while the RSTB signal is low. The signal istrigged with an internal pull-up resistor. All outputs are tristated when RSTB is asserted.
PMTICK	Performance Monitoring Tick	IO	TTL	Output. Asserted when the internal PMTICK timer generates a tick for latching performance counters in the device. Input: A low-to-high transition will (optionally) trigger latching of performance monitoring counters in the device.
GPIO[7..0]	General Purpose Input/Output	IO	TTL	Individually configurable as inputs or outputs. Intended for controlling monitoring external devices.

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Signal	*Name*	*I/O*	*Type*	*Description*
TDO	JTAG Test Data Output	O	TTL	This signal carries test data out of the device via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. The TDO signal is a tristate output which is inactive except when data scan shifting is in progress.
TDI	JTAG Test Data Input	I	TTL	The signal carries test data into the device via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an internal pull-up resistor.
TCK	JTAG Test Clock	I	TTL	This signal provides timing for test operations that are carried out using the IEEE P1149.1 test access port.
TMS	JTAG Test Mode Select	I	TTL	This signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an internal pull-up resistor.
TRSTB	JTAG Test Reset (active low)	I	TTL	This signal provides an asynchronous test access port reset via the IEEE P1149.1 test access port. TRSTB is a schmitt triggered input with an internal pull-up resistor.
OE	Chip Output Enable (active high)	I	TTL	When deasserted (set low), all TTL device outputs are tristated. The OE signal has an internal pull-up.
POS Mode only: RXTS	Rx FIFO SOP Word Write	O	TTL	*POS Mode only:* When enabled, the RXTS signal will be asserted for one RLCLK div 2 clock cycle period (nominally 77.76MHz) when the first word of a data structure (SOP) is written to the Rx FIFO. The RXTS signal shall be enabled via a register, but will be tristate by default.
POS Mode only: TXTS	Tx FIFO SOP Word Read	O	TTL	*POS Mode only:* When enabled, the TXTS signal will be asserted for one TLCLK div 2 clock cycle period (nominally 77.76MHz) when the first word of a data structure (SOP) is read out of the transmit FIFO. The TXTS signal is enabled via a register, but will be tristate by default.
POS Mode: TDAT[31..0] *ATM Mode:* TUDATA[31..0]	Transmit Packet Data Bus / UTOPIA Transmit Data Bus	I	TTL	*POS Mode:* Four-octet true data driven from Packet to PHY layer. TDAT[31] is MSB. Packets are aligned to 32 bit TDAT boundary. *ATM Mode:* Four-octet true data driven from ATM to PHY layer. TUDATA[31] is MSB.

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Signal	*Name*	*I/O*	*Type*	*Description*
POS Mode: TPRTY *ATM Mode:* TUPRTY	Transmit Bus Parity / UTOPIA Transmit Bus Parity	I	TTL	*POS Mode:* TPRTY is the odd/even (programmable, default odd) parity bit over TDAT[31..0]. The signal is only valid when asserted simultaneously with TENB. *ATM Mode:* TUPRTY is the odd/even (programmable, default odd) parity bit over TUDATA[31..0], driven by the ATM layer. The signal is only valid when asserted simultaneously with TUENB*.
POS Mode: TMOD[1..0]	Transmit Word Modulo	I	TTL	*POS Mode only:* Data Qualifier. Qualifer for the four TDAT bytes. Defines which of the four TDAT bytes contains valid data when TEOP and TENB are asserted. Non-EOP words always contains 4 valid TDAT bytes.
POS Mode: TSOP *ATM Mode:* TUSOC	Transmit Start Of Packet / UTOPIA Transmit Start Of Cell	I	TTL	*POS Mode:* Active high signal asserted by the packet layer when TDAT contains the first valid byte of the packet. The signal isvalid when asserted simultaneously with TENB. The packet interface can be operated without using this signal. *ATM Mode:* Start Of Cell. Active high signal asserted by the ATM layer when TUDATA contains the first valid byte of the cell. The signal is only valid when asserted simultaneously with TUENB*.
POS Mode: TEOP	Transmit End Of packet	I	TTL	*POS Mode only:* Is asserted by the packet layer when TDAT contains the last valid byte of the packet. The signal is only valid when asserted simultaneously with TENB. Active high signal.
POS Mode: DTPA *ATM Mode:* TUFULL*/ TUCLAV	Transmit Polled-PHY Packet Available / Transmit Full/Cell Available	O	TTL	*POS Mode:* DTPA transitions high when a programmable minimum number of bytes are available in the Tx FIFO. Once high, the DTPA indicates that the Tx FIFO is not full. WHEN DTPA transitions low, it optionally indicates that the Tx FIFO is full or near full. *ATM Mode:* For UTOPIA flow control. The TUFULL* definition applies to word level flow control, and TUCLAV definition applies to cell level flow control.

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Signal	*Name*	*I/O*	*Type*	*Description*
POS Mode: TERR	Transmit Error Indicator	I	TTL	*POS Mode only:* May be used to force HDLC frame abortion of insertion of FCS error in the transmitted HDLC/PPP frames. The TERR value is only relevant for the TEOP marked word, and ingored for all other word writes.
POS Mode: TENB *ATM Mode:* TUENB*	Transmit Write Enable / Transmit Write Enable	I	TTL	*POS Mode:* Active low signal asserted by the packet layer during cycles when TDAT contains valid packet data. *ATM Mode:* Active low signal asserted by the ATM layer during cycles when TUDATA contains valid cell data.
POS Mode: TFCLK *ATM Mode:* TUCLK	Transmit FIFO Write Clock / Transmit Write Clock	I	TTL	*POS Mode:* Transfer/synchronization clock provided by the packet layer to the PHY layer for synchronizing transfers on TDAT. *ATM Mode:* Transfer/synchronization clock provided by the ATM layer to the PHY layer for synchronizing transfers on TUDATA.
POS Mode: TFCLKO *ATM Mode:* TUCLKO	Transmit FIFO Write Clock Looped / Transmit Clock Looped	O	TTL	*POS Mode:* The TFCLK input looped back out. *ATM Mode:* The TUCLK input looped back out.
POS Mode: RDAT[31..0] *ATM Mode:* RUDATA[31..0]	Receive Packet Data Bus / Receive Cell Data Bus	O	TTL	*POS Mode:* Four-octet true data driven from PHY to packet layer. RDAT[31] is MSB. Packets are aligned to 32 bit RDAT boundary. *ATM Mode:* Four-octet wide data driven from PHY to ATM layer. RUDATA[31] is the MSB.
POS Mode: RPRTY *ATM Mode:* RUPRTY	Receive Bus Parity / Receive Bus Parity	O	TTL	*POS Mode:* RXPRTY is the odd/even (programmable, default odd) parity bit over RDAT[31..0]. *ATM Mode:* RUPRTY is the odd/even (programmable, default odd) parity for RUDATA[31..0].

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Signal	***Name***	***I/O***	***Type***	***Description***
POS Mode: RMOD[1..0]	Receive Word Module	O	TTL	*POS Mode only:* Data Qualifier. Qualifer for the four RDAT bytes. Defines which of the four RDAT bytes contains valid data. This signal is ignored when REOP is not asserted.
POS Mode: RSOP *ATM Mode:* RUSOC	Receive Start Of Packet / Receive Start Of Cell	O	TTL	*POS Mode:* Start Of Packet. Is asserted when RDAT contains the first valid byte of the packet. Active high signal. The interface can be operated without using this signal. *ATM Mode:* Active high signal asserted by the PHY layer when RUDATA contains the first valid byte of a cell. To support multiple PHY configurations.
POS Mode: REOP	Receive End Of Packet	O	TTL	*POS Mode only:* End Of Packet. Is asserted when RDAT contains the last valid byte of the packet. Active high signal.
POS Mode: RVAL *ATM Mode:* RUEMPTY*/ RUCLAV	Receive Data Valid / Receive Empty/ Cell Available.	O	TTL	*POS Mode:* RVAL indicates the validity of the receive data signals. When RVAL is high, the receive signals (RDAT, RSOP, REOP, RMOD, RXPRTY and RERR) are valid. When RVAL is low, all receive signals are invalid and must be disregarded. RVAL will transition low on a FIFO empty condition or on an end of packet. No data will be removed from the receive FIFO while RVAL is deasserted. Once deasserted, RVAL will remain deasserted until current PHY has been deselected. *ATM Mode:* For UTOPIA flow control. The RUEMPTY* definition applies to word level flow control, and RUCLAV definition applies to cell level flow control.
POS Mode: RERR	Receive Error Indicator	O	TTL	*POS Mode only:* Indicates if the packet contained an error (e.g. Abort/FCS error). This is an active high signal which is asserted during an EOP word.

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Signal	*Name*	*I/O*	*Type*	*Description*
POS Mode: RENB *ATM Mode:* RUENB	Receive Read Enable / UTOPIA Read Enable	I	TTL	*POS Mode:* Active low signal asserted by the packet layer to indicate that RVAL, RSOP, RPRTY, RDAT[31..0], RMOD[1..0], REOP, and RERR output signals will be sampled at the end of the next cycle. *ATM Mode:* Active low signal asserted by the ATM layer to indicate that RUDATA, RUSOC and RPRTY will be sampled at the end of the next cycle.
POS Mode: RFCLK *ATM Mode:* RUCLK	Receive FIFO Write Clock / Receive Clock	I	TTL	*POS Mode:* Clock. Transfer/synchronization clock provided by the packet layer to the PHY layer for synchronizing transfers on RDAT. *ATM Mode:* Clock. Transfer/synchronization clock provided by the ATM layer to the PHY layer for synchronizing transfers on RUDATA.
POS Mode: RFCLKO *ATM Mode:* RUCLKO	Receive FIFO Write Clock Looped / Receive Clock Looped	O	TTL	*POS Mode:* Looped clock. The RXCLK input looped back out. *ATM Mode:* The RUCLK looped back out.

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Package Pin List

BGA Pin	Signal Name	BGA Pin	Signal Name	BGA Pin	Signal Name
A1	GND	A2	GND	A3	TDAT[20]
A4	TDAT[25]	A5	GND	A6	TDAT[30]
A7	TMOD[1]	A8	GND	A9	DTPA
A10	TFCLK	A11	GND	A12	TTOHREN
A13	TSPFP1	A14	GND	A15	TSPDAT1
A16	TSPCLK1	A17	GND	A18	RTOHFP
A19	RSPCLK1	A20	GND	A21	RTOH[0]
A22	VSSOR	A23	GND	A24	GND
B1	GND	B2	GND	B3	TDAT[19]
B4	TDAT[22]	B5	TDAT[27]	B6	TDAT[28]
B7	TMOD[0]	B8	VDD33	B9	TERR
B10	TFCLKO	B11	TSPREN2	B12	TSPFP2
B13	TSPCLK2	B14	VDD33	B15	TSPREN1
B16	RTOHCLK	B17	RSPVALID2	B18	RSPCLK2
B19	RTOHVALID	B20	RTOH[2]	B21	TXRCLK
B22	VSSIR	B23	GND	B24	GND
C1	TDAT[16]	C2	TDAT[17]	C3	VDD33
C4	TDAT[21]	C5	TDAT[24]	C6	TDAT[26]
C7	TDAT[29]	C8	TPRTY	C9	TSOP
C10	TENB	C11	NC_1	C12	TTOHFP
C13	TTOHCLK	C14	TTOHEN	C15	TTOH[3]
C16	TTOH[1]	C17	RSPDAT2	C18	RSPFP
C19	RTOH[3]	C20	RSPVALID1	C21	VDDOR
C22	RLPRTY4-	C23	RLPRTY4+	C24	RLCLK4+
D1	TDAT[12]	D2	TDAT[13]	D3	TDAT[14]
D4	VDD	D5	TDAT[18]	D6	TDAT[23]
D7	VDD	D8	VDD33	D9	TDAT[31]
D10	TEOP	D11	VDD	D12	NC_2
D13	TSPDAT2	D14	VDD	D15	TTOH[2]

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BGA Pin	*Signal Name*	*BGA Pin*	*Signal Name*	*BGA Pin*	*Signal Name*
D16	TTOH[0]	D17	VDD33	D18	VDD
D19	RTOH[1]	D20	RSPDAT1	D21	VDD33
D22	RLIN4[0]-	D23	RLIN4[1]+	D24	RLCLK4-
E1	GND	E2	TDAT[9]	E3	TDAT[10]
E4	TDAT[15]	E21	RLIN4[0]+	E22	RLIN4[1]-
E23	RLIN4[3]-	E24	GND	F1	TDAT[6]
F2	TDAT[7]	F3	TDAT[8]	F4	TDAT[11]
F21	RLIN4[2]-	F22	RLIN4[2]+	F23	RLIN4[3]+
F24	RLINSER-	G1	TDAT[3]	G2	TDAT[4]
G3	TDAT[5]	G4	VDD	G21	VDDIR
G22	VDDOR	G23	VSSOR	G24	RLINSER+
H1	GND	H2	VDD33	H3	TDAT[2]
H4	VDD33	H21	VSSOA_DEMUX	H22	VDDOA_DEMUX
H23	RLINSERCNTR	H24	GND	J1	RDAT[30]
J2	RDAT[31]	J3	TDAT[0]	J4	TDAT[1]
J21	CRUREFCLK-	J22	CRUREFCLK+	J23	VSSOA_CRU
J24	CRURECCLK+	K1	RDAT[26]	K2	RDAT[27]
K3	RDAT[28]	K4	RDAT[29]	K21	GND
K22	CRUFILTER+	K23	VDDOA_CRU	K24	CRURECCLK-
L1	GND	L2	RDAT[24]	L3	RDAT[25]
L4	VDD	L21	CMUFILTER+	L22	CMUFILTER-
L23	CRUFILTER-	L24	VSSOA_CMU	M1	RDAT[23]
M2	RDAT[22]	M3	RDAT[20]	M4	RDAT[21]
M21	VDDOA_CMU	M22	VSSOA_DATA	M23	CMUREFCLK+
M24	TLOUTSER+	N1	RDAT[16]	N2	RDAT[19]
N3	RDAT[18]	N4	RDAT[17]	N21	VDDOA_DATA
N22	VSSOA_CLK	N23	CMUREFCLK-	N24	TLOUTSER-
P1	GND	P2	RDAT[15]	P3	RDAT[14]
P4	VDD	P21	VDDOA_CLK	P22	VDDOA_MUX

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BGA Pin	Signal Name	BGA Pin	Signal Name	BGA Pin	Signal Name
P23	GND	P24	TLCLKSER+	R1	RDAT[13]
R2	RDAT[12]	R3	RDAT[11]	R4	RDAT[10]
R21	VSSOA_MUX	R22	VSSOT	R23	VDDOT
R24	TLCLKSER-	T1	RDAT[9]	T2	RDAT[8]
T3	RDAT[7]	T4	RDAT[6]	T21	TLSYNCLVDS+
T22	TLSYNCLVDS-	T23	VDDIT	T24	TLCLK4-
U1	GND	U2	RDAT[5]	U3	RDAT[4]
U4	VDD33	U21	GND	U22	TLPRTY4+
U23	TLPRTY4-	U24	TLCLK4+	V1	RDAT[3]
V2	RDAT[2]	V3	RDAT[1]	V4	VDD
V21	VSSOT	V22	TLOUT4[0]+	V23	TLOUT4[0]-
V24	TLOUT4[1]-	W1	RDAT[0]	W2	RMOD[1]
W3	RMOD[0]	W4	RERR	W21	TLOUT4[2]+
W22	VDDOT	W23	TLOUT4[1]+	W24	TLCLKOUT4+
Y1	GND	Y2	VDD33	Y3	RPRTY
Y4	RFCLK	Y21	VSSOT	Y22	TLOUT4[2]-
Y23	GND	Y24	TLCLKOUT4-	AA1	RSOP
AA2	RVAL	AA3	RENB	AA4	RFCLKO
AA5	NC_0	AA6	TXTS	AA7	VDD
AA8	VDD33	AA9	INTB	AA10	A[2]
AA11	VDD	AA12	ALE	AA13	LOF
AA14	VDD	AA15	CRUREFSEL[0]	AA16	CMUREFSEL[0]
AA17	VDD33	AA18	VDD	AA19	GPIO[2]
AA20	GPIO[0]	AA21	VDD33	AA22	VSSIT
AA23	TLOUT4[3]+	AA24	TLOUT4[3]-	AB1	VDD
AB2	REOP	AB3	VDD33	AB4	LCD-P
AB5	LOS	AB6	D[0]	AB7	D[3]
AB8	RDB	AB9	A[0]	AB10	WRB
AB11	A[6]	AB12	PMTICK	AB13	A[8]
AB14	SELLINE4	AB15	CRUREFSEL[1]	AB16	CMUREFSEL[1]

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BGA Pin	*Signal Name*	*BGA Pin*	*Signal Name*	*BGA Pin*	*Signal Name*
AB17	CMUCLKDIV	AB18	GPIO[7]	AB19	GPIO[4]
AB20	GPIO[1]	AB21	TCK	AB22	VDDOT
AB23	TLSYNCTTL	AB24	TRSTB	AC1	GND
AC2	GND	AC3	RXTS	AC4	D[1]
AC5	D[4]	AC6	D[5]	AC7	D[7]
AC8	VDD33	AC9	A[3]	AC10	A[5]
AC11	A[7]	AC12	CLKRSTEN	AC13	LOPC
AC14	VDD33	AC15	CRULOCKDET	AC16	CMULOCKDET
AC17	CMUREFDET	AC18	CMUCRUBYPASS	AC19	GPIO[5]
AC20	GPIO[3]	AC21	TDO	AC22	TMS
AC23	GND	AC24	GND	AD1	GND
AD2	GND	AD3	RSTB	AD4	D[2]
AD5	GND	AD6	D[6]	AD7	A[1]
AD8	GND	AD9	A[4]	AD10	CSB
AD11	GND	AD12	RXRCLK	AD13	COREBYPASS
AD14	GND	AD15	CRUREFDET	AD16	CRUCLKDIVREFSEL
AD17	GND	AD18	LOOPTIMING	AD19	GPIO[6]
AD20	GND	AD21	OE	AD22	TDI
AD23	GND	AD24	GND		

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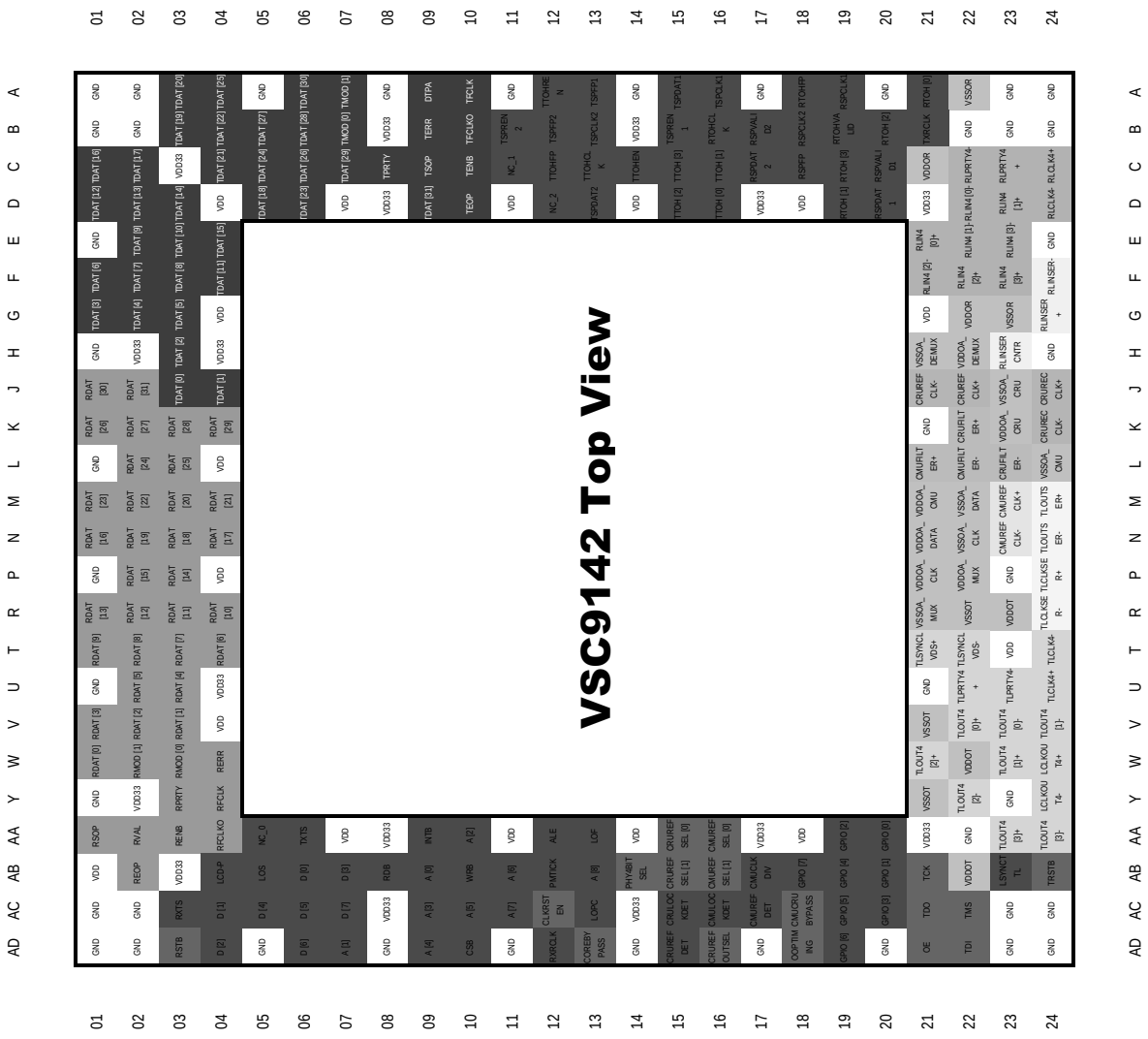
Package Pin Layout

Figure 11: Top View Pin Layout



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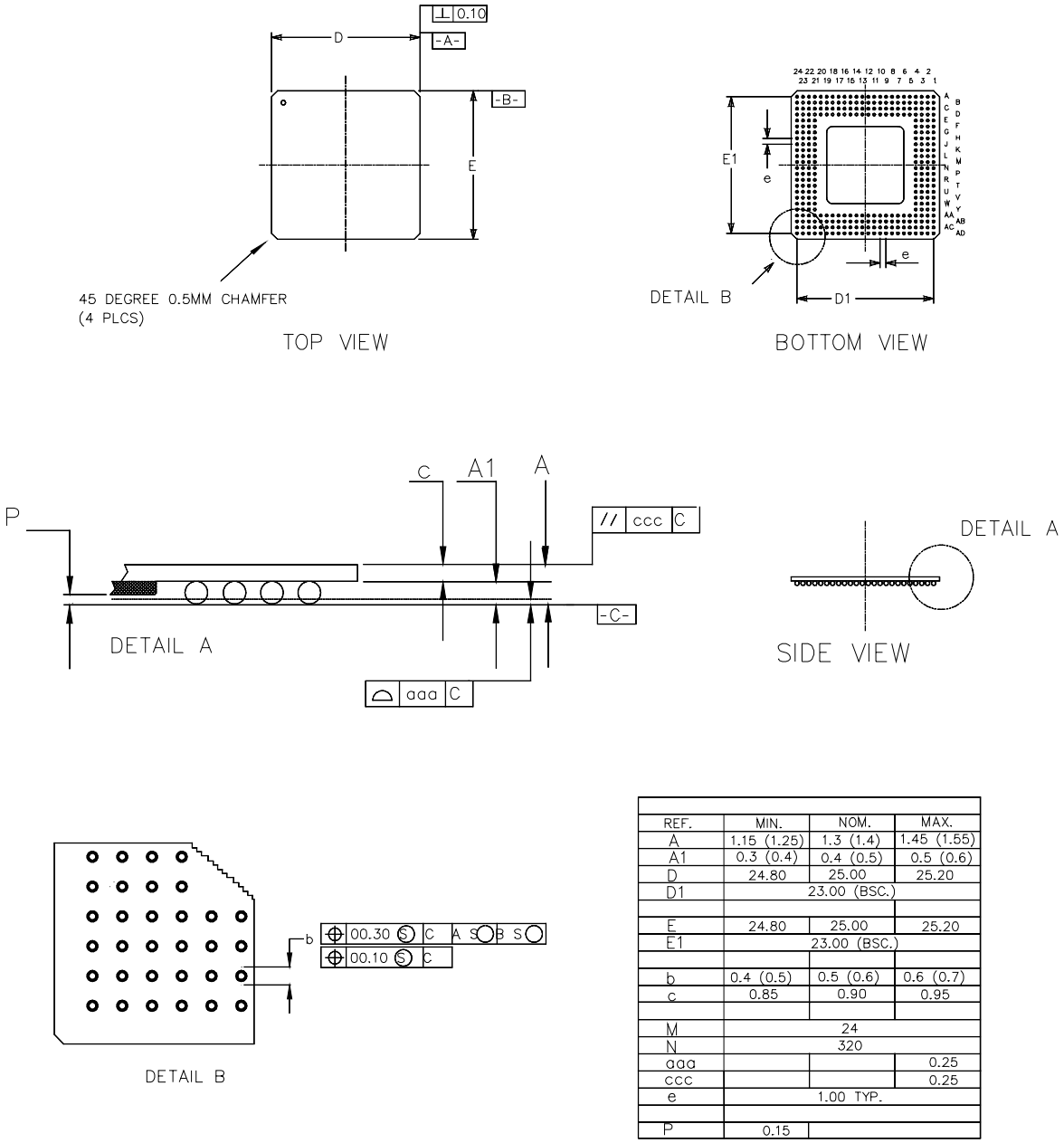
Package Information

Figure 12: 320-pin TBGA



REF.	MIN.	NOM.	MAX.
A	1.15 (1.25)	1.3 (1.4)	1.45 (1.55)
A1	0.3 (0.4)	0.4 (0.5)	0.5 (0.6)
D	24.80	25.00	25.20
D1	23.00 (BSC.)		
E	24.80	25.00	25.20
E1	23.00 (BSC.)		
b	0.4 (0.5)	0.5 (0.6)	0.6 (0.7)
c	0.85	0.90	0.95
M	24		
N	320		
aaa			0.25
ccc			0.25
e	1.00 TYP.		
P	0.15		

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Package Thermal Characteristics

Parameter	*Description*	*(Typ)*	*Units*
Th_{JA}	Theta J/A in Still Air	12.0	C/W
Th_{JA200}	Theta J/A at 200 LFPM	10.0	C/W
Th_{JC}	Theta J/C	0.22	C/W

Ordering Information

The ordering number for this product is formed by a combination of the device number and package type.

VSC9142 UK

Device Type
VSC9142 - 2.5Gb/s POS/ATM Framer with Integrated Mux/Demux and Clock and Data Recovery

Package Type
UK - 320-pin TBGA

Notice

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