# INTEGRATING CONVERTER ANALOG PROCESSORS

## FEATURES

- **Resolution ..... Up to 16 Bits + Sign (TC500A)**
- **Differential Analog Input**
- **Differential Reference**
- **Low Linearity Error ..... 0.003%**
- **Fast Zero-Crossing Comparator ..... 4 µs**
- **Low Power Dissipation ..... 10 mW**
- **Auto-Zero Cycle Eliminates Zero-Scale Error and Drift**
- **Zero Integrator Phase Speeds Recovery From Overrange Input Signals**
- **Automatic Internal Polarity Detection**
- **Low Input Current ..... 15 pA Max**
- **Wide Analog Input Voltage ..... ±4.2V**
- **Microprocessor Control of Dual-Slope ADC Conversion**

## IMPROVED PERFORMANCE

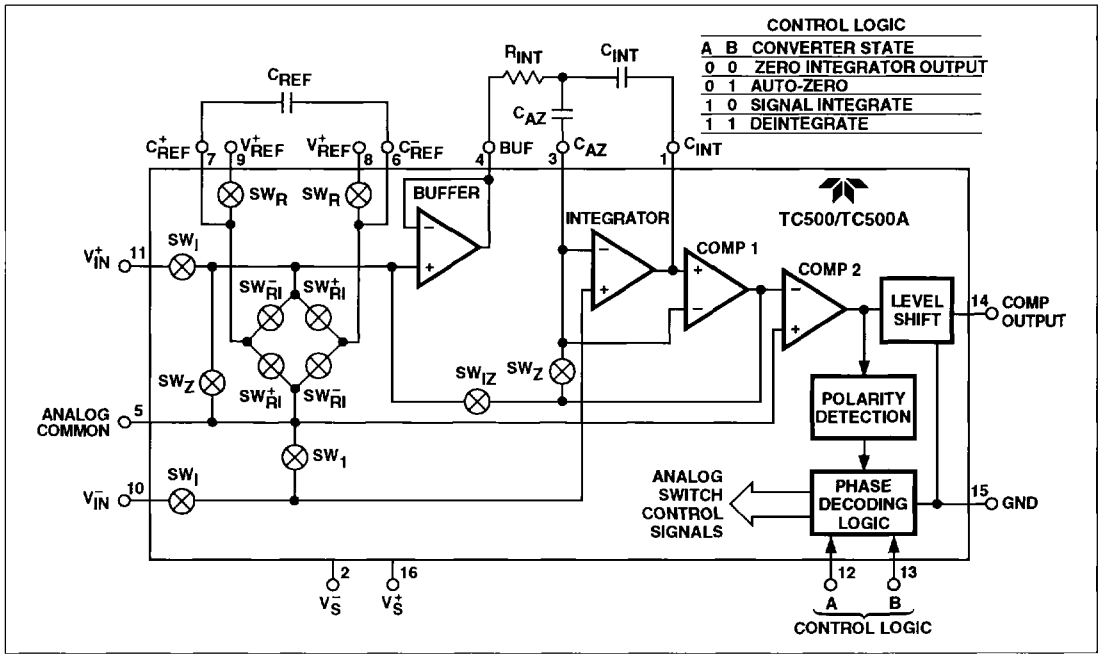
The TC500A is an improved version of the popular TC500. The improvements allow up to 16 bits of resolution (plus sign) or faster conversion times for lower resolution applications.

## GENERAL DESCRIPTION

The CMOS TC500/TC500A contain all the analog circuits needed to construct an integrating analog-to-digital converter. The analog input buffer, integrator, analog switches, comparator and phase control logic are all on chip.

The dual-slope converter uses time to quantize the analog input signal. A microprocessor and software routine perform the digital function of "counting clocks" for the dual-slope integrating converter process. The user can control resolution and conversion speed through software. The TC500/TC500A analog building block can be used to construct a fast or high-resolution converter by modifying software routines.

## FUNCTIONAL DIAGRAM



# TC500
# TC500A

A microprocessor controls the TC500/TC500A through the A and B logic input signals. Four phases are possible: auto-zero, signal integrate, reference integrate (deintegrate), and integrator zero output.

The TC500/TC500A comparator's output provides polarity and integrator zero-crossing information. The comparator output is always low when the integrator crosses zero during the deintegrate phase. This signals the end of a conversion to the processor.

A precision, dual-slope integrating converter with automatic zero-scale offset voltage and drift correction requires only a reference, three capacitors, a resistor and a controller. The TC500/TC500A contain the analog circuits needed to construct a dual-slope integrating converter with an auto-zero phase. A zero-integrator output phase can be selected to eliminate errors caused by out-of-range input signals. The zero-integrator phase greatly improves recovery after an overrange conversion.

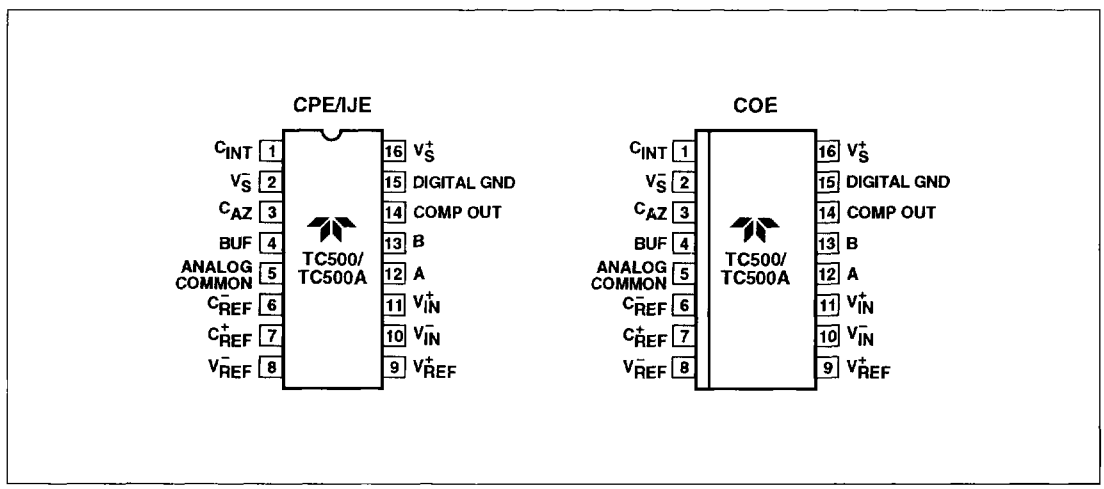
The CMOS TC500/TC500A operate from ±5V supplies. Power dissipation is only 10 mW. Leakage currents at the differential inputs are a low 10 pA. The TC500/TC500A differential reference inputs allow easy ratiometric measurements.

Although the TC500A is pin-for-pin compatible with the TC500, some programming constraints are imposed. (See "Integrator Output Zero.")

## ORDERING INFORMATION

| Part No. | Package | Temperature Range | System Resolution |
|---|---|---|---|
| TC500ACPE | 16-Pin Plastic DIP | 0°C to +70°C | 16-Bit (30 ppm) |
| TC500AIJE | 16-Pin CerDIP | –25°C to +85°C | 16-Bit (30 ppm) |
| TC500ACOE | 16-Pin SO | 0°C to +70°C | 16-Bit (30 ppm) |
| TC500CPE | 16-Pin Plastic DIP | 0°C to +70°C | 4-1/2 Digits (50 ppm) |
| TC500IJE | 16-Pin CerDIP | –25°C to +85°C | 4-1/2 Digits (50 ppm) |
| TC500COE | 16-Pin SO | 0°C to +70°C | 4-1/2 Digits (50 ppm) |

## PIN CONFIGURATIONS



## ABSOLUTE MAXIMUM RATINGS

Supply ($V_S^+$ to $V_S^-$) ..... +18V
Positive Supply Voltage ($V_S^+$ to GND) ..... +12V
Negative Supply Voltage ($V_S^-$ to GND) ..... −12V
Analog Input Voltage ($V_{IN}^+$ or $V_{IN}^-$) ..... $V_S^+$ to $V_S^-$
Logic Input Voltage ..... $V_S^+$ +0.3V to GND −0.3V
Package Power Dissipation ..... 0.5W
Ambient Operating Temperature Range
Plastic Package (C) ..... 0°C to +70°C
CerDIP Package (I) ..... −25°C to +85°C

Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

## ELECTRICAL CHARACTERISTICS: $T_A$ = +25°C, $V_S$ = ±5V, unless otherwise specified. $C_{AZ}$ = $C_{REF}$ = 0.1 µF.

| | | | TC500 | | | TC500A | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Test Conditions** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| **Analog** | | | | | | | | | |
| | Resolution | Note 1 | — | — | 50 | — | — | 30 | ppm |
| ZSE | Zero-Scale Error | Note 1 | — | — | 0.005 | — | — | 0.003 | % |
| ENL | End Point Linearity | Note 1 | — | 0.005 | 0.01 | — | 0.005 | 0.01 | % |
| NL | Best Case Straight Line Linearity | Notes 1 and 2 | — | — | 0.005 | — | — | 0.003 | % |
| DNL | Differential Nonlinearity | | — | — | 0.0025 | — | — | 0.0025 | % |
| $TC_{ZS}$ | Zero-Scale Temperature Coefficient | Over Operating Temperature Range | — | 1 | 2 | — | 1 | 2 | µV/°C |
| SYE | Full-Scale Symmetry Error (Roll-Over Error) | | — | — | 0.01 | — | — | 0.006 | % |
| | Ratiometric Reading | $V_{IN} = V_{REF}$ = 1V | — | — | 0.035 | — | — | 0.035 | % |
| $FS_{TC}$ | Full-Scale Temperature Coefficient | Over Operating Temperature Range External Reference TC = 0 ppm/°C | — | — | 10 | — | — | 10 | ppm/°C |
| $I_{IN}$ | Input Current | $V_{IN}$ = 0V | — | 6 | 15 | — | 6 | 15 | pA |
| CMRR | Common-Mode Rejection Ratio | $-1V \leq V_{CM} \leq 1V$ | — | 80 | — | — | 80 | — | dB |
| $V_{CMR}$ | Common-Mode Voltage Range | $V_S$ = ±5V | $V_S^-$ +1.5 | — | $V_S^+$ −1.5 | $V_S^-$ +1.5 | — | $V_S^+$ −1.5 | V |
| | Integrator Output Swing | $V_S$ = ±5V | — | — | ±4.1 | — | — | ±4.1 | V |
| | Analog Input Signal Range | | $V_S^-$ +0.8 | — | $V_S^+$ −0.8 | $V_S^-$ +0.8 | — | $V_S^+$ −0.8 | V |
| $e_N$ | Noise | $V_{IN}$ = 0V | — | 30 | — | — | 30 | — | $\mu V_{P-P}$ |
| **Digital** | | | | | | | | | |
| | Reference Input Signal Range | | $V_S^-$ +1 | — | $V_S^+$ −1 | $V_S^-$ +1 | — | $V_S^+$ −1 | V |
| $V_{OH}$ | Comparator Logic 1, Output High | $I_{SOURCE}$ = 800 µA | 4 | — | — | 4 | — | — | V |
| $V_{OL}$ | Comparator Logic 0, Output Low | $I_{SINK}$ = 4 mA | — | — | 0.4 | — | — | 0.4 | V |
| $V_{IH}$ | Logic 1, Input High Voltage | | 3.5 | — | — | 3.5 | — | — | V |
| $V_{IL}$ | Logic 0, Input Low Voltage | | — | — | 1 | — | — | 1 | V |
| $I_L$ | Logic Input Current | Logic 1 or 0 | — | 0.05 | — | — | 0.05 | — | µA |
| $t_D$ | Comparator Delay | | — | 4 | — | — | 4 | — | µs |

# TC500
# TC500A

## ELECTRICAL CHARACTERISTICS (Cont.)

| Symbol | Parameter | Test Conditions | TC500 Min | TC500 Typ | TC500 Max | TC500A Min | TC500A Typ | TC500A Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| **Power** | | | | | | | | | |
| $I_S$ | Supply Current | $V_S = \pm5V$, A = 1, B = 1 | — | 1 | 1.5 | — | 1 | 1.5 | mA |
| $P_D$ | Power Dissipation | $V_S = \pm5V$ | — | — | 15 | — | — | 15 | mW |
| $V_S^+$ | Positive Supply Operating Voltage Range | | 4 | — | 10 | 4 | — | 10 | V |
| $V_S^-$ | Negative Supply Operating Voltage Range | | −3 | — | −8 | −3 | — | −8 | V |
| $V_S^+ - V_S^-$ | Supply Operating Voltage Range | | 7 | — | 15 | 7 | — | 15 | V |

**NOTES:** 1. Integrate time ≥200 ms, auto-zero time ≥100 ms, $V_{INT}$ (peak) ≈ 4V.
2. End point linearity at ±1/4, ±1/2, ±3/4 FS after full-scale adjustment.

## OPERATIONAL THEORY

The TC500 and TC500A are dual-slope, integrating analog processors which are used with a microprocessor to generate analog-to-digital conversions of up to 16 bits of resolution. Although the TC500 and TC500A are virtually the same, the TC500A is recommended for applications requiring more than 14 bits of resolution.

The TC500 and TC500A incorporate a system zero phase and integrator output voltage zero phase, in addition to the normal two-phase, dual-slope measurement cycle. Reduced system errors, fewer calibration steps, and shorter overrange recovery time result.

The TC500 and TC500A measurement cycle can use all four phases, if desired.

(1) Auto zero

(2) Analog input signal integration

(3) Reference voltage integration (deintegrate)

(4) Integrator output zero

Internal analog gate status is shown in Table I for each phase (see the functional diagram).

### Auto-Zero Phase

During this phase, errors due to buffer, integrator and comparator offset voltages are compensated for by charging $C_{AZ}$ (auto-zero capacitor) with a compensating error voltage.

The external input signal is disconnected from the internal circuitry by opening the two $SW_I$ switches. The internal input points connect to analog common. The reference capacitor charges to the reference voltage potential through $SW_R$. A feedback loop, closed around the integrator and comparator, charges the $C_{AZ}$ capacitor with a voltage to compensate for buffer amplifier, integrator and comparator offset voltages.

### Analog Input Signal Integration Phase

The TC500/TC500A integrate the differential voltage between the (+) and (–) inputs. The differential voltage must be within the device's common-mode range.

The input signal polarity is normally checked via software at the end of this phase.

**Table I. Internal Analog Gate Status**

| | Internal Analog Gate Status | | | | | | |
|---|---|---|---|---|---|---|---|
| **Conversion Phase** | **$SW_I$** | **$SW_{RI}^+$** | **$SW_{RI}^-$** | **$SW_Z$** | **$SW_R$** | **$SW_1$** | **$SW_{IZ}$** |
| Auto-Zero (A=0, B=1) | | | | Closed | Closed | Closed | |
| Input Signal Integration | Closed | | | | | | |
| (A=1, B=0) | | | | | | | |
| Reference Voltage | | Closed* | | | | Closed | |
| Deintegration (A=1, B=1) | | | | | | | |
| Integrator Output Zero | | | | | Closed | Closed | Closed |
| (A=0, B=0) | | | | | | | |

*Assumes a positive polarity input signal. $SW_{RI}^-$ would be closed for a negative input signal.

### Reference Voltage Deintegration Phase

The previously charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero.

### Integrator Output Zero Phase

This phase guarantees the integrator output is at 0V when the system zero phase is entered and that the true system offset voltages are compensated. This phase is used at the end of the reference voltage deintegration (DEINT) phase and SHOULD be used for all TC500/TC500A applications. This phase MUST be used for resolutions of more than 14 bits. If this phase is not used, the value of the auto-zero capacitor ($C_{AZ}$) must be about 23 the value of the integration capacitor ($C_{INT}$) to reduce the effects of charge-sharing. The integrator output zero phase should be programmed to operate until the output of the comparator returns "high" (1) or for fixed time of about 2 ms.

## ANALOG SECTION

### Differential Inputs ($V_{IN}^+$ [Pin 11], $V_{IN}^-$ [Pin 10])

The TC500/TC500A operate with differential voltages within the input amplifier common-mode range. The input amplifier common-mode range extends from 0.8V below positive supply to 0.8V above negative supply. Within this common-mode voltage range, a common-mode rejection is typically 80 dB. Full accuracy is maintained, however, when the inputs are no less than 1.5V from either supply.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst-case condition exists, for example, when a large, positive common-mode voltage with a near full-scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications, the integrator swing can be reduced. The integrator output can swing within 0.9V of either supply without loss of linearity.

### Analog Common (Pin 5)

Analog common is used as $V_{IN}$ return during system-zero and reference deintegrate. If $V_{IN}^-$ is different from analog common, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications, $V_{IN}^-$ will be set at a fixed known voltage (i.e., power supply common). A common-mode voltage will exist when $V_{IN}^-$ is not connected to analog common.

### Differential Reference ($V_{REF}^+$ [Pin 9], $V_{REF}^-$ [Pin 8])

The reference voltage can be generated anywhere within 1V of the power supply voltage of the converter. Roll-over error is caused by the reference capacitor losing or gaining charge due to stray capacitance on its nodes. The difference in reference for (+) or (–) input voltages will cause a roll-over error. This error can be minimized by using a large reference capacitor in comparison to the stray capacitance.

### Phase Control Inputs (A [Pin 12], B [Pin 13])

The A, B unlatched logic inputs select the TC500/TC500A operating phase. The A, B inputs are normally driven by a microprocessor I/O port or peripheral I/O chip.

### Comparator Output

By monitoring the comparator output during the fixed-signal integrate time, the input signal polarity can be determined by the microprocessor controlling the conversion. The comparator output is high for positive signals and low for negative signals during the signal-integrate phase.

During the reference deintegrate phase, the comparator output will make a high-to-low transition as the integrator output ramp crosses zero. The transition is used to signal the processor that the conversion is complete.

The internal comparator delay is 4 µs, typically.

Figure 1 shows the comparator output for large positive and negative signal inputs. For signal inputs at or near zero volts, however, the integrator swing is nonexistent. If common-mode noise is present, the comparator can switch several times during the signal-integrate period. To ensure that the polarity reading is correct, the comparator output should be read and stored at the end of signal integrate.

A "low" (0) on the TC500/TC500A comparator, during the deintegrate phase, signals the processor that the conversion is complete.

The comparator output is undefined during the auto-zero and the integrator output zero phases.

## GENERAL THEORY OF OPERATION

### Dual-Slope Conversion Principles

The TC500 is an integrating analog-to-digital converter building block. An understanding of the dual-slope conversion technique will aid in following the detailed TC500A operation theory.

The conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input signal integration

(2) Reference voltage integration (deintegration)

## TC500
## TC500A

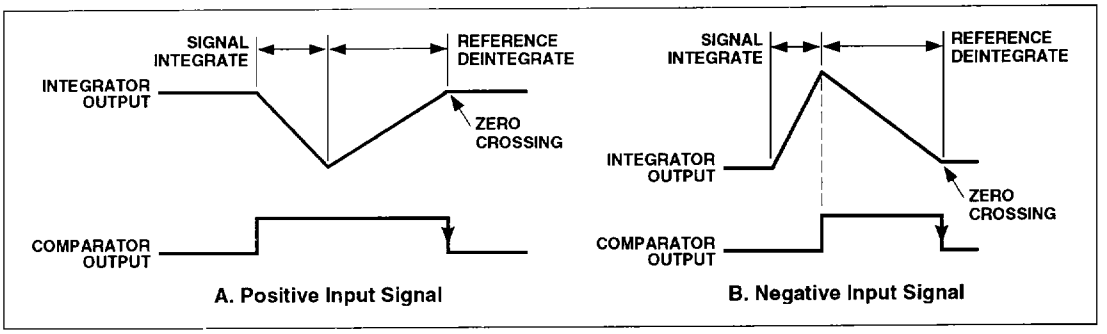



**Figure 1. Comparator Output**

The input signal being converted is integrated for a fixed time period, measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The TC500/TC500A automatically switch in the proper polarity reference signal. The reference integration time is directly proportional to the input signal (Figure 2).

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down." The TC500/TC500A comparator zero-crossing signals the processor to indicate the deintegrate cycle is complete.

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{R_{INT}\,C_{INT}}\int_0^{t_{INT}} V_{IN}\,(t)\,dt = \frac{V_{REF}\,t_{DEINT}}{R_{INT}\,C_{INT}}$$

where:

$V_{REF}$ = Reference voltage
$t_{INT}$ = Signal integration time (fixed)
$t_{DEINT}$ = reference voltage integration time (variable)

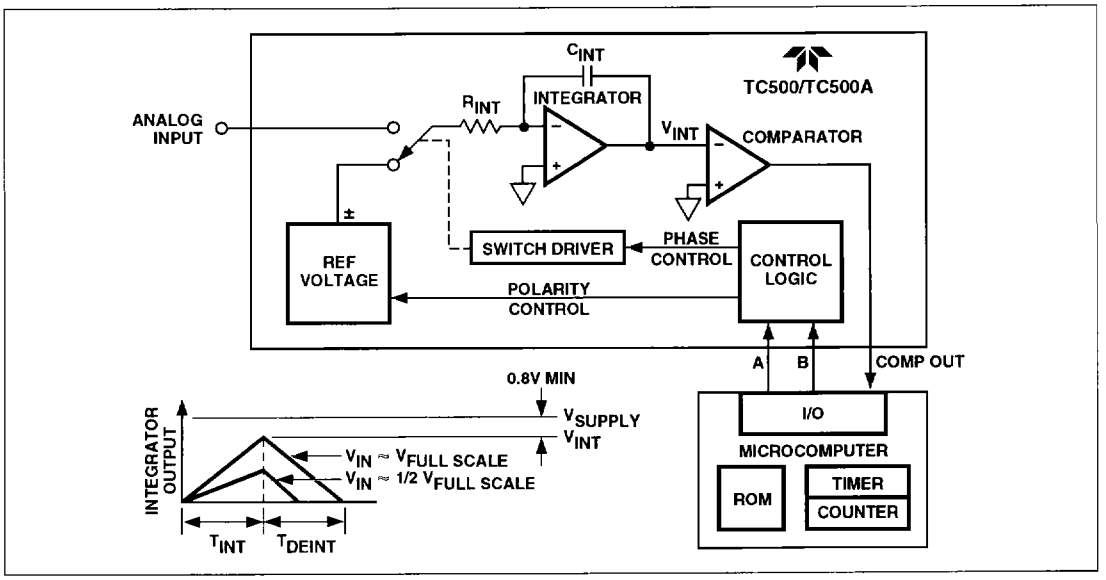



**Figure 2. Basic Dual-Slope Converter**

For a constant $V_{IN}$:

$$V_{IN} = V_{REF} \frac{t_{DEINT}}{t_{INT}}$$

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle.

An inherent benefit is noise immunity. Input noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague succesive approximation converters in high-noise environments.

Integrating converters provide noise rejection automatically with at least a 20-dB/decade attenuation rate. Interference signals with frequencies at integral multiples of the integration period are, theoretically, completely removed. This intuitively makes sense, since the average value of a sine wave of frequency (1/t) averaged over a period (t) is zero.

Integrating converters often establish the integration period to reject 50/60 Hz line frequency interference signals. The ability to reject such signals is shown by a normal mode rejection plot (Figure 3). Normal mode rejection is practically set to 50 to 65 dB, since the line frequency can deviate by a few tenths of a percent (Figure 4).

### Criteria for $C_{AZ}$ and $C_{REF}$

$$C_{AZ} \approx C_{REF} \approx \frac{2^N t_{INT} (V_{INT} + V_{REF}) I_{LEAKAGE}}{V_{INT} V_{REF}}$$

where:

N = resolution (bits)

$I_{LEAKAGE} \approx 15$ pA

$V_{INT}$ (see Figure 2)

This equation is for reference only. Use 0.1 µF capacitor for all applications that have 8 or more conversions per second. Use a 0.22 µF capacitor for 3 to 7 conversions per second, and a 0.47 µF capacitor for 2 or less conversions per second.

## COMPONENT VALUE SELECTION

### Integrating Resistor ($R_{INT}$)

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal class A output stage amplifiers will supply a 20-µA drive current with minimal linearity error. $R_{INT}$ is easily calculated for a 20-µA full-scale current:

$$R_{INT}\ (M\Omega) = \frac{\text{Full-Scale Input Voltage (V)}}{20} \quad \pm 20\%$$

For loop stability, $R_{INT}$ should be ≥50 kΩ.

### Reference Capacitor ($C_{REF}$)

A 0.1-µF capacitor is suggested. Larger values may be used to limit roll-over errors. Low leakage capacitors (such as polypropylene) are required.

### Auto-Zero Capacitor ($C_{AZ}$)

A 0.1-µF polypropylene capacitor is suggested.

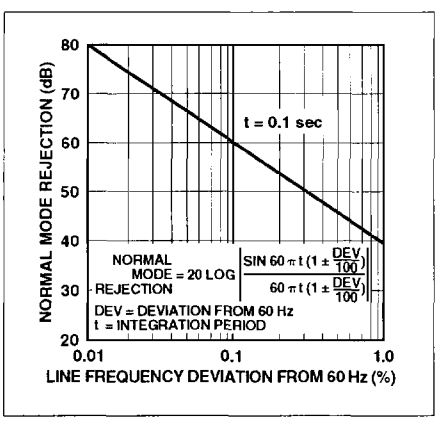



Figure 3. Normal Mode Rejection vs Input Frequency

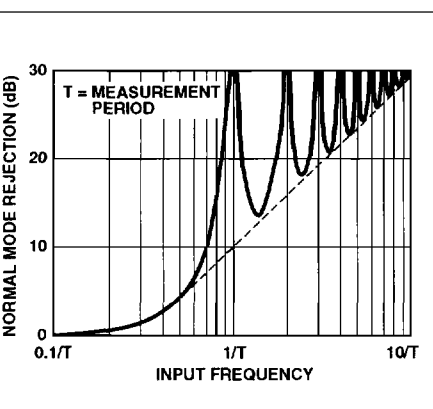



Figure 4. Intregrating Converter Normal Mode Rejection vs 60 Hz Line Frequency Variations

# TC500
# TC500A

## Integrating Capacitor ($C_{INT}$)

The integrating capacitor should be selected to maximize integrator output swing. The integrator output will swing to within 0.8V of $V_S^+$ or $V_S^-$ without saturating.

Using the suggested 20-μA full-scale buffer output current, the integrating capacitor is easily calculated:

$$C_{INT} = \frac{(t_{INT})(V_{FS})}{(V_{INT})(R_{INT})} \approx 5\, t_{INT}\ (\mu F)$$

where:

$t_{INT}$ = Integration period
$V_{FS}$ = Full-scale input voltage
$V_{INT}$ = Integrator output voltage swing

A very important integrating capacitor characteristic is dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polyester and polycarbonate capacitors may also be used in less critical applications.

The threshold noise ($N_{TH}$) is the algebraic sum of the integrator noise and the comparator noise. This value is typically about 30 μV. The graph shows how the value of the reference voltage can influence the results of the final count.

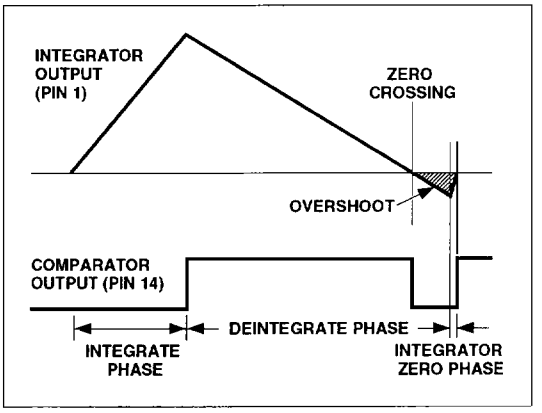
Errors caused by the low-frequency buffer noise may be reduced by increased integration times.

## Signal-to-Noise Ratio

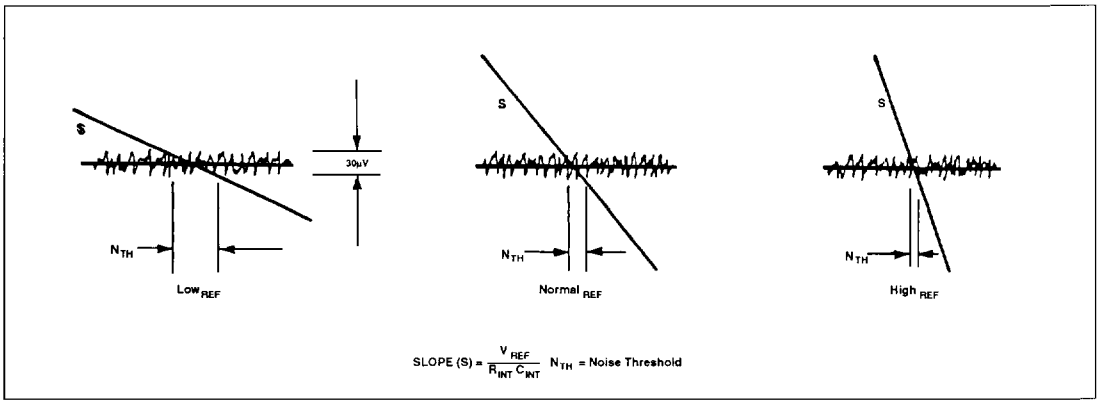
$$S/N\ (dB) = 20\ Log\left(\frac{V_{IN}}{30\ \mu V} \bullet \frac{t_{INT}}{R_{INT} \bullet C_{INT}}\right)$$

The maximum performance of the TC500/TC500A require that overshoot at the end of the deintegration phase be minimized. Also, the integrator zero phase may be terminated as soon as the comparator output returns to "high" (1).

## OVERSHOOT

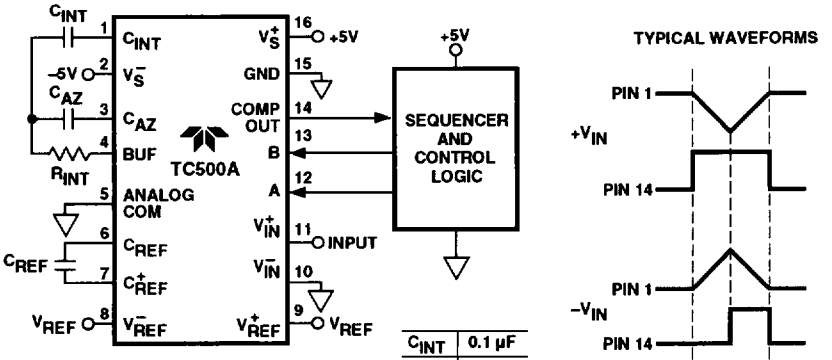



## NOISE



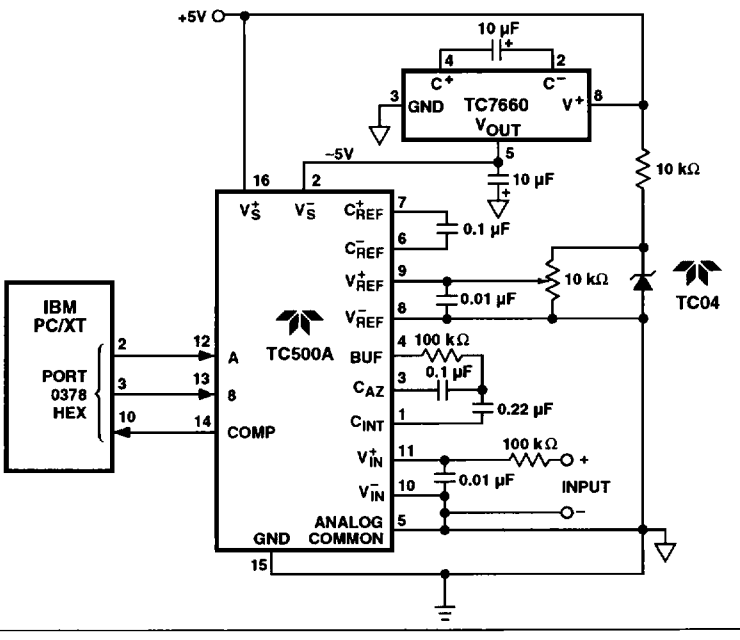
## TC500A DESIGN EXAMPLE (See "Component Selection Example")

TIMING CONDITIONS: A) AZ PLUS ZI..... 10,000 CLOCK PERIODS (40 ms)
B) INT..... 10,000 CLOCK PERIODS (40 ms)
C) DEINT..... $V_{IN}$ (V) 10,000 CLOCK PERIODS (14 bits)
D) CLOCK PERIOD..... 4 µs
E) $V_{FS}$..... ±2.5V




| | |
|---|---|
| $C_{INT}$ | 0.1 µF |
| $R_{INT}$ | 250 kΩ |
| $C_{AZ}$ | 0.1 µF |
| $C_{REF}$ | 0.1 µF |

## TC500A TO IBM PC/XT PRINTER PORT



## Interrupt Operation

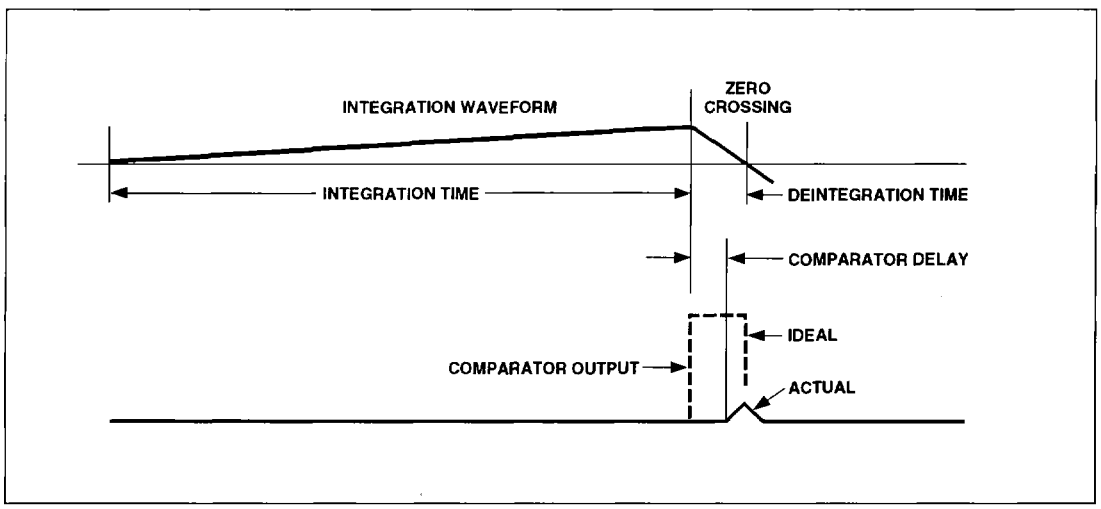
The comparator output stays low during the Integration phase (A=1, B=0) whenever the input polarity is negative. In those cases where the input polarity is negative AND very near zero, the zero-crossing occurs before the comparator has had a chance to go positive. Thus, no negative-edge will be generated and the microprocessor will not be interrupted.

With a negative input voltage very near zero, the output of the comparator does not have enough time to get full positive. This anomaly is caused by the comparator delay and rise time limitations.

One solution to overcome this condition is to have the microprocessor monitor the comparator output. It can then end the deintegration phase as soon as it sees a zero.

Another solution is to have the microprocessor enable the interrupt and look at the comparator output. If the output is high, the interrupt will be properly triggered. If the output is low, end the deintegration phase and disable the interrupt.

Either solution will produce reliable low voltage conversions.




## Rate of Conversion

The conversion times for the TC500/TC500A are a function of many variables and constants. The dominate component is $C_{INT}$:

$$\text{Conversion Time (sec)} = 0.4 \times C_{INT}\ (\mu F) \times (2 + (V_{IN}/V_{REF}))$$

The assumptions for this equation are suggested but not strictly required. They are:

Auto-zero time ($T_{AZ}$) = Integration time ($T_{NT}$)
Peak integration voltage ($V_{INT}$) = 4V
Maximum buffer current ($V_{IN(MAX)}/R_{INT}$) = 20 µA

## Component Selection Example

**Known:**

| | | |
|---|---|---|
| 1) | Supply voltage for TC500A | ($V_{SUP}$) |
| 2) | Maximum input voltage | ($V_{IN(MAX)}$) |
| 3) | Integration time | ($T_{INT}$) |
| 4) | Output resolution (bits) | (N) |
| 5) | Clock period | ($t_{CLOCK}$) |

**Assume:**

| | |
|---|---|
| $V_{SUP} = \pm 5V$ | $V_{SUP} = \lvert V_{SUP}\rvert$ |
| $V_{IN(MAX)} = \pm 2.5V$ | $V_{IN(MAX)} = \lvert V_{IN(MAX)}\rvert$ |
| $T_{INT}$ = 40 ms | |
| N = 14 bits | |
| $t_{CLOCK}$ = 4 µs | |

**Step 1:** Calculate $R_{INT}$ $\quad R_{INT} = \dfrac{V_{IN(MAX)}}{I_{BUF(MAX)}}$

Where $I_{BUF(MAX)} \approx 20\ \mu A$

$$R_{INT} = \frac{2.5V}{20\ \mu A} = 125K$$

Use 130K

$$\therefore I_{BUF} = \frac{2.5V}{130K} = 19.2\ \mu A$$

**Step 2:** Calculate $C_{INT}$ $\quad C_{INT} = \dfrac{T_{INT}\ I_{BUF(MAX)}}{V_{INT}}$

Where $V_{INT} = V_{SUP} - 1V = 4V$

$$C_{INT} = \frac{40\ ms\ 19.2\ \mu A}{4V} = 0.192\ \mu F$$

Use 0.2 µF

**Step 3:** Calculate $V_{REF}$ $\quad V_{REF} = \dfrac{V_{INT}\ C_{INT}\ R_{INT}}{T_{DEINT}}$

Where $T_{DEINT} = 2^N\ t_{CLOCK}$

$$V_{REF} = \frac{4V \bullet 0.2\ \mu F \bullet 130K}{2^N\ t_{CLOCK}} = 1.587...V$$

**Step 4:** Calculate integrate count $\quad K_{INT} = \dfrac{T_{INT}}{t_{CLOCK}}$

Where $R_{INT}$ $\quad \dfrac{40\ ms}{4\ \mu s} = 10{,}000$ Counts

**Results:** $K_{DEINT} = V_{IN}\ \dfrac{K_{INT}}{V_{REF}} = V_{IN}\ \dfrac{10{,}000}{1.587...V}$

Where $K_{DEINT}$ = Number of clock periods during $T_{DEINT}$

## Normalization

The reference voltage can be adjusted to scale the deintegrate count to be directly equivalent to the input voltage.

Since: $\quad \dfrac{K_{INT}}{V_{REF}} = \text{Counts/Volt}$

If: $\quad V_{REF}$ is adjusted such that

$$V_{REF} = \frac{10000\ \text{Counts}}{10000\ \text{Counts/Volt}} = \frac{K_{INT}}{10000\ \text{Counts/Volt}} = 1V$$

Then: $\quad K_{DEINT} = \dfrac{V_{IN}}{100\ \mu V}$ and N ≈ 14.61 Bits

e.g., $\quad$ If $K_{DEINT}$ = 18357 Counts,
then $V_{IN}$ = 1.8357V

## BONDING DIAGRAM