

DESCRIPTION:

The DPE832V is a high-performance Electrically Erasable and Programmable Read Only Memory (EEPROM) module and may be organized as 8K X 32, 16K X 16 or 32K X 8.

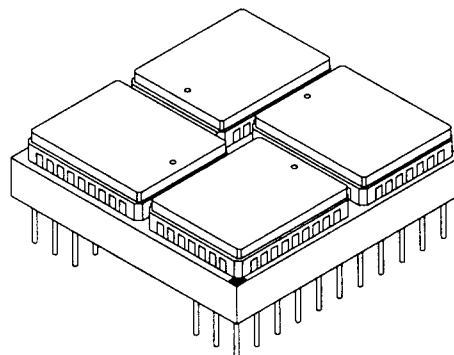
The module is built with four low-power CMOS 8K X 8 EEPROMs. The four chip enables are used for individual BWDW* selection. The DPE832V is ideally suited for those computer systems having 16-bit or 32-bit architectures.

The DPE832V contains a 32-BWDW page register to allow writing of up to 32 BWDWs simultaneously. During a write cycle, the address and 1 to 32 BWDWs of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the module will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA Polling of the most significant data bit in each byte. Once the end of a write cycle has been detected, a new access for a read or write can begin.

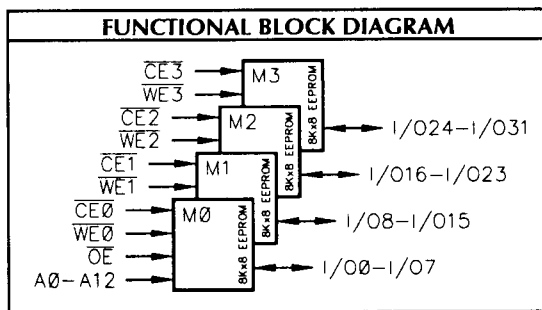
FEATURES:

- Fast Access Times: 55, 70, 90, 120, 150, 200, 250ns
- Automatic Page Write Operation
 - Internal Address and Data Latches
 - Internal Control Timer
- Fast Write Cycle Times
 - Page Write Cycle Time: 10ms maximum
 - 1 to 32 BWDW* Page Write Operation
- DATA Polling for END of Write Detection
- High Reliability CMOS Technology
 - Endurance: 10⁴ Cycles
 - Data Retention: 10 years
- Single +5V Power Supply, ±10% Tolerance
- CMOS and TTL Compatible Inputs and Outputs
- Available with All Semiconductor Components used to Construct the Module Compliant to MIL-STD-883; Class B
- 66-Pin PGA (Grid Array) Package
- Same Package as other Versapac Versions (SRAMs, EPROMs, and Mixed)

* Byte, Word or Double Word (BWDW)

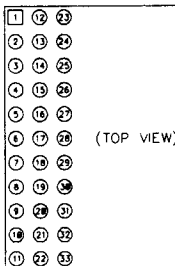


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| PIN NAMES | |
|--------------|----------------|
| A0 - A12 | Address Inputs |
| I/O0 - I/O31 | Data In/Out |
| CE0 - CE3 | Chip Enables |
| WE0 - WE3 | Write Enables |
| OE | Output Enable |
| VDD | Power (+5V) |
| Vss | Ground |
| N.C. | No Connect |

PIN-OUT DIAGRAM

| | | | | | | |
|---------|----------|----------|---|----------|----------|----------|
| 1 I/O8 | 12 WE1 | 23 I/O14 |  | 34 I/O24 | 45 VDD | 56 I/O30 |
| 2 I/O9 | 13 CE1 | 24 I/O13 | | 35 I/O25 | 46 CE3 | 57 I/O29 |
| 3 I/O10 | 14 VSS | 25 I/O12 | | 36 I/O26 | 47 WE3 | 58 I/O28 |
| 4 N.C. | 15 I/O15 | 26 I/O11 | | 37 A6 | 48 I/O31 | 59 I/O27 |
| 5 N.C. | 16 A10 | 27 OE | | 38 A7 | 49 A3 | 60 A0 |
| 6 N.C. | 17 A11 | 28 N.C. | | 39 N.C. | 50 A4 | 61 A1 |
| 7 N.C. | 18 A12 | 29 WE0 | (TOP VIEW) | 40 A8 | 51 A5 | 62 A2 |
| 8 N.C. | 19 VDD | 30 I/O6 | | 41 A9 | 52 WE2 | 63 I/O22 |
| 9 I/O0 | 20 CE0 | 31 I/O5 | | 42 I/O16 | 53 CE2 | 64 I/O21 |
| 10 I/O1 | 21 N.C. | 32 I/O4 | | 43 I/O17 | 54 VSS | 65 I/O20 |
| 11 I/O2 | 22 I/O7 | 33 I/O3 | | 44 I/O18 | 55 I/O23 | 66 I/O19 |

FOR FURTHER INFORMATION
SEE CHAPTER 10
FOR COMPLETE DATA SHEET