

MB814100A-60L/-70L/-80L

CMOS 4M x 1 BIT FAST PAGE MODE LOW POWER DRAM

CMOS 4,194,304 x 1 Bit Fast Page Mode Low Power Dynamic RAM

The Fujitsu MB814100A is a fully decoded CMOS Dynamic RAM (DRAM) that contains a total of 4,194,304 memory cells in a x1 configuration. The MB814100A features a "fast page" mode of operation whereby high-speed random access of up to 2,048-bits of data can be selected in the same row. The MB814100A-60L/-70L/-80L DRAM is ideally suited for memory applications such as embedded control, buffers, portable computers, and video imaging equipment where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB814100A-60L/-70L/-80L is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB814100A is fabricated using silicon gate CMOS and Fujitsu's advanced four-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB814100A are not critical and all inputs are TTL compatible.

PRODUCT LINE & FEATURES

Parameter		MB814100A-60L	MB814100A-70L	MB814100A-80L
RAS Access Time		60ns max.	70ns max.	80ns max.
CAS Access Time		15ns max.	20ns max.	20ns max.
Address Access Time		30ns max.	35ns max.	40ns max.
Random Cycle Time		110ns min.	125ns min.	140ns min.
Fastpage Mode Cycle Time		40ns min.	45ns min.	45ns min.
Low Power Dissipation	Operating current	605mW max.	550mW max.	495mW max.
	Standby current	8.25mW max. (TTL level) 1.1mW max. (CMOS level)		
	Battery Back up current	1.4mW max		

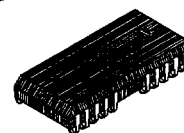
- 4,194,304 word x 1 bit organization
- Common I/O capability by using early write
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- $\overline{\text{RAS}}$ only, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$, or Hidden Refresh
- All input and output are TTL compatible
- Fast Page Mode, Read-Modify-Write capability
- 1024 refresh cycles every 128ms
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see Note)

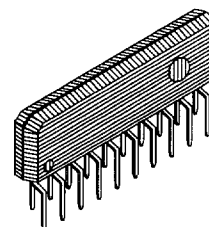
Parameter	Symbol	Value	Unit
Voltage at any pin relative to VSS	$V_{\text{IN}}, V_{\text{OUT}}$	-1 to +7	V
Voltage of V_{CC} supply relative to VSS	V_{CC}	-1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current		50	mA
Storage Temperature	TSTG	-55 to +125	°C

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

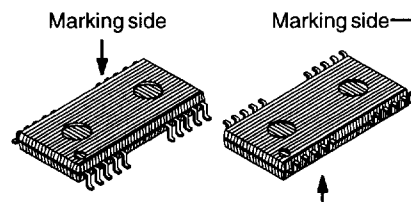
PRELIMINARY



Plastic SOJ Package
(LCC-26P-M04)



Plastic ZIP Package
(ZIP-20P-M02)



Plastic TSOP Packages
(FPT-26P-M01) (Normal Bend) (FPT-26P-M02) (Reverse Bend)

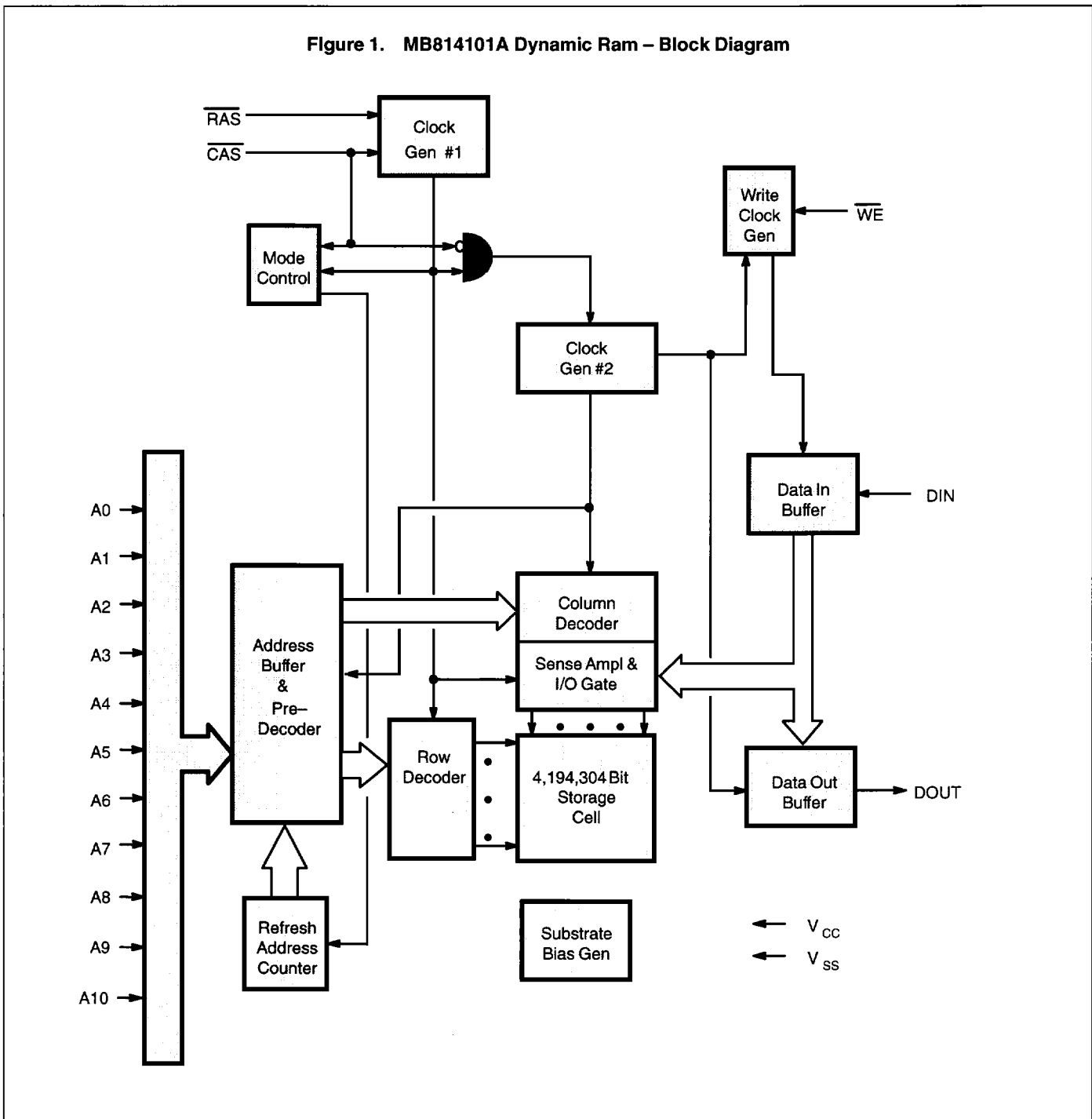
Package and Ordering Information

- 26-pin plastic (300mil) SOJ order as MB814100A-xxLPJN
- 20-pin plastic (400mil) ZIP order as MB814100A-xxLPZ
- 26-pin plastic (300mil) TSOP-II with normal bend leads order as MB814100A-xxLPJN
- 26-pin plastic (300mil) TSOP-II with reverse bend leads order as MB814100A-xxLPTR

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUJMS120

Figure 1. MB814101A Dynamic Ram - Block Diagram

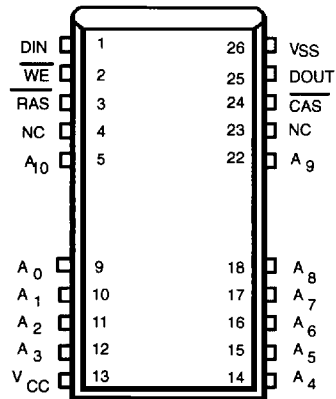


CAPACITANCE (T_A = 25°C, f = MHz)

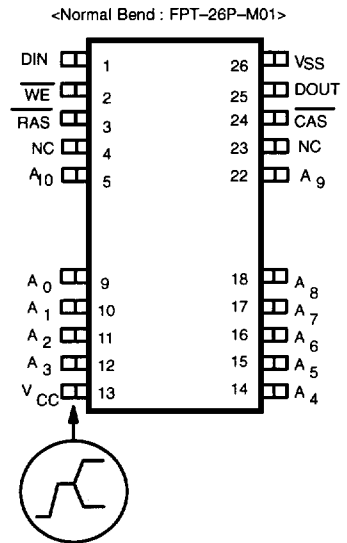
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A10, DIN	C _{IN1}	—	5	pF
Input Capacitance, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	C _{IN2}	—	7	pF
Output Capacitance, D _{OUT}	C _{OUT}	—	7	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

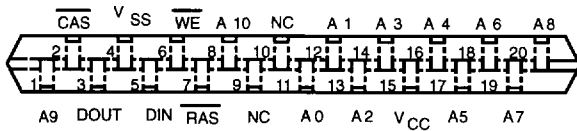
26-Pin SOJ:
(TOP VIEW)



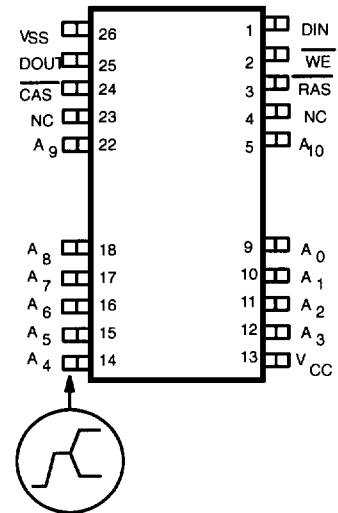
26-Pin FPT:
(TOP VIEW)



20-Pin ZIP:
(TOP VIEW)



<Reverse Bend : FPT-26P-M02>



Designator	Function
D _{IN}	Data Input
D _{OUT}	Data Output
\overline{WE}	Write Enable
\overline{RAS}	Row Address Strobe
NC	No Connection
A ₀ to A ₁₀	Address Inputs
VCC	+5 volt power supply
\overline{CAS}	Column address strobe
VSS	Circuit ground

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V _{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V _{SS}	0	0	0		
Input High Voltage, all inputs	1	V _{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	V _{IL}	-2.0	—	0.8	V	

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty-two input bits are required to decode any one of 4,194,304 cell addresses in the memory matrix. Since only eleven address bits (A0-A10) are available, the column and row inputs are separately strobed by RAS and CAS as shown in Figure 5. First, eleven row address bits are applied on pins A0 through A10 and latched with the row address strobe (RAS) then, eleven column address bits are applied and latched with the column address strobe (CAS). Both row and column addresses must be stable on or before the falling edge of RAS and CAS respectively. The address latches are of the flow-through type; thus, address information appearing after t_{RAH} (min) + t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of \overline{WE} . When \overline{WE} is active Low, a write cycle is initiated; when \overline{WE} is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of two basic ways—an early write cycle and a read-modify-write cycle. The falling edge of \overline{WE} or \overline{CAS} , whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data is strobed by \overline{CAS} and the setup/hold times are referenced to \overline{CAS} because \overline{WE} goes Low before \overline{CAS} . In a delayed write or a read-modify-write cycle, \overline{WE} goes Low after \overline{CAS} ; thus, input data is strobed by \overline{WE} and all setup/hold times are referenced to the write-enable signal.

DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

- t_{RAC} : from the falling edge of \overline{RAS} when t_{RCD} (max) is satisfied.
- t_{CAC} : from the falling edge of \overline{CAS} when t_{RCD} is greater than t_{RCD} (max).
- t_{AA} : from column address input when t_{RAD} is greater than t_{RAD} (max).

The data remains valid until either \overline{CAS} returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, RAS is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 2,048 bits can be accessed and, when multiple MB814100s are used, CAS is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or read-modify-write cycles are permitted.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Notes 3

Parameter	Notes	Symbol	Conditions	Value			Unit
				Min	Typ	Max	
Output high voltage	1	V_{OH}	$I_{OH} = -5 \text{ mA}$	2.4			V
Output low voltage	1	V_{OL}	$I_{OL} = 4.2 \text{ mA}$			0.4	
Input leakage current (any input)		$I_{I(L)}$	$0V \leq V_{IN} \leq 5.5V$ $4.5 \leq V_{CC} \leq 5.5V$; $V_{SS} = 0V$; All other pins not under test = $0V$	-10		10	μA
Output leakage current		$I_{O(L)}$	$0V \leq V_{OUT} \leq 5.5V$; Data out disabled	-10		10	
Operating current (Average Power supply current)	2	MB814100A-60L	\overline{RAS} & \overline{CAS} cycling; $t_{RC} = \text{min}$			110	mA
		MB814100A-70L				100	
		MB814100A-80L				90	
Standby Current (Power supply current)	2	TTL level	$\overline{RAS} = \overline{CAS} = V_{IH}$			2.0	mA
		CMOS level	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2V$			1.0	
Refresh current #1 (Average power supply current)	2	MB814100A-60L	$\overline{CAS} = V_{IH}$, \overline{RAS} cycling; $t_{RC} = \text{min}$			110	mA
		MB814100A-70L				100	
		MB814100A-80L				90	
Fast Page Mode current	2	MB814100A-60L	$\overline{RAS} = V_{IL}$, \overline{CAS} cycling; $t_{PC} = \text{min}$			55	mA
		MB814100A-70L				50	
		MB814100A-80L				45	
Refresh current #2 (Average power supply current)	2	MB814100A-60L	RAS cycling; \overline{CAS} -before-RAS; $t_{RC} = \text{min}$			90	mA
		MB814100A-70L				80	
		MB814100A-80L				70	
Battery Back up current (Average power supply current)	2	MB814100A-60L	RAS cycling; \overline{CAS} -before-RAS; $t_{RC} = 125\mu\text{s}$, $t_{RAS} = \text{min to } 1\mu\text{s}$ $V_{IH} > V_{CC} - 0.2V$, $V_{IL} < 0.2V$			250	μA
		MB814100A-70L					
		MB814100A-80L					

MB814100A-60L
MB814100A-70L
MB814100A-80L

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted). Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814100A-60		MB814100A-70		MB814100A-80		Unit
				Min.	Max	Min.	Max	Min.	Max	
1	Time Between Refresh		t_{REF}		16.4		16.4		16.4	ms
2	Random Read/Write Cycle Time		t_{RC}	110		125		140		ns
3	Read-Modify-Write Cycle Time		t_{RW}	130		150		165		ns
4	Access Time from \overline{RAS}	6, 9	t_{RAC}		60		70		80	ns
5	Access Time from \overline{CAS}	7, 9	t_{CAC}		15		20		20	ns
6	Column Address Access Time	8, 9	t_{AA}		30		35		40	ns
7	Output Hold Time		t_{OH}	0		0		0		ns
8	Output Buffer Turn On Delay Time		t_{ON}	0		0		0		ns
9	Output Buffer Turn Off Delay Time	10	t_{OFF}		15		15		20	ns
10	Transition Time		t_T	2	50	2	50	2	50	ns
11	\overline{RAS} Precharge Time		t_{RP}	40		45		50		ns
12	\overline{RAS} Pulse Width		t_{RAS}	60	100000	70	100000	80	100000	ns
13	\overline{RAS} Hold Time		t_{RSH}	15		20		20		ns
14	\overline{CAS} to \overline{RAS} Precharge Time		t_{CRP}	5		5		5		ns
15	\overline{RAS} to \overline{CAS} Delay Time	11, 12	t_{RCD}	20	45	20	50	20	60	ns
16	\overline{CAS} Pulse Width		t_{CAS}	15		20		20		ns
17	\overline{CAS} Hold Time		t_{CSH}	60		70		80		ns
18	\overline{CAS} Precharge Time (Normal)	17	t_{CPN}	10		10		10		ns
19	Row Address Set Up Time		t_{ASR}	0		0		0		ns
20	Row Address Hold Time		t_{RAH}	10		10		10		ns
21	Column Address Set Up Time		t_{ASC}	0		0		0		ns
22	Column Address Hold Time		t_{CAH}	12		12		15		ns
23	\overline{RAS} to Column Address Delay Time	13	t_{RAD}	15	30	15	35	15	40	ns
24	Column Address to \overline{RAS} Lead Time		t_{RAL}	30		35		40		ns
25	Column Address to \overline{CAS} Lead Time		t_{CAL}	30		35		40		ns
26	Read Command Set Up Time		t_{RCS}	0		0		0		ns
27	Read Command Hold Time Reference to \overline{RAS}	14	t_{RRH}	0		0		0		ns
28	Read Command Hold Time Referenced to \overline{CAS}	14	t_{RCH}	0		0		0		ns
29	Write Command Set Up Time	15	t_{WCS}	0		0		0		ns
30	Write Command Hold Time		t_{WCH}	10		10		12		ns
31	\overline{WE} Pulse Width		t_{WP}	10		10		12		ns
32	Write Command to \overline{RAS} Lead Time		t_{RWL}	15		20		20		ns
33	Write Command to \overline{CAS} Lead Time		t_{CWL}	15		18		20		ns
34	DIN Set Up Time		t_{DS}	0		0		0		ns
35	DIN Hold Time		t_{DH}	10		10		12		ns
36	\overline{RAS} to \overline{WE} Delay Time	15	t_{RWD}	60		70		80		ns
37	\overline{CAS} to \overline{WE} Delay Time	15	t_{CWD}	15		20		20		ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted). Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814100A-60		MB814100A-70		MB814100A-80		Unit
				Min.	Max	Min.	Max	Min.	Max	
38	Column Address to WE Delay Time	15	t_{AWD}	30		35	—	40		ns
39	\overline{RAS} Precharge Time to \overline{CAS} Active Time (Refresh Cycles)		t_{RPC}	0		0		0		ns
40	\overline{CAS} Set Up Time for \overline{CAS} -before- \overline{RAS} Refresh		t_{CSR}	0		0		0		ns
41	\overline{CAS} Hold Time for \overline{CAS} -before- \overline{RAS} Refresh		t_{CHR}	10		10		12		ns
42	\overline{WE} Set Up Time from \overline{RAS}	18	t_{WSR}	0		0		0		ns
43	\overline{WE} Hold Time from \overline{RAS}	18	t_{WHR}	10		10		10		ns
51	Fast Page Mode Read/Write Cycle Time		t_{PC}	40		45		45		ns
52	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	60		68		70		ns
53	Access Time from \overline{CAS} Precharge	9, 16	t_{CPA}		35		40		40	ns
54	Fast Page Mode \overline{CAS} Precharge Time		t_{CP}	10		10		10		ns
55	Fast Page Mode \overline{RAS} Pulse width		t_{RASP}		200000		200000		200000	ns
56	Fast Page Mode \overline{RAS} Hold Time from \overline{CAS} Precharge		t_{RHCP}	35		40		40		ns
57	Fast Page Mode \overline{CAS} Precharge to \overline{WE} Delay Time		t_{CPWD}	35		40		40		ns

Notes:

- Referenced to VSS
- I_{CC} depends on the output load conditions and cycle rates. The specified values are obtained with the output open.
 I_{CC} depends on the number of address change as $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
 I_{CC1} , I_{CC3} and I_{CC5} are specified at one time of address change during $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
 I_{CC4} is specified at one time of address change during one Page Cycle.
- An Initial pause ($\overline{RAS}=\overline{CAS}=V_{IH}$) of 200 μ s is required after power-up followed by any eight \overline{RAS} -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight \overline{CAS} -before- \overline{RAS} initialization cycles instead of 8 \overline{RAS} cycles are required.
- AC characteristics assume $t_T = 5$ ns.
- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
- Assumes that $t_{RCD} \geq t_{RCD}(\max)$, $t_{RAD} \leq t_{RAD}(\max)$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Figures 2 and 3.
- If $t_{RCD} \geq t_{RCD}(\max)$, $t_{RAD} \geq t_{RAD}(\max)$, and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC} .
- If $t_{RAD} \geq t_{RAD}(\max)$ and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{AA} .
- Measured with a load equivalent to two TTL loads and 100 pF.
- t_{OFF} is specified that output buffer change to high impedance state.
- Operation within the $t_{RCD}(\max)$ limit ensures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
- $t_{RCD}(\min) = t_{RAH}(\min) + 2t_T + t_{ASC}(\min)$.
- Operation within the $t_{RAD}(\max)$ limit ensures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
- Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
- t_{WCS} , t_{CWD} , t_{RWD} and t_{AWD} are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}(\min)$, the cycle is an early write cycle and D_{OUT} pin will maintain high impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$, and $t_{AWD} \geq t_{AWD}(\min)$, the cycle is a read modify-write cycle and data from the selected cell will appear at the D_{OUT} pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the D_{OUT} pin, and write operation can be executed by satisfying t_{RWL} , t_{CWL} , t_{CAL} and t_{RAL} specifications.
- t_{CPA} is access time from the selection of a new column address (that is caused by changing \overline{CAS} from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than $t_{CPA}(\max)$.
- Assumes that \overline{CAS} -before- \overline{RAS} refresh.
- Assumes that Test mode function.

Figure 2. t_{RAC} vs. t_{RCD}

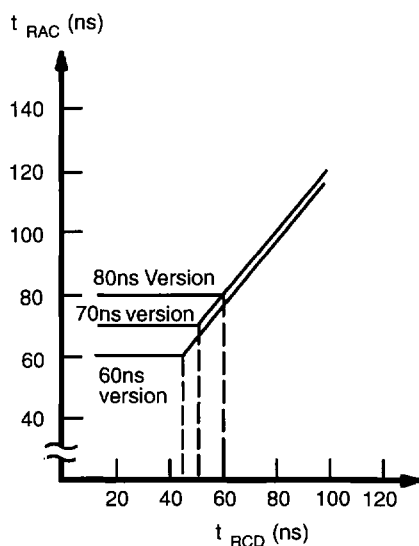


Figure 3. t_{RAC} vs. t_{RAD}

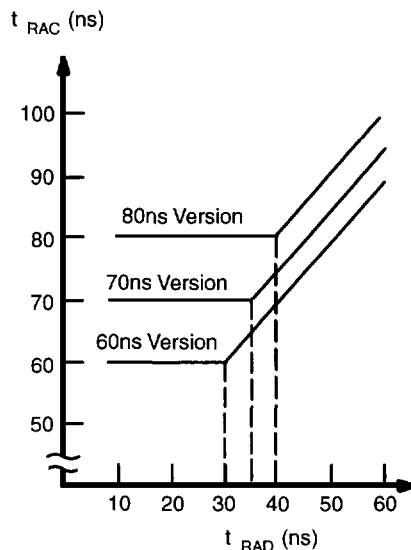
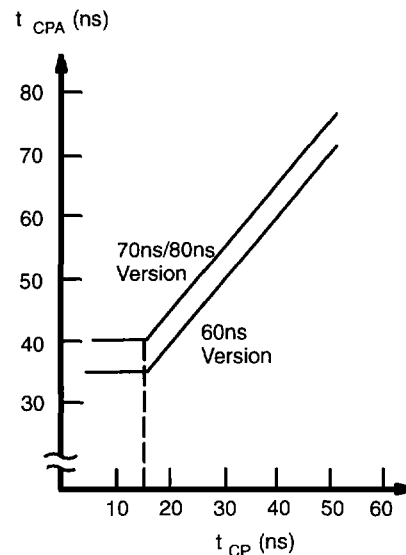


Figure 4. t_{CPA} vs. t_{CP}



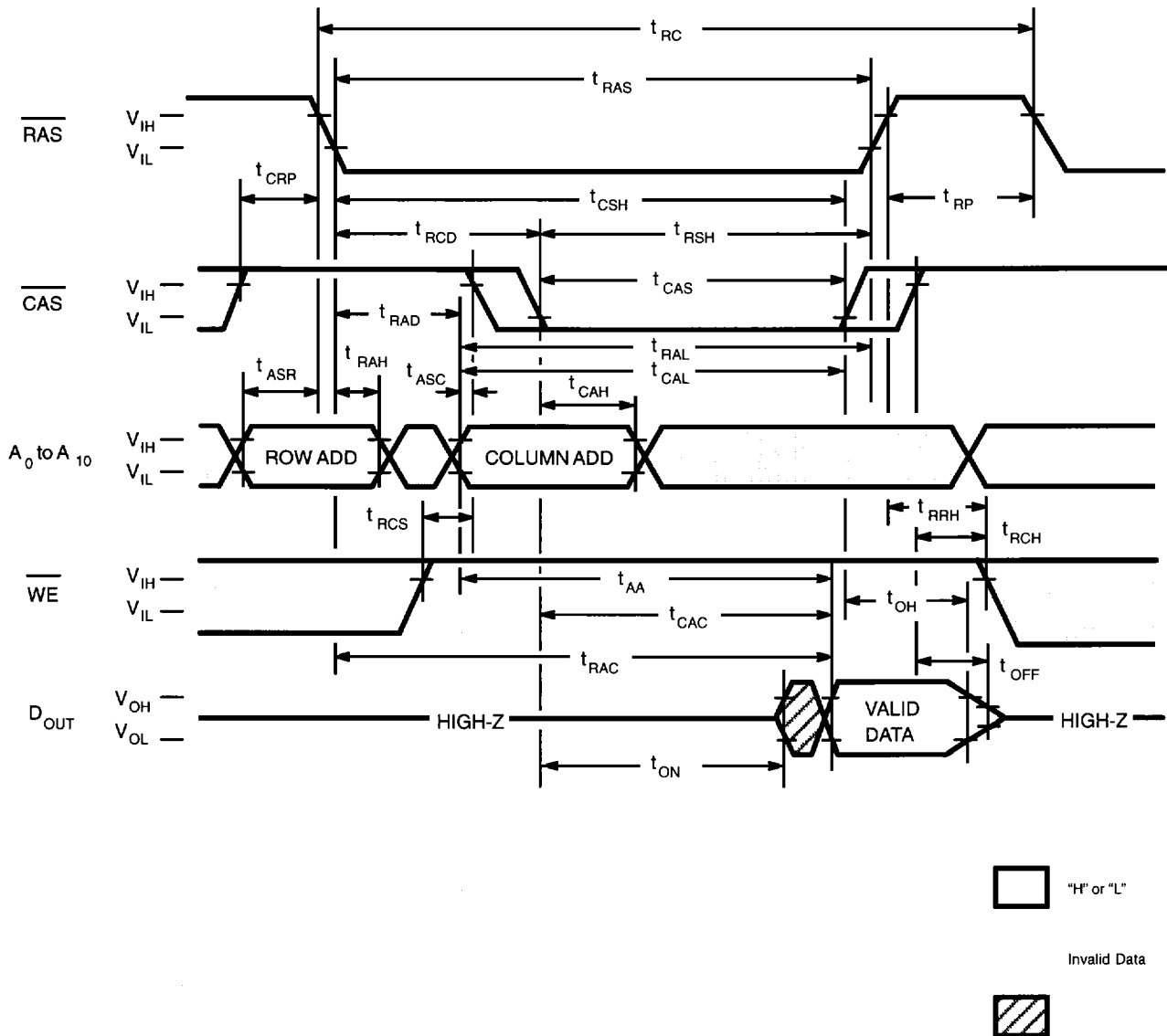
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	RAS	CAS	WE	Row	Column	Input	Output		
Standby	H	H	X				High-Z		
Read Cycle	L	L	H	Valid	Valid		Valid	Yes ¹	$t_{RCS} \geq t_{RCS}(\text{min})$
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	Yes ¹	$t_{WCS} \geq t_{WCS}(\text{min})$
Read-Modify-Write Cycle	L	L	H → L	Valid	Valid	X → Valid	Valid	Yes ¹	$t_{CWD} \geq t_{CWD}(\text{min})$
$\overline{\text{RAS}}$ -only Refresh Cycle	L	H	X	Valid			High-Z	Yes	
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle	L	L	H				High-Z	Yes	$t_{CSR} \geq t_{CSR}(\text{min})$
Hidden Refresh Cycle	H → L	L	H				Valid	Yes	Previous data is kept
Test mode set cycle (CBR)	L	L	L				High-Z	Yes	$t_{CSR} \geq t_{CSR}(\text{min})$ $t_{WSR} \geq t_{WSR}(\text{min})$
Test Mode set cycle (Hidden)	H → L						Valid	Yes	$t_{CSR} \geq t_{CSR}(\text{min})$ $t_{WSR} \geq t_{WSR}(\text{min})$

Notes: X= "H" or "L"

1. It is impossible in Fast Page Mode.

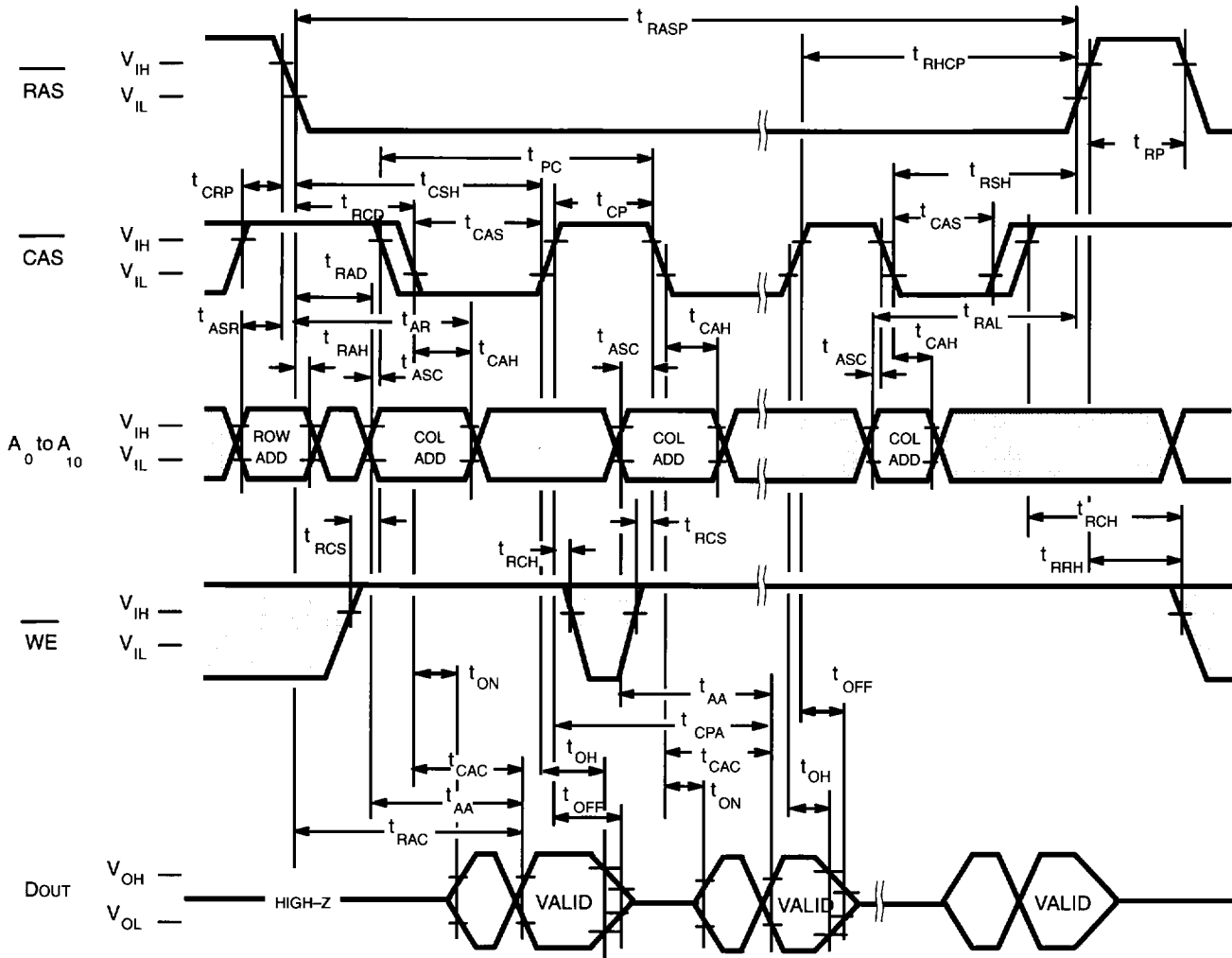
Figure 5. Read Cycle



DESCRIPTION

The read cycle is executed by keeping both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ "L" and keeping $\overline{\text{WE}}$ "H" throughout the cycle. The row and column addresses are latched with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$, respectively. The data output remains valid with $\overline{\text{CAS}}$ "L", i.e., if $\overline{\text{CAS}}$ goes "H", the data becomes invalid after t_{OH} is satisfied. The access time is determined by $\overline{\text{RAS}}$ (t_{RAC}), $\overline{\text{CAS}}$ (t_{CAC}), or column address input (t_{AA}). If t_{RCD} ($\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time) is greater than the specification, the access time is t_{AA} .

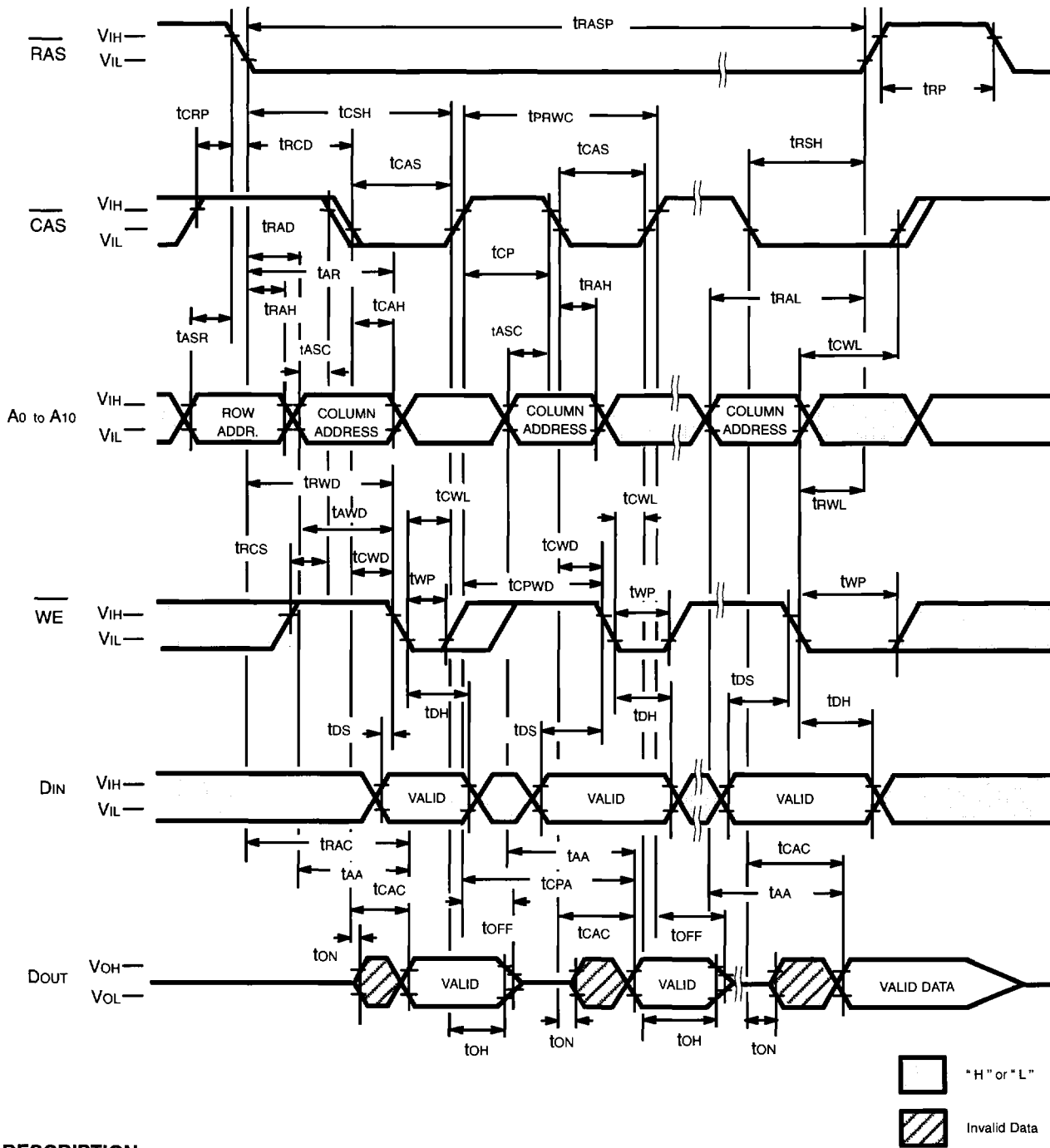
Figure 8. Fast Page Mode Read Cycle



DESCRIPTION

The fast page mode read cycle is executed after normal cycle with holding \overline{RAS} "L", applying column address and \overline{CAS} , and keeping WE "H". Once an address is selected normally using the \overline{RAS} and \overline{CAS} , other addresses in the same row can be selected by only changing the column address and applying the \overline{CAS} . During fast page mode, the access time is t_{CAC} , t_{AA} , or t_{CPA} , whichever occurs later. Any of the 2048 bits belonging to each row can be accessed.

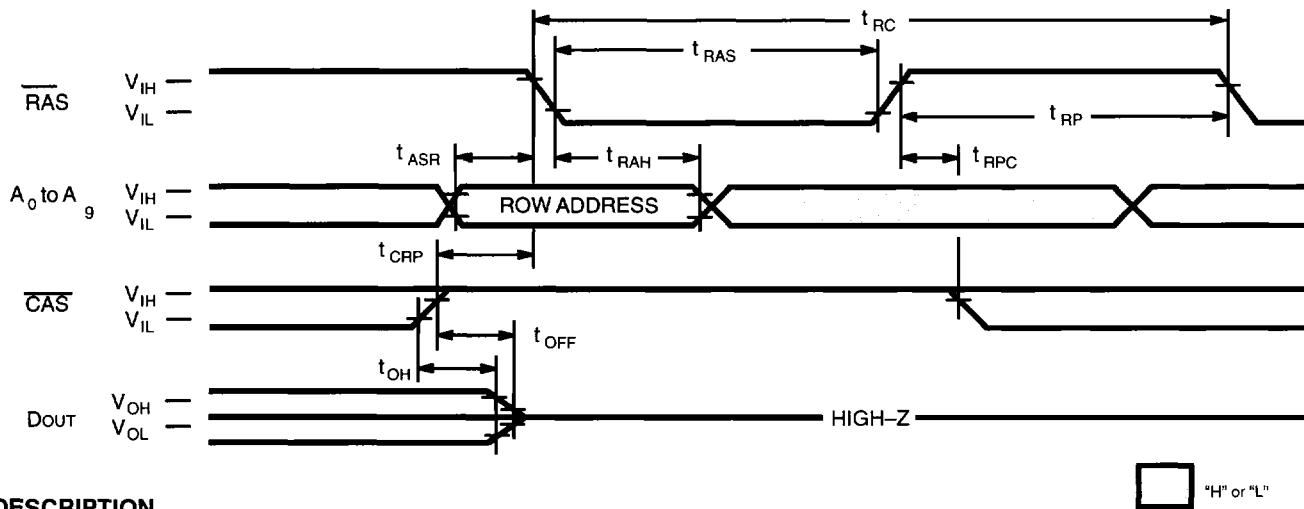
Figure 10. Fast Page Mode Read-Modify-Write Cycle



DESCRIPTION

During the fast page mode, the read-modify-write cycle can be executed by changing \overline{WE} high to low after the data appears at DOUT pin as well as normal cycle. Any of the 2048 bits belonging to each row can be accessed.

Figure 11. RAS-Only Refresh ($\overline{\text{WE}}$, DIN, A10 = "H" or "L")

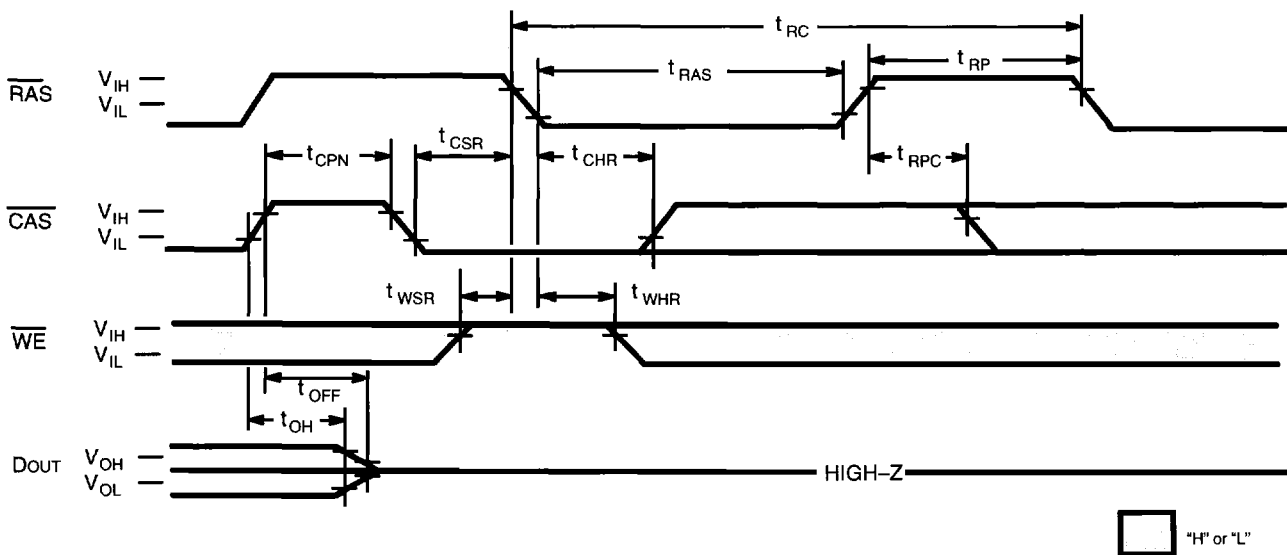


DESCRIPTION

The refresh of DRAM is executed by normal read, write or read-modify-write cycle, i.e., the cells on the one row line are also refreshed by executing one of three cycles. 1024 row address must be refreshed every 128ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and rewritten to the cell. The MB814100A has three types of refresh modes, RAS-only refresh, CAS-before-RAS refresh, and Hidden refresh.

The RAS only refresh is executed by keeping $\overline{\text{RAS}}$ "L" and $\overline{\text{CAS}}$ "H" throughout the cycle. The row address to be refreshed is latched on the falling edge of RAS. During RAS only refresh, the D_{OUT} pin is kept in a high impedance state.

Figure 12. CAS-Before-RAS Refresh (A0 to A10, DIN = "H" or "L")

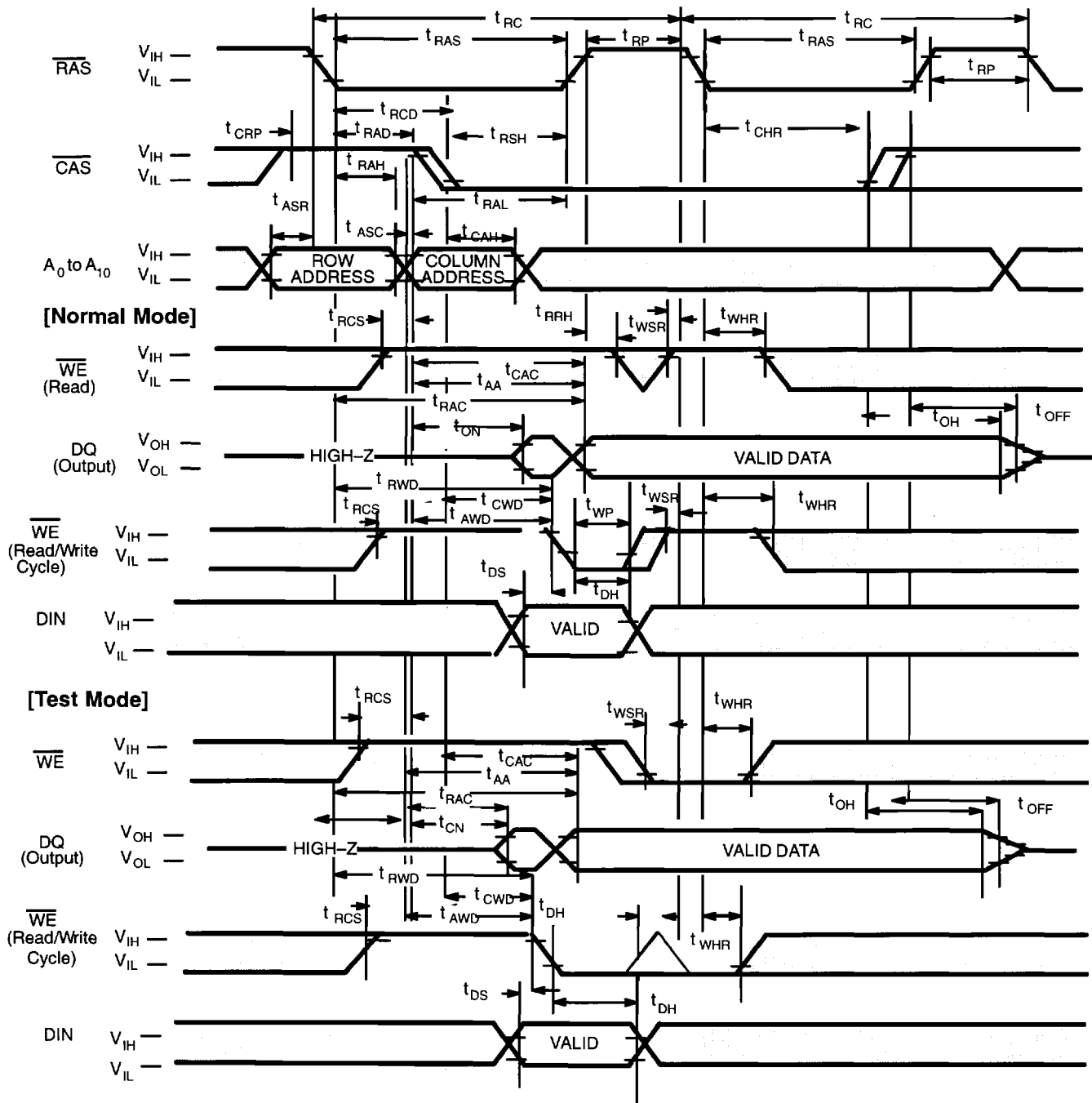


DESCRIPTION

The CAS-before-RAS refresh is executed by bringing $\overline{\text{CAS}}$ "L" before $\overline{\text{RAS}}$. By this timing combination, the MB814100A executes CAS-before-RAS refresh. The row address input is not necessary because it is generated internally.

$\overline{\text{WE}}$ must be held "H" for the specified set up time (t_{WSR}) before $\overline{\text{RAS}}$ goes "L" in order not to enter "test mode".

Figure 13. Hidden Refresh Cycle

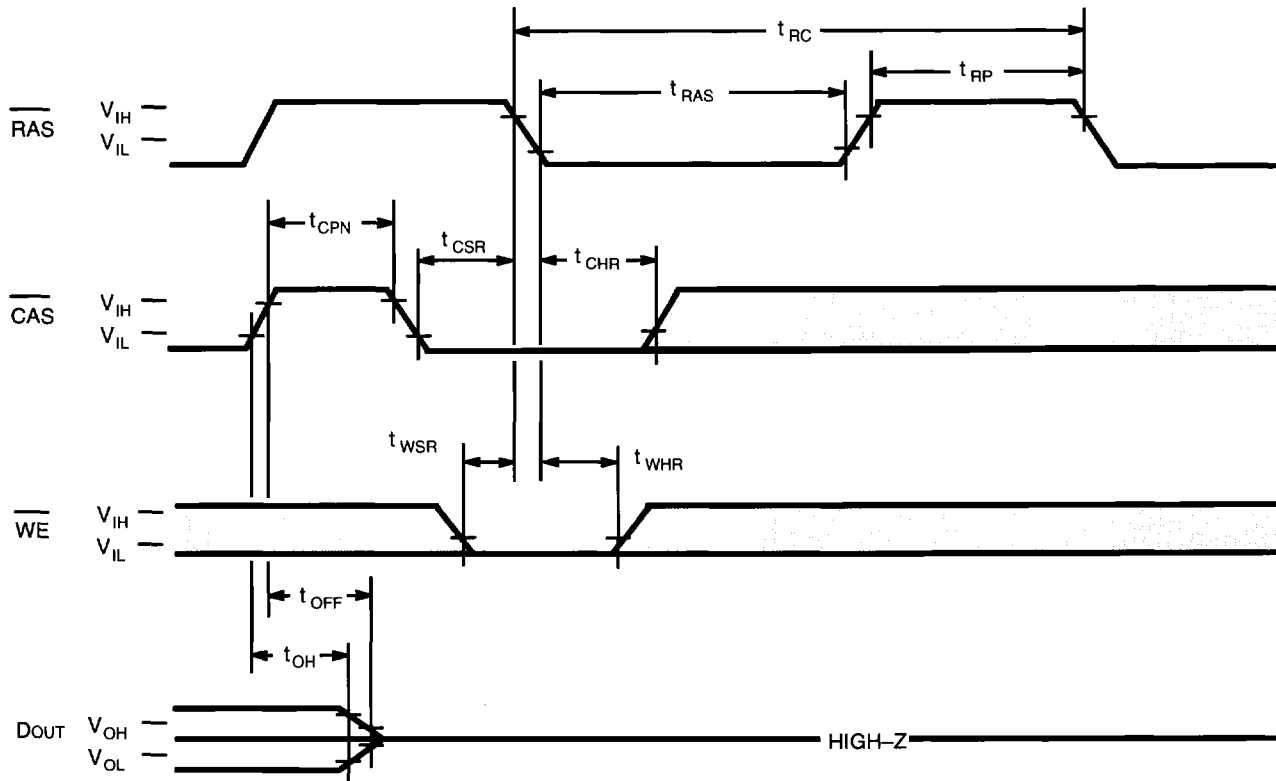


"H" or "L"

DESCRIPTION

The hidden refresh is executed by keeping $\overline{\text{CAS}}$ "L" to next cycle, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{\text{CAS}}$ is kept low continuously from previous cycle, followed refresh cycle should be CAS-before-RAS refresh. $\overline{\text{WE}}$ must be held "H" for the specified set up time (t_{WSR}) before RAS goes "L" for the second time in order not to enter "test mode."

Figure 14. Test Mode Set Cycle (A0 to A10, DIN = "H" or "L")



"H" or "L"

DESCRIPTION

Test Mode

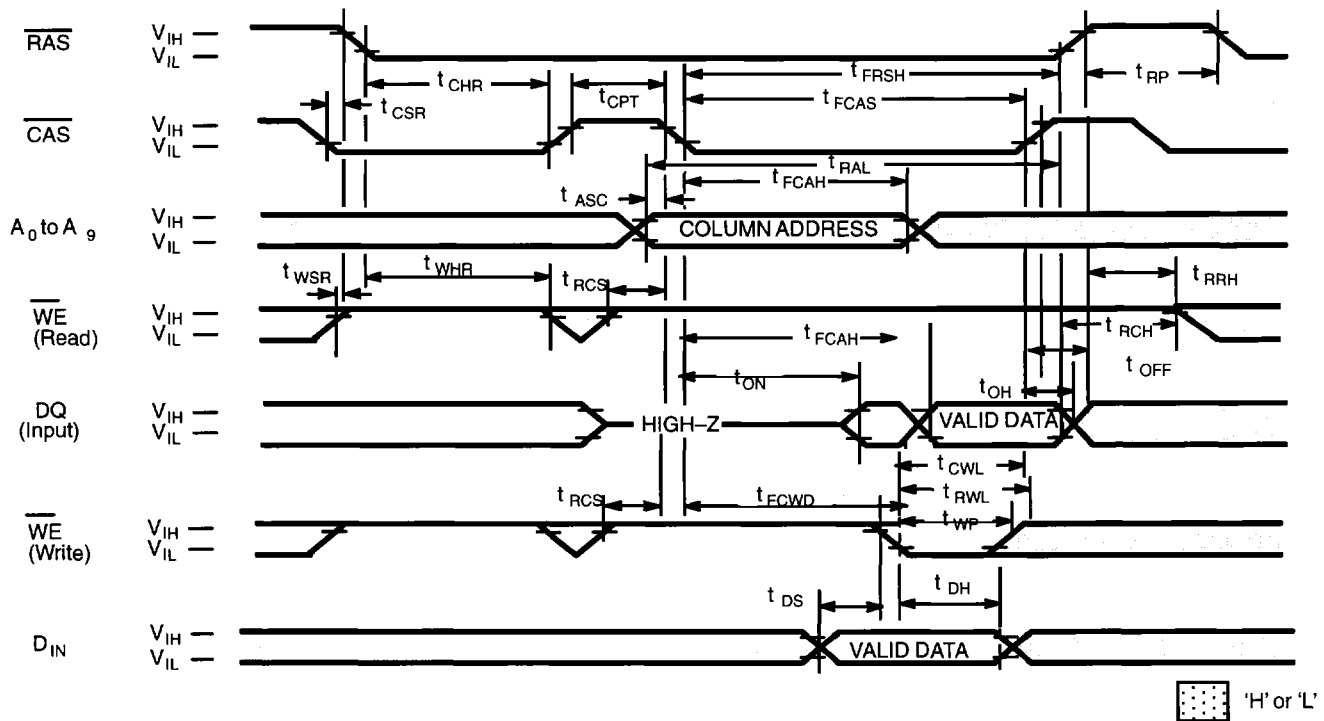
The purpose of this test mode is to reduce device test time to one eighth of that required to test the device conventionally. The test mode function is entered by performing a \overline{WE} and \overline{CAS} -before- \overline{RAS} (WCBR) refresh for the entry cycle. In the test mode, read and write operations are executed in units of eight bits which are selected by the address combination of RA10, CA0 and CA10. In the write mode, data at DIN is written into eight cells simultaneously. In the read mode, eight cells at the selected addresses are read back and checked in the following manner.

- When the eight bits are all "L" or all "H", a "H" level is output.
- When the eight bits show a combination of "L" and "H", a "L" level is output.

The test mode function is exited by performing a \overline{RAS} -only refresh or a \overline{CAS} -before- \overline{RAS} refresh for the exit cycle. In test mode operation, the following parameters are delayed approximately 5ns from the specified value in the data sheet.

t_{RC} , t_{RWC} , t_{RAC} , t_{AA} , t_{RAS} , t_{CSH} , t_{RAL} , t_{RWD} , t_{AWD} , t_C , t_{PRWC} , t_{CPA} , t_{RHCP} , t_{CPWD}

Figure 15. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Counter Test Cycle



DESCRIPTION

A special timing sequence using the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh circuitry. If, after a $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle, $\overline{\text{CAS}}$ makes a transition from High to Low while $\overline{\text{RAS}}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A10 are defined by the on-chip refresh counter.

Column Address: Bits A0 through A10 are defined by latching levels on A0-A9 at the second falling edge of $\overline{\text{CAS}}$.

The $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Counter Test procedure is as follows:

1. Initialize the internal refresh address counter by using 8 $\overline{\text{RAS}}$ only refresh cycles.
2. Use the same column address throughout the test.
3. Write "0" to all 1024 row addresses at the same column address by using normal write cycles.
4. Read "0" written in procedure 3 and check, simultaneously write "1" to the same addresses by using $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh counter test (read-modify-write cycles). Repeat this procedure 1024 times with addresses generated by the internal refresh address counter.
5. Read and check data written in procedure 4 by using normal read cycle for all 1024 memory locations.
6. Reverse test data and repeat procedures 3, 4, and 5.

(At recommended operating conditions unless otherwise noted)

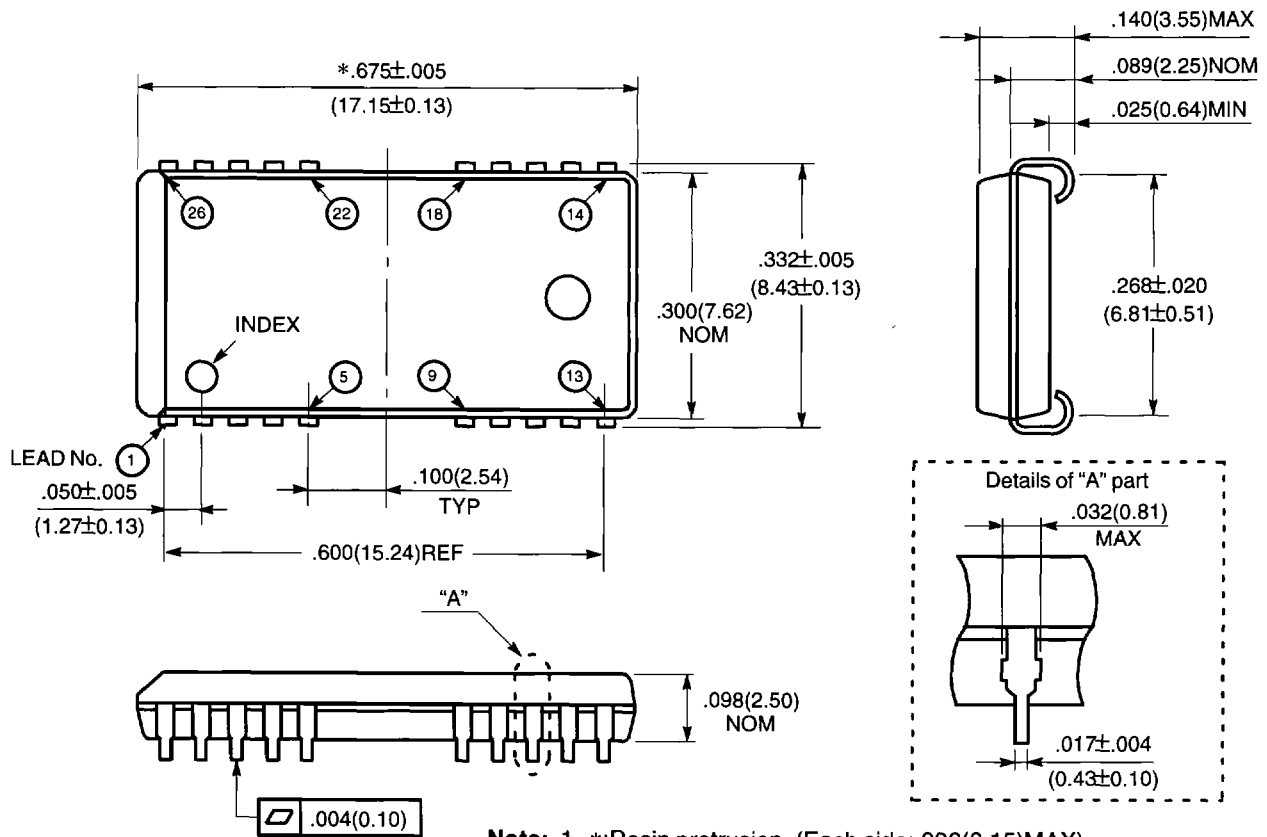
No.	Parameter	Symbol	MB814100A-60L		MB814100A-70L		MB814100A-80L		Unit
			Min	Max	Min	Max	Min	Max	
90	Access Time from $\overline{\text{CAS}}$	t_{FCAC}	—	50	—	55	—	60	ns
91	Column Address Hold Time	t_{FCAH}	30	—	30	—	35	—	ns
92	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t_{FCWD}	50	—	55	—	60	—	ns
93	$\overline{\text{CAS}}$ Pulse Width	t_{FCAS}	50	—	55	—	60	—	ns
94	$\overline{\text{RAS}}$ Hold Time	t_{FRSH}	50	—	55	—	60	—	ns

Note: Assumes that $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh counter test cycle only.

PACKAGE DIMENSIONS

(Suffix: -PJN)

26-LEAD PLASTIC LEADED CHIP CARRIER (CASE No.: LCC-26P-M04)



- Note:**
1. *: Resin protrusion. (Each side: $.006$ (0.15) MAX)
 2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.
 3. Dimensions in inches (millimeters)

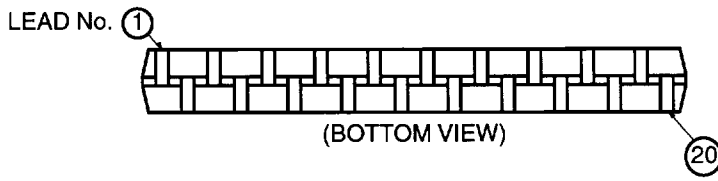
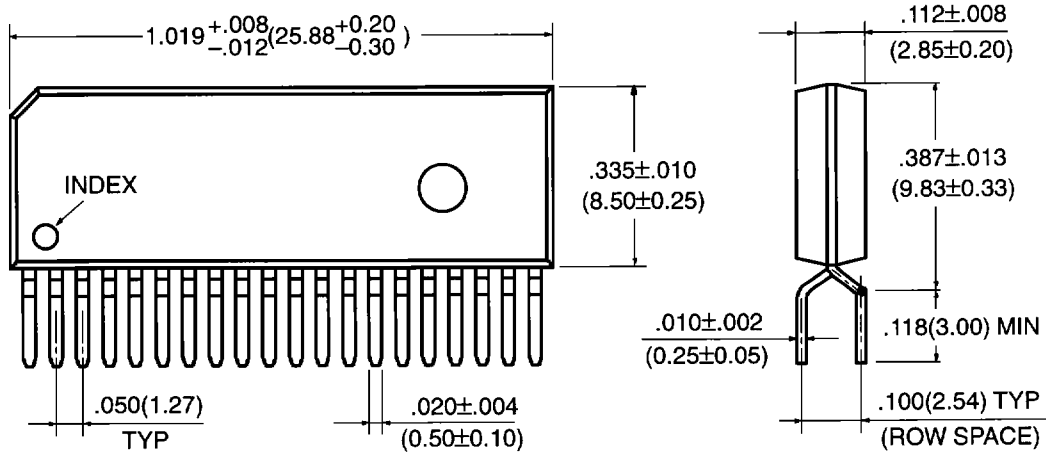
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MB814100A-60L
 MB814100A-70L
 MB814100A-80L

PACKAGE DIMENSIONS (Continued)

(Suffix: -PZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE (CASE No.: ZIP-20P-M02)



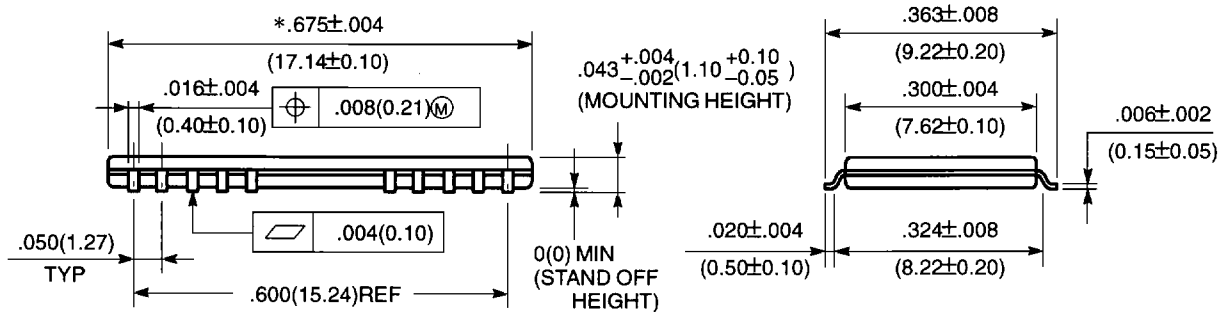
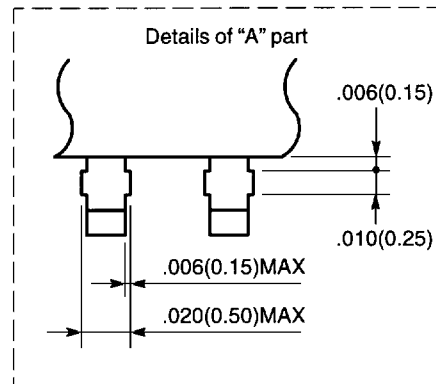
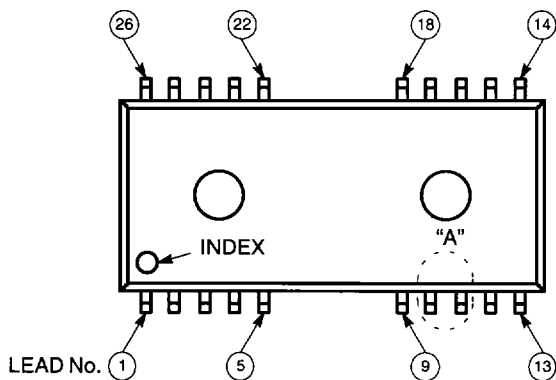
©1991 FUJITSU LIMITED Z20002S-4C

Dimensions in
 inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: -PFTN)

26-LEAD PLASTIC FLAT PACKAGE (CASE No.: FPT-26P-M01)



* : This dimension includes resin protrusion.(Each side : .006(0.15) MAX)

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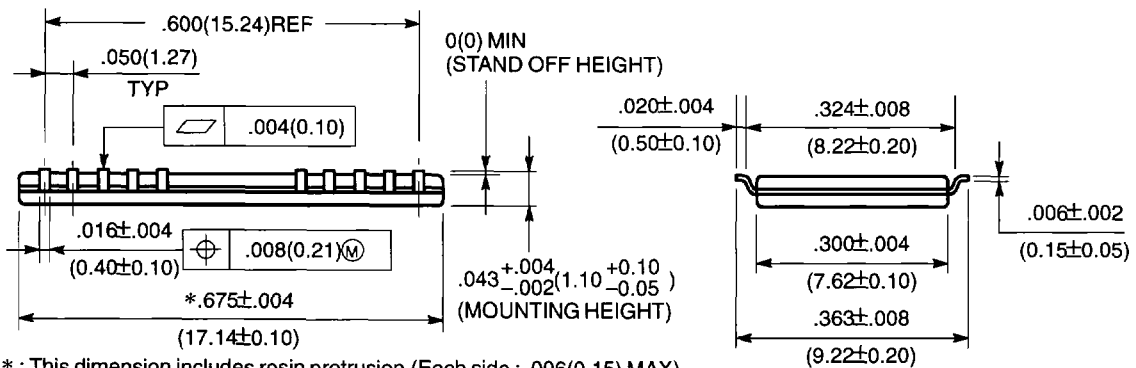
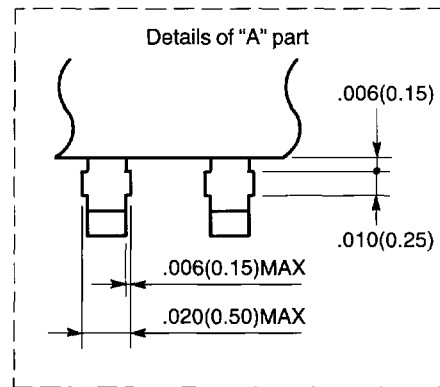
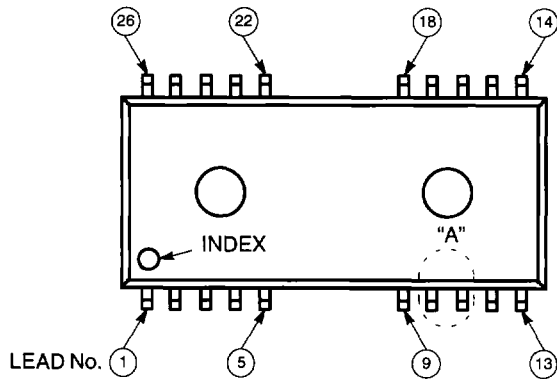
Dimensions in
 inches (millimeters)

MB814100A-60L
 MB814100A-70L
 MB814100A-80L

PACKAGE DIMENSIONS (Continued)

(Suffix: -PFTR)

26-LEAD PLASTIC FLAT PACKAGE (CASE No.: FPT-26P-M02)



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Dimensions in
 inches (millimeters)

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MB814100A-60L
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FUJITSU LIMITED

For further information, please contact:

Japan

FUJITSU LIMITED
Integrated Circuits and Semiconductor Marketing
Furukawa Sogo Bldg.
6-1, Marunouchi 2-chome
Chiyoda-ku, Tokyo 100
Japan
Tel: (03) 3216-3211
Telex: 781-2224361
FAX: (03) 3216-9771

North and South America

FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804 USA
Tel: (408) 922-9000
FAX: (408) 432-9044

Europe

FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
6072 Dreieich-Buchsschlag
Tel: (06103) 690-0
Telex: 411963 fmg d
FAX: (06103) 690-122

Asia

FUJITSU MICROELECTRONICS ASIA PTE LIMITED
51 Bras Basah Road
Plaza by the Park
#06-04/07
Singapore 0718
Tel: 336-1600
Telex: 55373
FAX: 336-1609