MP87091

CMOS 750 KSPS, 12-Bit Analog-to-Digital Converter with Parallel Logic Interface Port

EXAR

FEATURES

- 12-Bit Monotonic ADC
- SNR > 66 dB
- Sampling Frequency ≤ 750 kHz
- Internal Track and Hold
- Single 5 V Supply
- Rail-to-Rail Input Range
- DNL = ±1 LSB, INL = ±2 LSB
- V_{REF} Range: 1.5 V to V_{DD}
- CMOS Low Power: 175 mW (typ)
- 1/4, 1/2 and 3/4 Scale Reference Resistor Taps
- Three-State Outputs
- Binary and Two's Complement Digital Output Mode
- Latch-Up Proof

APPLICATIONS

- Control Systems
- Instrumentation
- DAS
- Sonar

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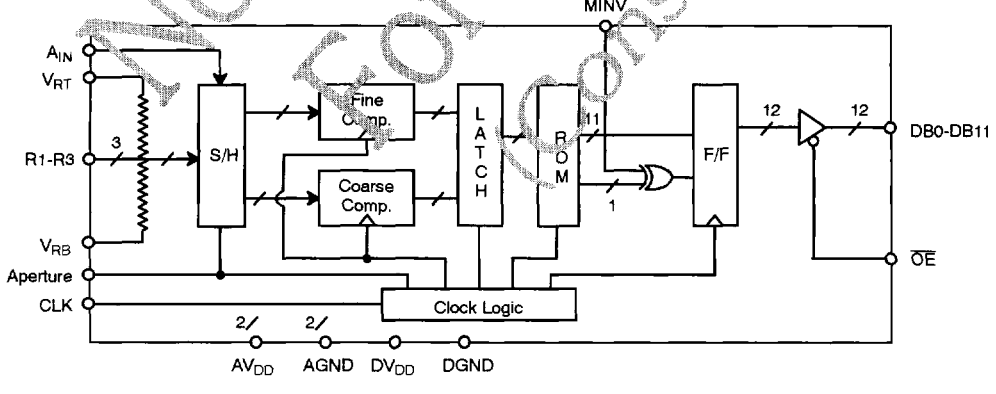
GENERAL DESCRIPTION

The MP87091 is a 750 kHz 12-bit subranging Analog-to-Digital Converter with an an internal track and hold.

The MP87091 operates with a single 5 V supply while consuming less than 175 mW of power (typical). Separate pins for V_{RT} and V_{RB} allow flexibility for various A_{IN} and ΔV_{REF}.

Data is presented at the parallel output port every clock cycle after a 2.5 cycle pipeline delay from sample edge. The digital output port is also equipped with a three-state function. MINV enables binary and 2's complement data formatting. Through pins R1-R3, transfer function adjustment, linearity, and speed enhancement can be accommodated.

SIMPLIFIED BLOCK DIAGRAM

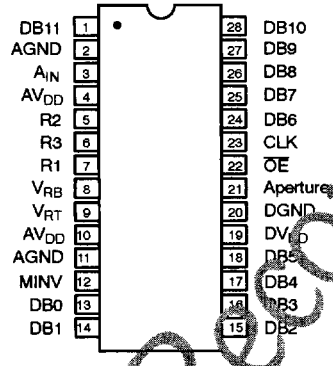


ORDERING INFORMATION

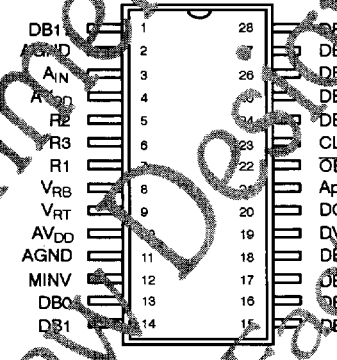
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PDIP	-40 to +85°C	MP87091AN	±1	±2
SOIC	-40 to +85°C	MP87091AS	±1	±2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP (0.600")



28 Pin SOIC (EIAJ, 0.335")

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB11	Data Output Bit 11 (MSB)
2	AGND	Analog Ground
3	A_{IN}	Analog Input
4	AV_{DD}	Analog Power Supply
5	R2	Ref. Resistor Ladder Tap (1/2 V_{REF})
6	R3	Ref. Resistor Ladder Tap (3/4 V_{REF})
7	R1	Ref. Resistor Ladder Tap (1/4 V_{REF})
8	V_{RB}	Bottom Reference
9	V_{RT}	Top Reference
10	AV_{DD}	Analog Power Supply
11	AGND	Analog Ground
12	MINV	Invert MSB (Active High)
13	DB0	Data Output Bit 0 (LSB)
14	DB1	Data Output Bit 1

PIN NO.	NAME	DESCRIPTION
15	DB2	Data Output Bit 2
16	DB3	Data Output Bit 3
17	DB4	Data Output Bit 4
18	DB5	Data Output Bit 5
19	DV_{DD}	Digital Power Supply
20	DGND	Digital Ground
21	Aperture	Delayed Clock, indicates sample point
22	$\overline{OE}$	Output Enable (Active Low)
23	CLK	Clock
24	DB6	Data Output Bit 6
25	DB7	Data Output Bit 7
26	DB8	Data Output Bit 8
27	DB9	Data Output Bit 9
28	DB10	Data Output Bit 10