



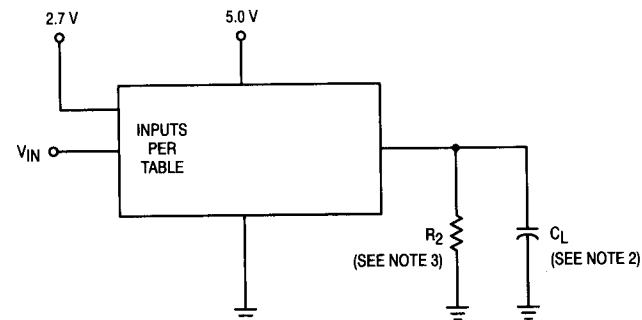
4-Bit Arithmetic Logic Unit

ELECTRICALLY TESTED PER:
MIL-M-38510/33803

The 54F381 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select input codes force the Function outputs to LOW or HIGH. Carry Propagate and Generate outputs are provided for use with the 'F182 Carry Lookahead Generator for high-speed expansion to longer word lengths. For ripple expansion, refer to the 'F382 ALU data sheet.

- Low Input Loading Minimizes Drive Requirements
- Performs Six Arithmetic and Logic Functions
- Selectable Low (Clear) and High (Preset) Functions
- Carry Generate and Propagate Outputs for use with Carry Lookahead Generator

TEST CIRCUIT



NOTES:

1. Pulse generator has the following characteristics:
 $t_r = t_f \leq 2.5$ ns, $PRR \leq 1.0$ MHz, $Z_{OUT} = 50 \Omega$.
2. $C_L = 50$ pF $\pm 10\%$ including scope probe, wiring and stray capacitance, without package in test fixture.
3. $R_L = 499 \Omega \pm 5.0\%$.
4. Voltage measurements are to be made with respect to network ground terminal.
5. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).

Military 54F381



AVAILABLE AS:

- 1) JAN: JM38510/33803BXA
- 2) SMD: 5962-8671001
- 3) 883: 54F381/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2

THE LETTER "M" APPEARS
BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
A ₁	1	1	1	VCC
B ₁	2	2	2	VCC
A ₀	3	3	3	VCC
B ₀	4	4	4	VCC
S ₀	5	5	5	VCC
S ₁	6	6	6	VCC
S ₂	7	7	7	VCC
F ₀	8	8	8	OPEN
F ₁	9	9	9	OPEN
GND	10	10	10	GND
F ₂	11	11	11	OPEN
F ₃	12	12	12	OPEN
G	13	13	13	OPEN
P	14	14	14	OPEN
C _n	15	15	15	VCC
B ₃	16	16	16	VCC
A ₃	17	17	17	VCC
B ₂	18	18	18	VCC
A ₂	19	19	19	VCC
VCC	20	20	20	VCC

BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

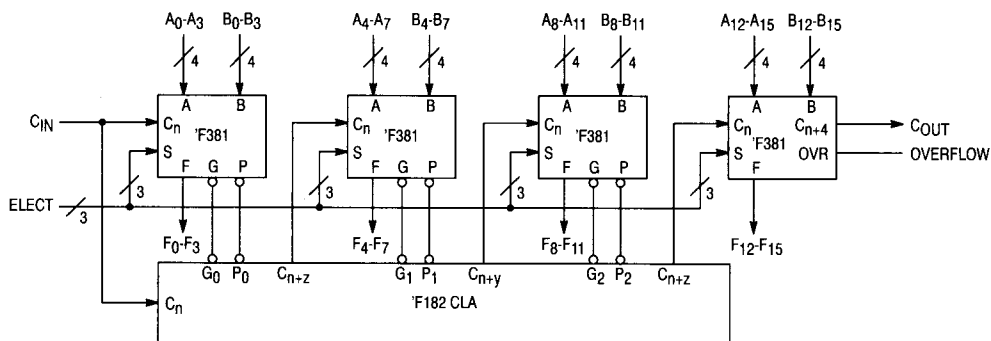
FUNCTIONAL DESCRIPTION

Signals applied to the Select inputs S_0 - S_2 determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Truth Table. The circuit performs the arithmetic functions for either active-HIGH or active-LOW operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a carry (HIGH for active-HIGH

operands, LOW for active-LOW operands) into the C_n input of the least significant package.

The Carry Generate ($\bar{G}$) and Carry Propagate ($\bar{P}$) outputs supply input signals to the 'F182 carry lookahead generator for expansion to longer word length, as shown in Figure 1. Note that an 'F382 ALU is used for the most significant package. Typical delays for Figure 1 are given in Figure 2.

Figure 1. 16-Bit Lookahead Carry ALU Expansion



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FUNCTION SELECT TABLE			
Select			Operation
S_0	S_1	S_2	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	$A \oplus B$
H	L	H	$A + B$
L	H	H	AB
H	H	H	Preset

H = HIGH Voltage Level

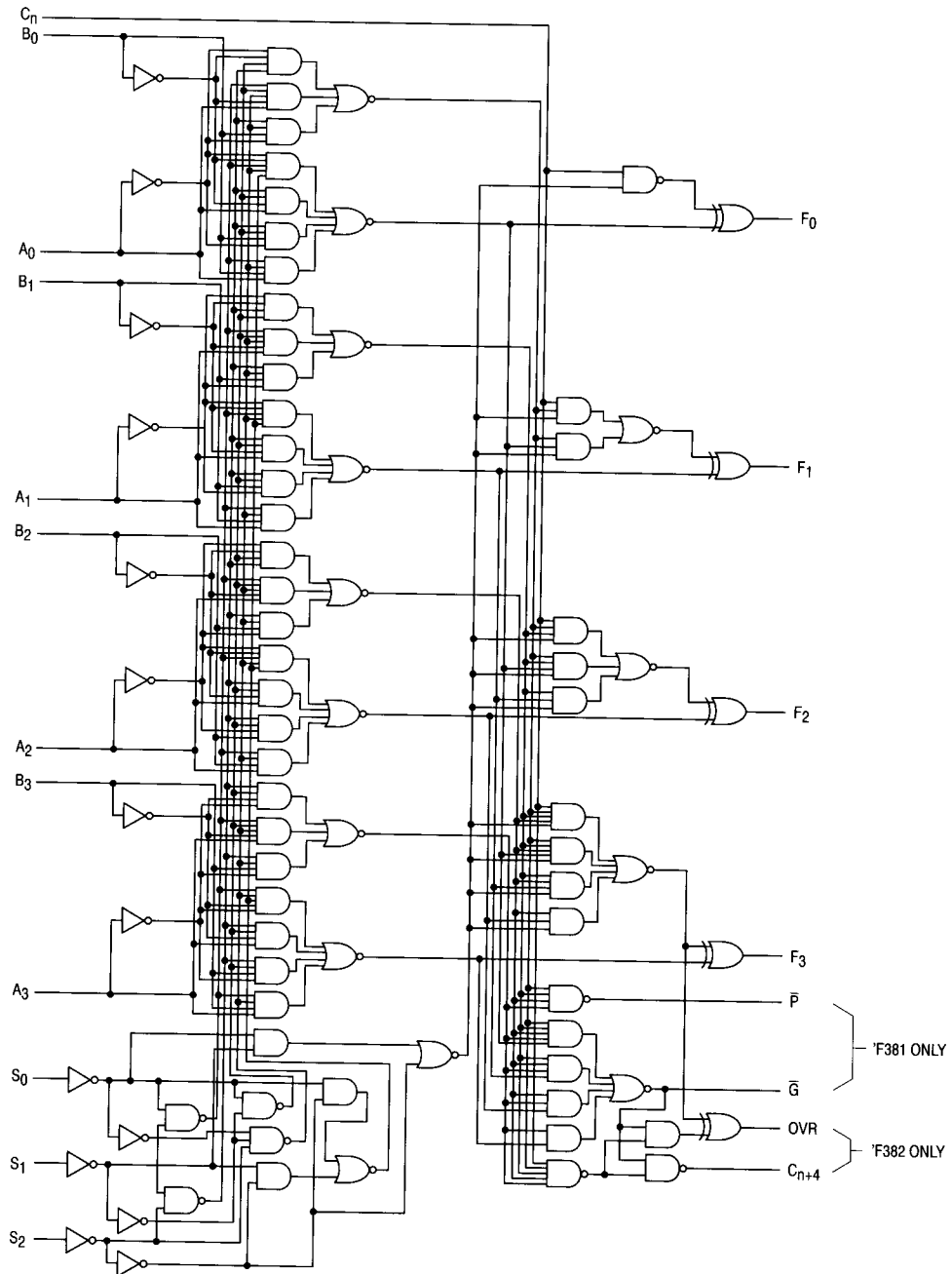
L = LOW Voltage Level

Figure 2. 16-Bit Delay Tabulation

Path Segment	Toward F	Output $C_n + 4$, over
A_1 or B_1 to $\bar{P}$	7.2 ns	7.2 ns
$\bar{P}_1$ to $C_n + J$ ('F182)	6.2 ns	6.2 ns
C_n to F	8.1 ns	—
C_n to $C_n + 4$, over	—	8.0 ns
Total Delay	21.5 ns	21.4 ns

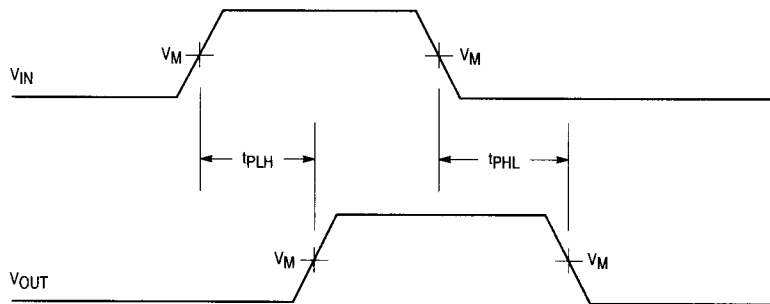
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LOGIC DIAGRAM

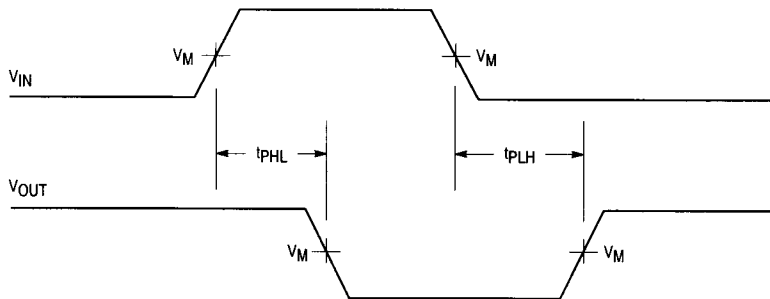


SWITCHING WAVEFORMS

Non-Inverting Waveforms



Inverting Waveforms



$V_M = 1.5 \text{ V}$
 $PRR \leq 1.0 \text{ MHz}$
 $t_r = t_f \leq 2.5 \text{ ns}$
 Input Amplitude (Base $\rightarrow$ Top) = $0 \rightarrow 3.0 \text{ V}$

TRUTH TABLE

Function	Inputs						Outputs					
	S ₀	S ₁	S ₂	C _n	A _n	B _n	F ₀	F ₁	F ₂	F ₃	$\bar{G}$	$\bar{P}$
CLEAR	0	0	0	X	X	X	0	0	0	0	0	0
B MINUS A	1	0	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	1	1	1	0	0
				0	1	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	1	1	1	0	0
				1	1	0	1	0	0	0	1	1
				1	1	1	0	0	0	0	1	0
A MINUS B	0	1	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	0	0	0	1	1
				0	1	0	0	1	1	1	0	0
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	0	0	0	1	1
				1	1	0	1	1	1	1	0	0
				1	1	1	0	0	0	0	1	0
A PLUS B	1	1	0	0	0	0	0	0	0	0	1	1
				0	0	1	1	1	1	1	1	0
				0	1	0	1	1	1	1	1	0
				0	1	1	0	1	1	1	0	0
				1	0	0	1	0	0	0	1	1
				1	0	1	0	0	0	0	1	0
				1	1	0	0	0	0	0	1	0
				1	1	1	1	1	1	1	0	0
A $\oplus$ B	0	0	1	X	0	0	0	0	0	0	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	0
				X	1	1	0	0	0	0	0	0
A + B	1	0	1	X	0	0	0	0	0	0	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0
AB	0	1	1	X	0	0	0	0	0	0	0	0
				X	0	1	0	0	0	0	1	1
				X	1	0	0	0	0	0	0	0
				X	1	1	1	1	1	1	1	0
PRESET	1	1	1	X	0	0	1	1	1	1	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0

1 = HIGH Voltage Level

0 = LOW Voltage Level

X = Immaterial

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = –1.0 mA, V _{IN} = 2.0 V or 0.8 V (all inputs).
V _{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V _{CC} = 4.5 V, I _{OL} = 20 mA, V _{IN} = 0.8 V or 2.0 V (all inputs).
V _{IC}	Input Clamping Voltage		–1.2					V	V _{CC} = 4.5 V, I _{IN} = –18 mA, other inputs are open.
I _{IH}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open.
I _{IHH}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 7.0 V, other inputs are open.
I _{OS}	Output Short Circuit Current	–60	–150	–60	–150	–60	–150	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V, other inputs are GND, V _{OUT} = 0 V.
I _{OD}	Diode Current	60		60		60		mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V (S ₀ , S ₁ , C _n), other inputs are GND, V _{OUT} = 2.5 V.
I _{IL(S)}	Logical "0" Input Current	–0.12	–0.6	–0.12	–0.6	–0.12	–0.6	mA	V _{CC} = 5.5 V, V _{IN} = 0.5 V (S), other inputs are open.
I _{IL}	Logical "0" Input Current	–0.12	–2.4	–0.12	–2.4	–0.12	–2.4	mA	V _{CC} = 5.5 V, V _{IN} = 0.5 V (A, B, & C _n), other inputs are open.
I _{CC}	Power Supply Current Off		89		89		89	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V (all inputs), S = GND.
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			
									per Truth Table with V _{CC} = 4.5 V, (Repeat at), V _{CC} = 5.5 V, V _{INL} = 0.5 V, V _{INH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL1}	Propagation Delay /Data-Output C _N to F _N	2.5	8.0	2.5	12	2.5	12	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PLH1}	Propagation Delay /Data-Output C _N to F _N	2.5	12	2.5	15	2.5	15	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PHL2}	Propagation Delay /Data-Output A _N to F _N	3.0	12.5	3.0	15	3.0	15	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PLH2}	Propagation Delay /Data-Output A _N to F _N	3.0	15	3.0	17	3.0	17	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PHL3}	Propagation Delay /Data-Output B _N to F _N	3.0	12.5	3.0	16	3.0	16	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PLH3}	Propagation Delay /Data-Output B _N to F _N	3.0	15	3.0	17	3.0	17	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PHL4}	Propagation Delay /Data-Output S _N to F _N	3.0	14	3.0	16	3.0	16	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PLH4}	Propagation Delay /Data-Output S _N to F _N	3.0	20	3.0	21	3.0	21	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PHL5}	Propagation Delay /Data-Output A _N to $\overline{G}$	3.0	10	3.0	13.5	3.0	13.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PLH5}	Propagation Delay /Data-Output A _N to $\overline{G}$	3.0	11.5	3.0	13.5	3.0	13.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PHL6}	Propagation Delay /Data-Output B _N to $\overline{G}$	3.0	10	3.0	13.5	3.0	13.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PLH6}	Propagation Delay /Data-Output B _N to $\overline{G}$	3.0	11.5	3.5	13	3.5	13	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PHL7}	Propagation Delay /Data-Output A _N to $\overline{P}$	3.0	9.5	3.0	12.5	3.0	12.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PLH7}	Propagation Delay /Data-Output A _N to $\overline{P}$	2.0	11	2.0	14	2.0	14	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL8}	Propagation Delay /Data-Output B _n to $\bar{P}$	3.0	9.5	3.0	12.5	3.0	12.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PLH8}	Propagation Delay /Data-Output B _n to $\bar{P}$	2.0	11	2.0	14	2.0	14	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PHL9}	Propagation Delay /Data-Output S _n to $\bar{G}$	3.0	13.5	3.0	18	3.0	18	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PLH9}	Propagation Delay /Data-Output S _n to $\bar{G}$	3.0	14	3.0	17	3.0	17	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PHL10}	Propagation Delay /Data-Output S _n to $\bar{P}$	3.0	13.5	3.0	18	3.0	18	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PLH10}	Propagation Delay /Data-Output S _n to $\bar{P}$	3.0	14	3.0	16	3.0	16	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.