IM6653/IM6654
4096-Bit CMOS UV EPROM

GENERAL DESCRIPTION

The Intersil IM6653 and IM6654 are fully decoded 4096 bit CMOS electrically programmable ROMs (EPROMs) fabricated with Intersil's advanced CMOS processing technology. In all static states these devices exhibit the microwatt power dissipation typical of CMOS. Inputs and three-state outputs are TTL compatible and allow for direct interface with common system bus structures. On-chip address registers and chip select functions simplify system interfacing requirements.

The IM6653 and IM6654 are specifically designed for program development applications where rapid turn-around for program changes is required. The devices may be erased by exposing their transparent lids to ultra-violet light, and then re-programmed.

FEATURES

- **Organization — IM6653: 1024 x 4**
  IM6654: 512 x 8
- **Low Power — 770μW Maximum Standby**
- **High Speed**
  - 300ns 10V Access Time For IM6653/54 AI
  - 450ns 5V Access Time For IM6653/54-1I
- **Single +5V Supply Operation**
- **UV Erasable**
- **Synchronous Operation For Low Power Dissipation**
- **Three-State Outputs and Chip Select for Easy System Expansion**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IM6653/4IJG	-40°C to +85°C	24-Pin CERDIP
IM6653/4-1IJG	-40°C to +85°C	24-Pin CERDIP
IM6653/4AIJG	-40°C to +85°C	24-Pin CERDIP
IM6653/4MJG*	-55°C to +125°C	24-Pin CERDIP
IM6653/4AMJG*	-55°C to +125°C	24-Pin CERDIP

* Add /HR for HiRel processing

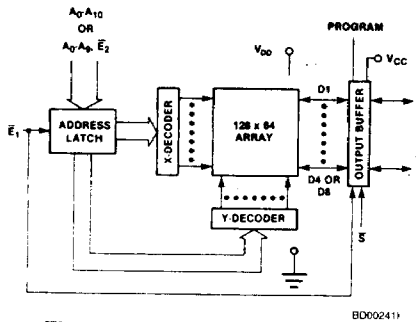

Figure 1: Functional Diagram

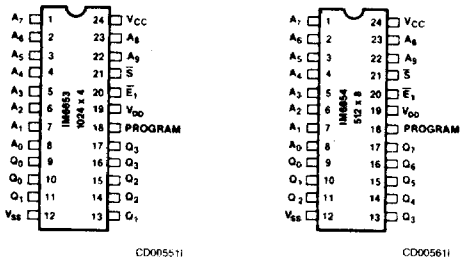

Figure 2: Pin Configurations

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Note: All typical values have been guaranteed by characterization and are not tested.

IM6653/IM6654

ABSOLUTE MAXIMUM RATINGS (IM6653/54 I, -1I, M)

Supply Voltages
- $V_{DD} - V_{SS}$ ..... +8.0V
- $V_{CC} - V_{SS}$ ..... +8.0V

Input or Output Voltage ....(V_{SS} -0.3V) to (V_{DD} +0.3V)

Operating Range Range (T_A)
- Industrial ..... -40°C to +85°C
- Military ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = V_{DD} = 5V \pm 10\%$ $V_{SS} = 0V$, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	IM6653/54I, -1I, M		UNIT
			MIN	MAX	
V_{IH}	Logical "1" Input Voltage	$\overline{E}_1$, $\overline{S}$	V_{DD} - 2.0		V
V_{IH}		Address Pins	2.7		
V_{IL}	Logical "0" Input Voltage			0.8	
I_I	Input Leakage	$GND \le V_{IN} \le V_{DD}$	-1.0	1.0	µA
V_{OH}	Logical "1" Output Voltage	$I_{OH} = -0.2mA$	2.4		V
V_{OL}	Logical "0" Output Voltage	$I_{OL} = 2.0mA$		0.45	
I_{OLK}	Output Leakage	$GND \le V_O \le V_{CC}$	-1.0	1.0	µA
I_{STBY}	Standby Supply Current	$V_{IN} = V_{DD}$		100	
I_{CC}		$V_{IN} = V_{DD}$		40	
I_{DD}	Operating Supply Current (1)	f = 1MHz		6	mA
C_I	Input Capacitance	Note 1		7.0	pF
C_O	Output Capacitance	Note 1		10.0	

Note: 1. For design reference only, not 100% tested.

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = V_{DD} = 5V \pm 10\%$ $V_{SS} = 0V$, $C_L = 50pf$, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	IM6653/54-1I		IM6653/54 I		IIM6653/54 M		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
TE_1LQV	Access Time From $\overline{E}_1$		450		550		600	ns
TSLQV	Output Enable Time		110		140		150	
TE_1HQZ	Output Disable Time		110		140		150	
TE_1HE_1L	$\overline{E}_1$ Pulse Width (Positive)	130		150		150		
TE_1LE_1H	$\overline{E}_1$ Pulse Width (Negative)	450		550		600		
$TAVE_1L$	Address Setup Time	0		0		0		
TE_1LAX	Address Hold Time	80		100		100		
TE_2VE_1L	Chip Enable Setup Time (6654)	0		0		0		
TE_1LE_2X	Chip Enable Hold Time (6654)	80		100		100		

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS (IM6653/54AI, AM)

Supply Voltages
- $V_{DD} - V_{SS}$ ..... +11.0V
- $V_{CC} - V_{SS}$ ..... +11.0V

Input or Output Voltage ....(V_{SS} −0.3V) to (V_{DD} +0.3V)

Operating Temperature Range
- Industrial .....−40°C to +85°C
- Military .....−55°C to +125°C

Storage Temperature Range .....−65°C to +150°C

Lead Temperature (Soldering, 10sec) .....300°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = V_{DD} = 4.5V$ to $10.5V$ $V_{SS} = 0V$, T_A = Operational Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	IM6653/54AI, AM		UNIT
			MIN	MAX	
V_{IH}	Logical "1" Input Voltage	$\overline{E}_1$, $\overline{S}$	V_{DD} − 2.0		V
V_{IH}		Address Pins	V_{DD} − 2.0		
V_{IL}	Logical "0" Input Voltage			0.8	
I_I	Input Leakage	$GND \le V_{IN} \le V_{DD}$	−1.0	1.0	μA
V_{OH}	Logical "1" Output Voltage	$I_{OUT} = 0$ (Note 1)	V_{CC} − 0.01		V
V_{OL}	Logical "0" Output Voltage	$I_{OUT} = 0$ (Note 1)		V_{SS} + 0.01	
I_{OLK}	Output Leakage	$V_{SS} \le V_O \le V_{CC}$	−1.0	1.0	μA
I_{STBY}	Standby Supply Current	$V_{IN} = V_{DD}$		100	
I_{CC}		$V_{IN} = V_{DD}$		40	
I_{DD}	Operating Supply Current	f = 1MHz		12	mA
C_I	Input Capacitance	Note 1		7.0	pF
C_O	Output Capacitance	Note 1		10.0	

Note: 1. For design reference only, not 100% tested.

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = V_{DD} = 10V$ ±5% $V_{SS} = 0V$, $C_L = 50pf$, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	IM6653/54 AI		IM6653/54 AM		UNIT
		MIN	MAX	MIN	MAX	
TE_1LQV	Access Time From $\overline{E}_1$		300		350	ns
TSLQV	Output Enable Time		60		70	
TE_1HQZ	Output Disable Time		60		70	
TE_1HE_1L	$\overline{E}_1$ Pulse Width (Positive)	125		125		
TE_1LE_1H	$\overline{E}_1$ Pulse Width (Negative)	300		350		
$TAVE_1L$	Address Setup Time	0		0		
TE_1LAX	Address Hold Time	60		60		
TE_2VE_1L	Chip Enable Setup Time (6654)	0		0		
TE_1LE_2X	Chip Enable Hold Time (6654)	60		60		

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Note: All typical values have been guaranteed by characterization and are not tested.

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PIN ASSIGNMENTS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1-8,23	A_0-A_7,A_8	–	Address Lines
9-11, 13-17	Q_0-Q_7 Q_0-Q_3	– –	Data Out lines, 6654 Data Out lines, 6653
12	V_{SS}	–	Negative Supply
18	Program	–	Programming pulse input
19	V_{DD}	–	Chip positive supply, normally tied to V_{CC}
20	$\overline{E}_1$	L	Strobe line, latches both address lines and, for 6654, Chip enable $\overline{E}_2$
21	$\overline{S}$	L	Chip select line, must be low for valid data out
22	A_9 $\overline{E}_2$	– L	Additional address line for 6653 Chip enable line, latched by Chip enable $\overline{E}_1$ on 6654
24	V_{CC}	–	Output buffer positive supply

READ MODE OPERATION

In a typical READ operation address lines and chip enable $\overline{E}_2$* are latched by the falling edge of chip enable $\overline{E}_1$ (T = 0). Valid data appears at the outputs one access time (TELQV) later, provided level-sensitive chip select line $\overline{S}$ is low (T = 3). Data remains valid until either $\overline{E}_1$ or $\overline{S}$ returns to a high level (T = 4). Outputs are then forced to a high-Z state.

Address lines and $\overline{E}_2$ must be valid one setup time before (TAVEL), and one hold time after (TELAX), the falling edge of $\overline{E}_1$ starting the read cycle. Before becoming valid, Q output lines become active (T = 2). The Q output lines return to a high-Z state one output disable time (TE_1HQZ) after any rising edge on $\overline{E}_1$ or $\overline{S}$.

The program line remains high throughout the READ cycle.

Chip enable line $\overline{E}_1$ must remain high one minimum positive pulse width (TEHEL) before the next cycle can begin.

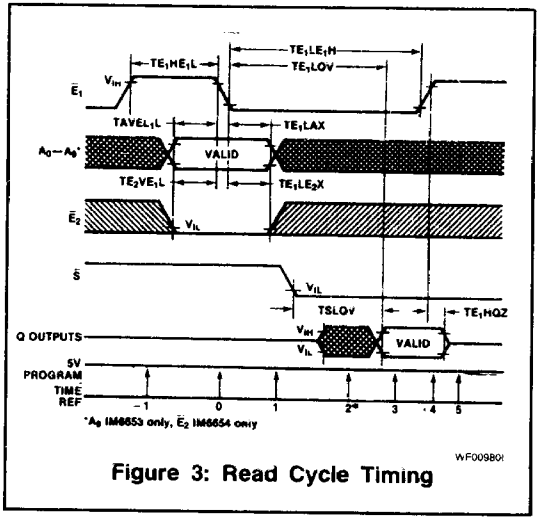

Figure 3: Read Cycle Timing

FUNCTION TABLE

TIME REF	INPUTS				OUTPUTS Q	NOTES
	$\overline{E}_1$	$\overline{E}_2$	$\overline{S}$	A		
–1	H	X	X	X	Z	DEVICE INACTIVE
0	↘	L	X	V	Z	CYCLE BEGINS: ADDRESSES, $\overline{E}_2$ LATCHED*
1	L	X	X	X	Z	INTERNAL OPERATIONS ONLY
2	L	X	L	X	A	OUTPUTS ACTIVE UNDER CONTROL OF $\overline{E}_1$, $\overline{S}$
3	L	X	L	X	V	OUTPUTS VALID AFTER ACCESS TIME
4	↗	X	L	X	V	READ COMPLETE
5	H	X	X	X	Z	CYCLE ENDS (SAME AS –1)

Note: All typical values have been guaranteed by characterization and are not tested.

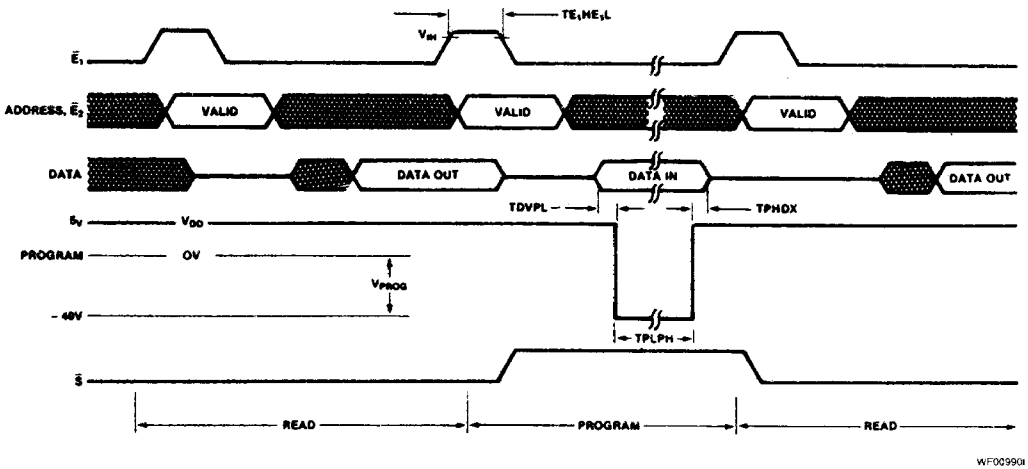

Figure 4: Read and Program Cycle Timing

DC CHARACTERISTICS FOR PROGRAMMING OPERATION

($V_{CC} = V_{DD} = 5V \pm 5\%$ $V_{SS} = 0V$, $T_A = 25°C$)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PROG}	Program Pin Load Current			80	100	mA
V_{PROG}	Programming Pulse Amplitude		-38	-40	-42	V
I_{CC}	V_{CC} Current			0.1	5	mA
I_{DD}	V_{DD} Current			40	100	
V_{IHA}	Address Input High Voltage		$V_{DD}-2.0$			V
V_{ILA}	Address Input Low Voltage				0.8	
V_{IH}	Data Input High Voltage		$V_{DD}-2.0$			
V_{IL}	Data Input Low Voltage				0.8	

AC CHARACTERISTICS FOR PROGRAMMING OPERATION

($V_{CC} = V_{DD} = 5V \pm 5\%$ $V_{SS} = 0V$, $T_A = 25°$)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPLPH	Program Pulse Width	$t_{rise} = t_{fall} = 5\mu s$	18	20	22	ms
	Program Pulse Duty Cycle				75%	
TDVPL	Data Setup Time		9			µs
TPHDX	Data Hold Time		9			
TE_1HE_1L	Strobe Pulse Width		150			ns
$TAVE_1L$	Address Setup Time		0			
TE_1LE_1X	Address Hold Time		100			
TE_1LQV	Access Time				1000	

PROGRAM MODE OPERATION

Initially, all 4096 bits of the EPROM are in the logic one (output high) state. Selective programming of proper bit locations to "0"s is performed electrically.

In the PROGRAM mode for all EPROMs, V_{CC} and V_{DD} are tied together to a +5V operating supply. High logic levels at all of the appropriate chip inputs and outputs must be set at V_{DD} -2V minimum. Low logic levels must be set at V_{SS} +0.8V maximum. Addressing of the desired location in PROGRAM mode is done as in the READ mode. Address and data lines are set at the desired logic levels, and PROGRAM and chip select ($\overline{S}$) pins are set high. The address is latched by the downward edge on the strobe line ($\overline{E}_1$). During valid DATA IN time, the PROGRAM pin is pulsed from V_{DD} to -40V. This pulse initiates the program-

Note: All typical values have been guaranteed by characterization and are not tested.

ming of the device to the levels set on the data outputs. Duty cycle limitations are specified from chip heat dissipation considerations. PULSE RISE AND FALL TIMES MUST NOT BE FASTER THAN 5μs.

Intelligent programmer equipment with successive READ/PROGRAM/VERIFY sequences is recommended.

PROGRAMMING SYSTEM CHARACTERISTICS

1. During programming the power supply should be capable of limiting peak instantaneous current to 100mA.
2. The programming pin is driven from V_{DD} to −40 volts (±2V) by pulses of 20 milliseconds duration. These pulses should be applied in the sequence shown in the flow chart. Pulse rise and fall times of 10 microseconds are recommended. Note that any individual location may be programmed at any time.
3. Addresses and data should be presented to the device within the recommended setup/hold time and high/low logic level margins. Both "A" (10V) and non "A" EPROMs are programmed at V_{CC}, V_{DD} of 5V ±5%.
4. Programming is to be done at room temperature.

ERASING PROCEDURE

The IM6653/54 are erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose (i.e., UV intensity x exposure time) is 10W sec/cm^2. The lamps should be used without short-wave filters, and the IM6653/54 to be erased should be placed about one inch away from the lamp tubes. For best results it is recommended that the device remain inactive for 5 minutes after erasure, before reprogramming.

The erasing effect of UV light is cumulative. Care should be taken to protect EPROMs from exposure to direct sunlight or fluorescent lamps radiating UV light in the 2000Å to 4000Å range.

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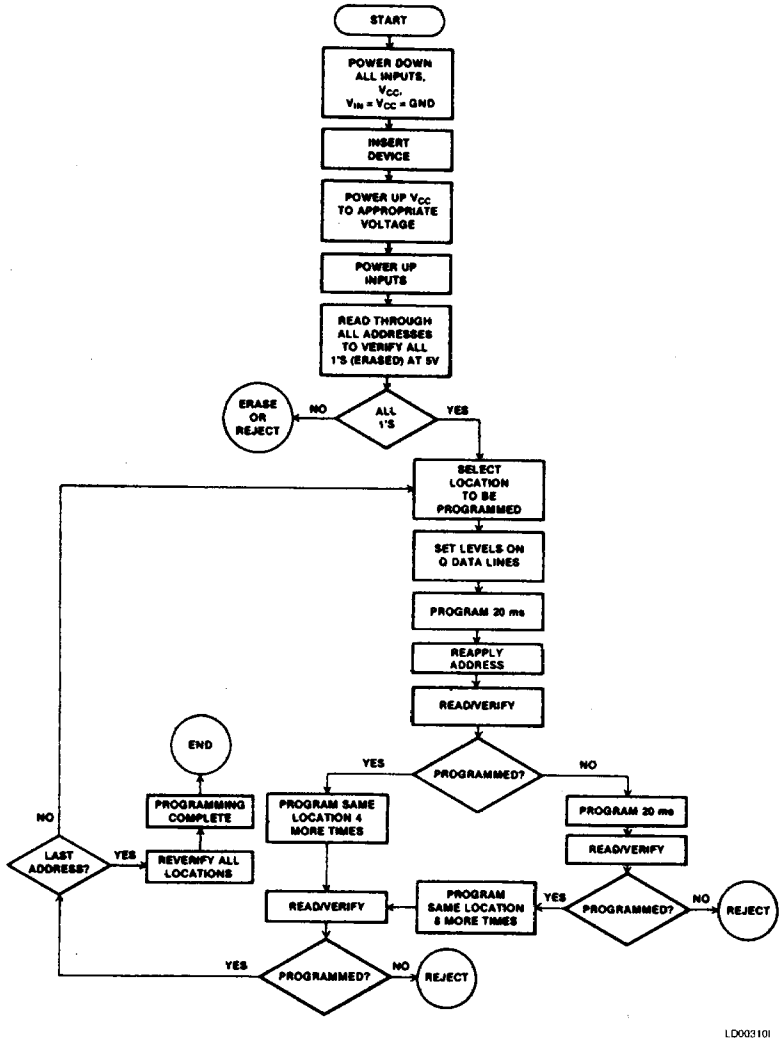

Figure 5: Programming Flow Chart

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Note: All typical values have been guaranteed by characterization and are not tested.

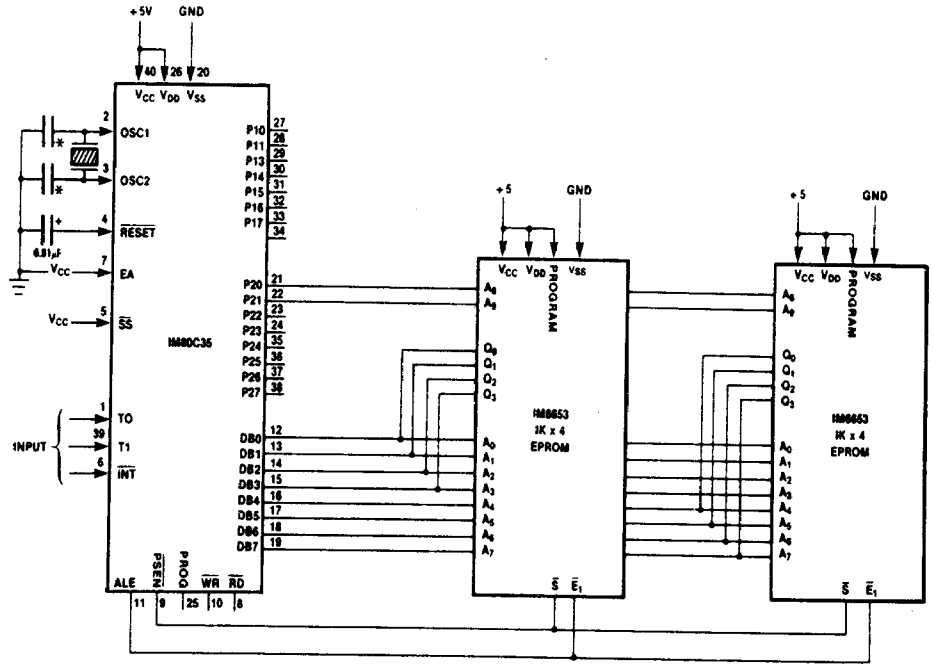

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Figure 6: IM6653 CMOS EPROMS as External Program Memory with the IM80C35

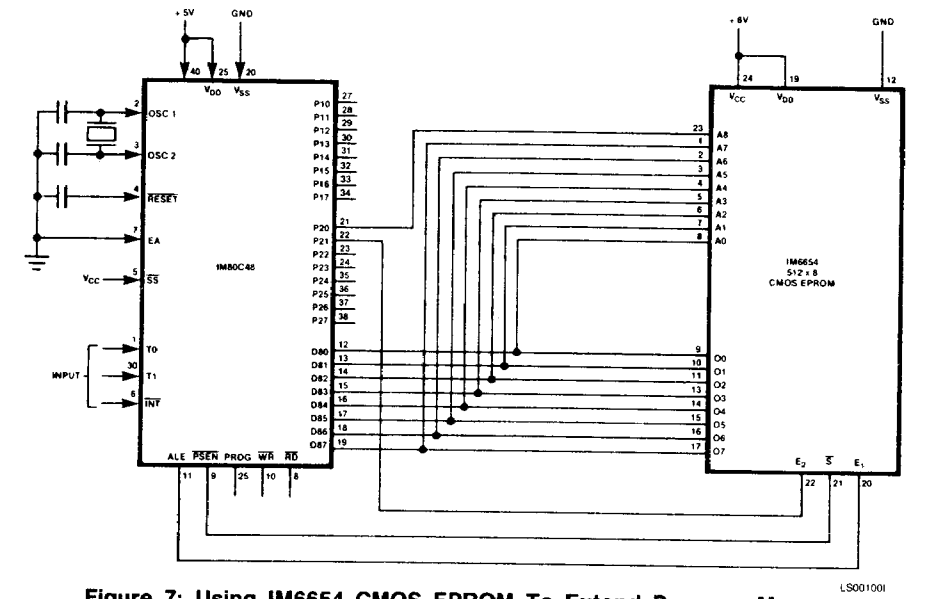

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Figure 7: Using IM6654 CMOS EPROM To Extend Program Memory

Note: All typical values have been guaranteed by characterization and are not tested.