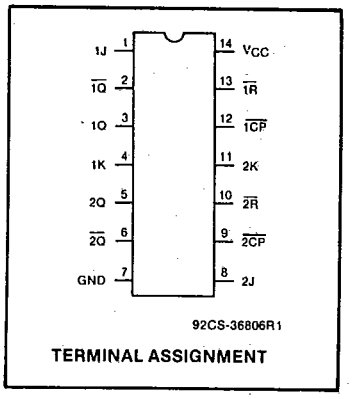
CD54/74HC107
CD54/74HCT107

Dual J-K Flip-Flop with Reset
Negative Edge Trigger



TERMINAL ASSIGNMENT

TRUTH TABLE

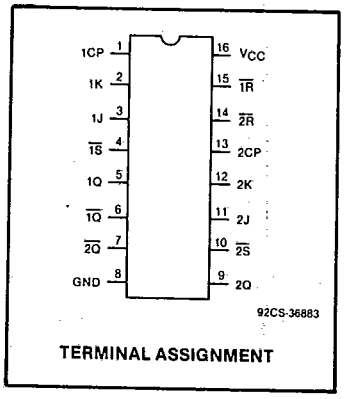
INPUTS				OUTPUTS	
$\overline{R}$	CP	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	QO	QO
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	QO	QO

Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, t_r, $t_f = 6$ ns

Symbol	Parameter	Test Conditions	Typical	Units
t_{PHL}/t_{PLH}	Propagation Delay: Clock to Q or $\overline{Q}$	$C_L = 15$ pF $C_L = 50$ pF	18 20	ns ns
f_{max}	Maximum Clock Frequency	$C_L = 15$ pF $C_L = 50$ pF	60 50	MHz MHz

CD54/74HC112
CD54/74HCT112

Dual J-K Flip-Flop with Set and Reset
Negative Edge Trigger



TERMINAL ASSIGNMENT

TRUTH TABLE

Inputs					Outputs	
$\overline{S}$	$\overline{R}$	CP	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0

*This is an unstable condition, and is not guaranteed.

Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, t_r, $t_f = 6$ ns

Symbol	Parameter	Test Conditions	Typical	Units
t_{PHL}/t_{PLH}	Propagation Delay: Clock to Q	C_L = 15 pF C_L = 50 pF	18 20	ns ns
f_{max}	Maximum Clock Frequency	C_L = 15 pF C_L = 50 pF	60 50	MHz MHz