Rockwell

MOS/LSI TELECOMMUNICATIONS DEVICES
DATA SHEET

Dual Tone Multi-Frequency Detector

Digital range filter detects all 16 Touch Tone® signal combinations

Detects a tone pair in 22 ms to 39 ms

Digital logic impervious to frequency or bandwidth drift caused by time, temperature, or voltage

Automatic internal reset when no tones are present

Variable pulsewidth Strobe output provides increased talk-off protection

Binary or 2-of-8 coded outputs option

Inputs/outputs can be left floating when not used

Single or dual power supply option

On-chip oscillator — 3.579545 MHz color-burst crystal

Central-office-quality detection

Excellent talk-off protection — As little as one hit on Mitel test tape (CM 7290)

DTMF Signaling and Receivers

Dual-Tone Multi-Frequency (DTMF) or Touch-Tone® signaling has made telephone communication faster, more efficient and more convenient than dial pulse signaling. Touch-Tone® telephone instruments or automatic dialers generate a tone pair representing the "dialed" number and send them over the lines to a receiver which detects the tones and reliably identifies the number. DTMF signals are defined by a 4 x 4 audio tone matrix as illustrated in figure 1. Each digit is represented by one tone from the low-group and one tone from the high-group. These non-harmonically related frequencies protect the message against false-keying by stray signals and voice-generated tones.

A DTMF receiver must recognize the dual tones within a certain bandwidth while tolerating dial tone, noise, input amplitude variation and "twist" or amplitude differential between the two tones. In addition, the receiver has to comply with timing restrictions imposed by the DTMF generation process and meet other specific requirements of the particular application.

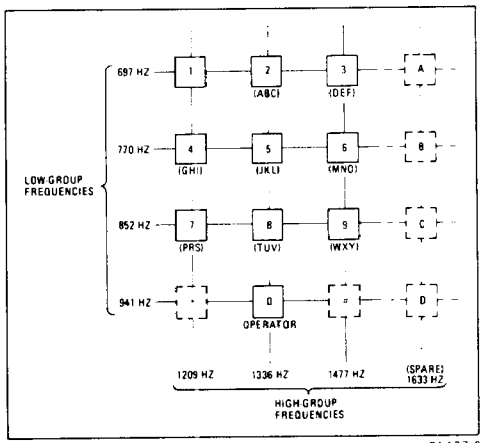

Figure 1. Touch Tone® Pad (Dual Tone Multi Frequency Signaling)

CRC 8030 General Description

The CRC 8030 provides a low-cost and high-performance solution for DTMF detection. Utilizing a unique digital filter algorithm, the patented* CRC 8030 performs the key critical functions of a DTMF receiver. When used in conjunction with a front-end band-split filter/limiter, the CRC 8030 implements a complete DTMF receiver (figure 2). This design approach provides the optimum technological benefits of analog and digital design techniques.

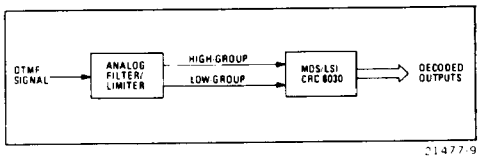

Figure 2. DTMF Receiver Utilizing CRC 8030

® Registered trademark of AT&T

*U.S. Patent No. 4016371

The exact requirements for the front-end filter/limiter vary with the particular receiver application. For example, high quality central office receivers require a more selective front-end filter. Conversely, low-noise environment keyphone systems can use a less stringent front-end filter design.

DTMF receivers historically have been implemented with all-analog filtering techniques, i.e., phase-locked loops, LC filters and active filters. Compared to a phase-locked-loop receiver, the CRC 8030 provides much superior performance. Compared to LC or active filter receivers, the CRC 8030 can be manufactured for a significantly lower cost while providing improved performance. The CRC 8030 provides the economy, performance, size and reliability benefits of digital MOS/LSI. The CRC 8030 is packaged in a 28-pin DIP.

Applications

The CRC 8030 can be applied to all systems requiring DTMF detection. This includes the traditional telephony systems: keyphone, PABX, central office, intercom and mobile radio communications. Other applications include computer signaling and control systems. Where it is necessary to interface with a dial pulse system, the CRC 8030 and the CRC 8000 (a Binary-to-Dial-Pulse Dialer) implement a DTMF-to-dial-pulse conversion system.

The CRC 8030 has been functionally designed to provide optimum performance for a wide variety of DTMF detection applications.

Operation

The CRC 8030 is a DTMF detector implemented with PMOS ion-implantation processing. This detector accepts group-filtered and square-shaped DTMF frequencies and converts them to binary data or 2-of-8 coded data in 22 ms to 39 ms; out-of-tolerance frequencies are rejected. The device ignores the first few pulses of the input signal in order to prevent errors in detection due to the transients from the Touch-Tone® pad. The signal is then analyzed several times by a digital range filter prior to being accepted as valid. As soon as the range filter has recognized a frequency below 1680 Hz, the Audio Detect (AUD) output is enabled. This output provides the user with a signal for controlling the limiter gain at the receiver front-end. A Strobe (ST) output indicates when the output data are valid.

Once a digit is accepted as valid, the CRC 8030 will ignore any change in tone frequency until either the high-group or low-group tone disappears for more than 10 ms. When this occurs, the device is reset internally and will be ready to accept another Touch-Tone® digit. This feature provides immunity to frequency drift that could be caused by Doppler shift. Should a frequency in either the high- or low-group disappear for less than 10 ms, the gap is bridged resulting in only one digit.

A block diagram of the CRC 8030 is shown in figure 3. The functions include timebase generation, wave shaping circuitry, range counters with correlation circuitry, and the output timing and decoding functions.

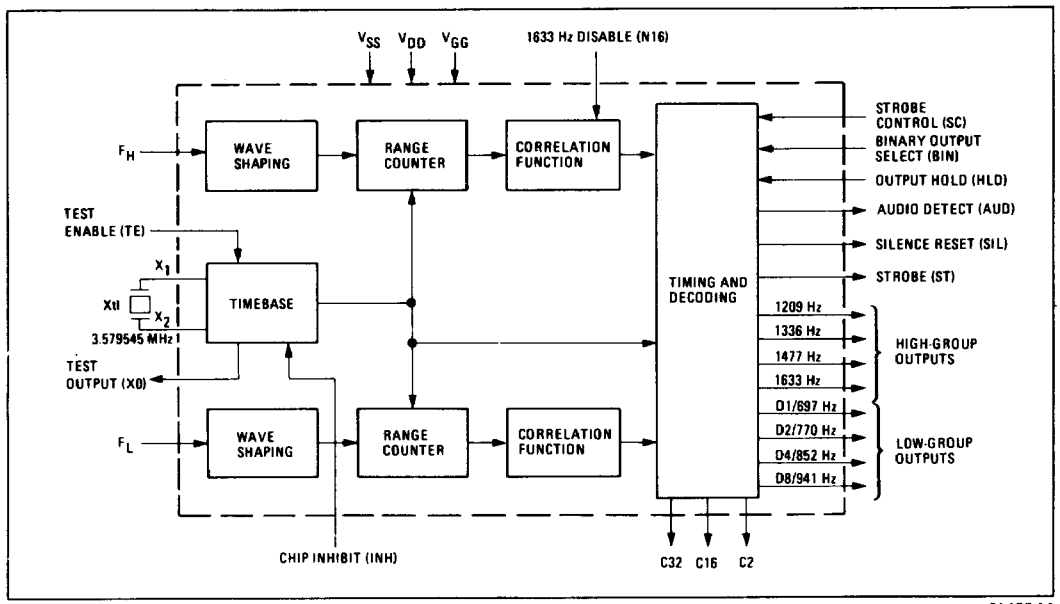

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Figure 3. CRC 8030 Block Diagram.

Technical Characteristics

Maximum Ratings: Non-operating voltages with no damage to device —

Supply Voltage V_{DD} . . . . . V_{SS} -8.0V
Supply Voltage V_{GG} . . . . . V_{SS} -21.0V
Positive Voltage on any pin . . . . . V_{SS} +0.3V
Negative Voltage on any pin . . . . . V_{SS} -20.0V

Power Dissipation ($0^{o}C \leq T_A \leq 70^{o}C$) . . . . . 200 mW
Operating Temperature Range (case) . . . 0^{o} to $+70^{o}C$*
Storage Temperature Range (case) . . $-65^{o}C$ to $+150^{o}C$

*An extended temperature range device will be available in the future.

Inputs and Outputs

The inputs and outputs are illustrated in figure 3 and are described below with a positive logic convention assumed. However, the operation is defined such that when a 2-of-8 output format is chosen, the Strobe and the low-group outputs display data with a negative logic convention. The high-group outputs always display data in a negative logic convention. Detailed timing is shown in the timing diagram, figure 4.

Inputs

Logic levels are MOS compatible. Inputs BIN, INH, HLD, SC, N16, and TE have on-chip active pull-up devices to V_{SS} with a minimum of 50 KΩ resistance; therefore, no connection is required to these pins if a high-level input is desired.

- High- and low-group DTMF signals (FL, FH) — These are the filtered and square-shaped DTMF tones. When no signal is present, both input levels should be low (most negative level).
- Binary Output Select (BIN) — If this input is low (most negative level), the decoded outputs are displayed in a binary format and Strobe (ST) pulses from a normally low state to a high state (figure 4). If this input is high or open, the decoded outputs are displayed in a 2-of-8 code and Strobe pulses from a normally high state to a low state.
- Chip Inhibit (INH) — If this input is low, the device is inhibited from decoding any DTMF tones. When decoding binary, the outputs stay low. When decoding 2-of-8, the outputs stay high. If this input is high or open, the outputs function normally. Chip Inhibit is also a master reset except for the output data registers when Output Hold is low.
- Output Hold (HLD) — If this input is low, the output data, if valid, are stored in the output registers. If the input is high or open, the outputs will function normally.
- Strobe Control (SC) — This input controls the pulsewidth of the Strobe (ST) output.

  When Strobe Control is high or open, the signal is analyzed for the full 39 ms data acquisition (t_{DA1}, Long Strobe) period. If the input tone-pair is detected within 22 ms, then the Strobe (ST) output pulsewidth is at a maximum of 17 ms. If detection takes more than 22 ms, the Strobe pulsewidth is reduced by the extra time needed for detection. If the signal is detected after the 39 ms period, no Strobe pulse will occur.

  When Strobe Control is low, the input signal is analyzed for a 33 ms period (t_{DA2}, Short Strobe). If the tone is detected within 25 ms after its inception, then the Strobe pulsewidth is 8 ms. If detection occurs after 25 ms, then the Strobe pulsewidth is reduced by the lag time. If no signal is detected within the 33 ms period, no Strobe pulse will occur.

  When a Short Strobe is selected, a higher quality input signal must be present in order to be accepted as a valid signal. Thus, voice or noise signals on the telephone line, which require a longer detection time, will be ignored by the chip. As a result, the device has a higher immunity to false-keying when Strobe Control is low.

  In either case, the tone pair may be detected, but the Strobe signal may not necessarily be generated, depending on the quality of the input tone-pair.
- 1633 Hz Disable (N16) — If this input is low, the device will not respond to the 1633 Hz tone, thus improving the talk-off rate. If this input is high or open, the device will respond to the 1633 Hz tone.
- Clock Inputs and Control (X1, X2, TE) — The CRC 8030 contains an on-chip oscillator for a 3.57954 MHz parallel resonant crystal. This crystal is connected to X1 and X2 and TE is held high or left open. As an option, an external 447.443 kHz oscillator can be used to clock the CRC 8030. In this case, X1 is the 447.443 kHz clock input, X2 is left open, and TE is held low. For some applications (e.g., using several CRC 8030 devices on a board), it is possible to drive the chip with an external 3.579545-MHz clock at pin X2, while leaving the TE pin open, and tying pin X1 to V_{SS}.

Outputs

All outputs feature open-drain devices. With a single-power supply ($V_{GG} = V_{DD}$), they will drive LPTTL, MOS or CMOS inputs. With a dual power supply, they will drive the base of a transistor. The open-drain output devices must be tied through a pull-down resistor to a negative voltage between V_{DD} and V_{GG} (when used); the value of this resistor depends upon the type of interface. Typically:

Resistor	Interface
1.5KΩ	LPTTL
10.0KΩ	MOS or CMOS
7.5KΩ	Base of a Transistor

These outputs can also drive LEDs. For more design details, consult the Collins Application Note, "CRC 8030 Telephone DTMF Receiver".

- Decoded Outputs (D1/697 Hz, D2/770 Hz, D4/852 Hz, D8/941 Hz, 1209 Hz, 1336 Hz, 1477 Hz, 1633 Hz) — These outputs display decoded information in either a binary or a 2-of-8-coded format as described below.

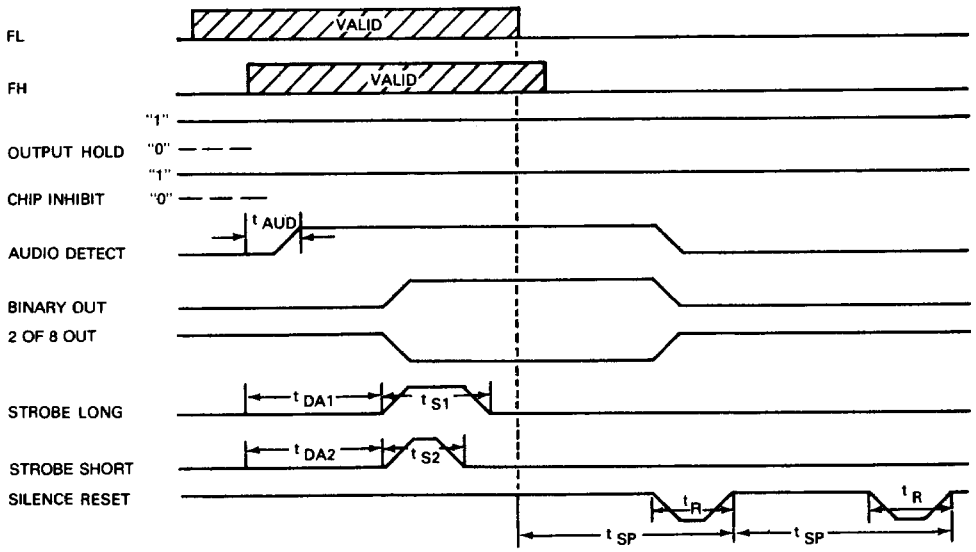
  When a 2-of-8 format is selected (BIN input is held high or left open), all 8 outputs are utilized. When a particular digit is decoded, the corresponding high- and low-group outputs go low (figure 1). For

RECOMMENDED OPERATING CONDITIONS/ELECTRICAL CHARACTERISTICS

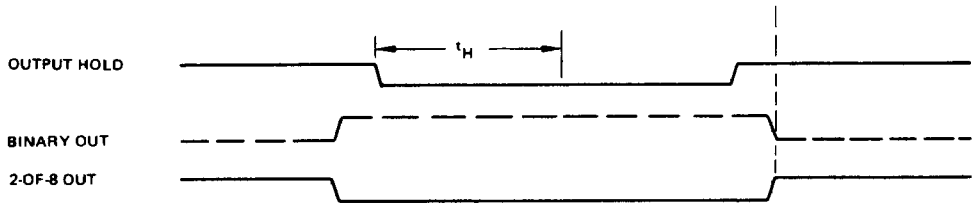
Unless Otherwise Noted V_{SS} = +5.0V, V_{GG} = -8.0V, V_{DD} = 0.0V
0°C ≤ T_A ≤ 70°C
Positive Logic

PARAMETER		MIN.	TYP.	MAX.	UNITS	CONDITIONS
Power Supplies						
V_{SS}		+4.75	+5	+5.25	V	
V_{GG}		-13.0	-8.0	V_{DD}	V	
V_{DD}				0		
Inputs						
$V_{IN}(0)$	Logical "0" input voltage	-13.0	-8.0	V_{SS}-4.0	V	
$V_{IN}(1)$	Logical "1" input voltage	V_{SS}-0.7		V_{SS}+0.2	V	
R_{IN}	Input impedance	50			kΩ	
C_{IN}	Input capacitance			10.0	pF	V_{IN} = V_{SS}-1.0V
t_r & t_f	Input voltage rise or fall time			15.0	μS	Voltage swing 10% to 90% of final level
Input Timing						
F_1	Clock Crystal Frequency		3.579545		MHz	±0.005%
F_2	Optional Clock Frequency		447.443		KHz	±0.005%
DC	Clock duty cycle	45	50	55	%	Optional Clock
t_r	Input clock pulse rise time	40		200	ns	10% to 90% of final level (Optional Clock)
t_f	Input clock pulse fall time	40		200	ns	90% to 10% of final level (Optional Clock)
Detected Frequencies Low Group			697		Hz	Bandwidth range: −1.9 to −3.2% +2.0 to +3.3%
			770		Hz	
			852		Hz	
			941		Hz	
Detected Frequencies High Group			1209		Hz	
			1336		Hz	
			1477		Hz	
			1633		Hz	
IDC	Input signal (FL or FH) duty cycle	30	50	70	%	
Outputs*						
$V_{OUT}(0)$	Logical "0" output voltage					V_{GG} + R_L I_{sink}
t_f(OUT)	Output fall time					2.2 R_L C_L
$V_{OUT}(1)$	Logical "1" output voltage	V_{SS}-0.4			V	I_{SOURCE} = 2.0 mA
t_r(OUT)	Output rise time			4	μS	10% to 90% of final level (with 30 pF load)
Output Timing						
t_{SP}	Silence Period	9.4	10	10.6	ms	
t_R	Silence Pulsewidth	1.0	1.1	1.2	ms	
t_{DA1}	Data Acquisition Time Option 1	22		39	ms	
t_{DA2}	Data Acquisition Time Option 2	25		33	ms	
t_{AUD}	Audio Detection Time	1.5	5	8	ms	
t_H	Output Hold Set-up Time	10			μS	
t_{INH}	Chip Inhibit Pulsewidth	2			μS	
C_2	Clock		2		kHz	±0.1 %
C_{16}	Clock		16		kHz	±0.1 %
C_{32}	Clock		32		kHz	±0.1 %
t_{S1}	Strobe Pulsewidth Option 1	0		17	ms	
t_{S2}	Strobe Pulsewidth Option 2	0		8	ms	
Power						
P_{D1}	Power Dissipation (Dual Power Supply)			200	mW	V_{SS} = 5.25V; V_{GG} = -13V
P_{D2}	Power Dissipation (Single Power Supply)			180	mW	V_{SS} = 5.25V; V_{GG} = V_{DD} = 0V

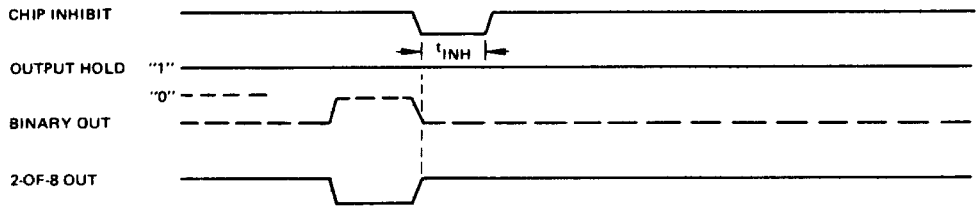
*For a full description of the output buffer capabilities, refer to the CRC 8030 Application Note.



NORMAL HOLD OPERATION



OUTPUT HOLD OPERATION



INHIBIT OPERATION

— — — OUTPUT LEVELS FOR BINARY OPERATION

——— OUTPUT LEVELS FOR 2-OF-8 OUTPUT OPTION

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Figure 4. Timing Diagram

Touch-Tone® Matrix: Binary Outputs																
	1209				1336				1477				1633			
	D1	D2	D4	D8	D1	D2	D4	D8	D1	D2	D4	D8	D1	D2	D4	D8
697	1	0	0	0	0	1	0	0	1	1	0	0	1	0	1	1
770	0	0	1	0	1	0	1	0	0	1	1	0	0	1	1	1
852	1	1	1	0	0	0	0	1	1	0	0	1	1	1	1	1
941	1	1	0	1	0	1	0	1	0	0	1	1	0	0	0	0

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Outputs (continued)

example, for digit 1, D1/697 Hz and 1209 Hz outputs will go low when detected. All other outputs remain high.

When the binary format is selected (BIN input is held low), the high-group outputs operate as described above. The low-group outputs (D1/697 Hz, D2/770 Hz, D4/852 Hz and D8/941 Hz) provide the binary coded information. These binary outputs are normally low and go high when a tone is detected. The outputs are defined by the above matrix:

- Strobe (ST) — This output indicates when the output data are valid. Validity is defined as detection within 39 ms or 33 ms depending upon the level of Strobe Control. For a description of the operation, refer to the inputs BIN and SC and figure 4.
- Silence Reset (SIL) — This output pulses to a low level when silence is detected. This occurs 9 ms after the interruption of a signal on either high- or low-group inputs. This output can be used to reset any external logic or to exercise the Output Hold option. The chip will reset itself after the Silence Reset output returns to a high level. Silence reset pulses at 10 ms intervals until a signal is present on either F_L or F_H.
- Audio Detect (AUD) — Audio is defined as energy carried by any frequency lower than 1680 Hz. AUD remains low when both FL and FH are low; AUD will go high if either FL or FH is toggling and will return to a low level as soon as Silence Reset returns from a low to a high level. This output may be used to control the admissible level in the Front-End circuitry (off-chip) or to give advance notice of a tone-pair.
- Test Output (X0) — When using the 3.579545 MHz crystal on-chip oscillator, X0 will display a 447.443 kHz clock. If the 447.443 kHz external oscillator option is utilized, X0 will display a 55.930 kHz clock. The X0 output frequency will be the X1 input frequency divided by 8.
- Clock Outputs (C2, C16, C32) — These outputs will generate 2 kHz, 16 kHz and 32 kHz clocks, respectively.

DTMF Receiver Design

The CRC 8030, in conjunction with a front-end analog filter/limiter, implements a complete DTMF receiver. Figure 2 illustrates this design. With this approach, a central-office-quality receiver with the following specification can be implemented:

- Input Dynamic Range . . . . . -26 dBm to +6 dBm
- Twist . . . . . -8 dB to +4 dB
- Valid Tone Tolerance . . . . . ±1.5%
- Invalid Tone Reject Limit . . . . . ±3.5%
- Tone Burst (minimum) . . . 40 ms ON, 11 ms OFF at 12 bursts per second

Inasmuch as the front-end filter is an essential part of the total receiver, its characteristics have a major impact on the performance of the system. For example, for high-quality central-office receivers, a more selective front-end filter is required. Conversely, low-noise environment keyphone systems will operate with a less stringent front-end filter design. In view of the differences in specifications for DTMF receivers, the front-end design must be tailored for the particular application. Several manufacturers have off-the-shelf hybrid products which meet these filtering requirements. For more details concerning these design considerations, refer to the Collins "Application Note — CRC 8030 Telephone DTMF Receiver"

For specialized applications, the CRC 8030 has several mask programmable features. The parameters that can be programmed include the bandwidth, detection time, strobe time, silence time, and output decode format. Contact Collins Applications Engineering for details.

Packaging and Ordering Information

The DTMF Detector is available in a 28-pin, hermetically sealed ceramic dual-in-line package and in a 28-lead ceramic chip carrier (see pin assignments and package dimension diagrams). Order by type number.

CRC 8030-1-3 (ceramic DIP) 765-5795-001
CRC 8030-4-3 (ceramic carrier) . . . 765-5795-003

For further information on Rockwell MOS/LSI Standard Products, call your local Rockwell Sales office or:

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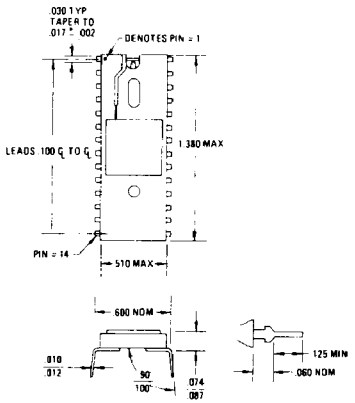
TWX 910-591-1698

DTMF DETECTOR (CRC 8030-1-3)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	V_{SS}	15	1209 HZ
2	1633 HZ	16	HLD
3	SIL	17	SC
4	INH	18	V_{DD}
5	C2	19	D4/852 HZ
6	C16	20	D8/941 HZ
7	C32	21	ST
8	X2	22	D2/770 HZ
9	V_{GG}	23	BIN
10	X1	24	FL
11	TE	25	FH
12	X0	26	D1/697 HZ
13	AUD	27	1477 HZ
14	1336 HZ	28	N16

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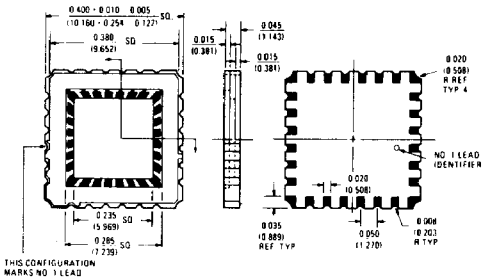
DTMF DETECTOR (CRC 8030-4-3)



PINS ARE READ COUNTERCLOCKWISE

PIN NO	FUNCTION	PIN NO.	FUNCTION
1	V_{SS}	15	1209 HZ
2	1633 HZ	16	HLD
3	SIL	17	SC
4	INH	18	V_{DD}
5	C2	19	D4/852 HZ
6	C16	20	D8/941 HZ
7	C32	21	ST
8	X2	22	D2/770 HZ
9	V_{GG}	23	BIN
10	X1	24	FL
11	TE	25	FH
12	X0	26	D1/697 HZ
13	AUD	27	1477 HZ
14	1336 HZ	28	N16

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NOTE: Collins MOS/LSI Products is now a part of Microelectronic Devices, Rockwell International.