54F/74F557 • 54F/74F558

8-Bit By 8-Bit Multipliers With 3-State Outputs

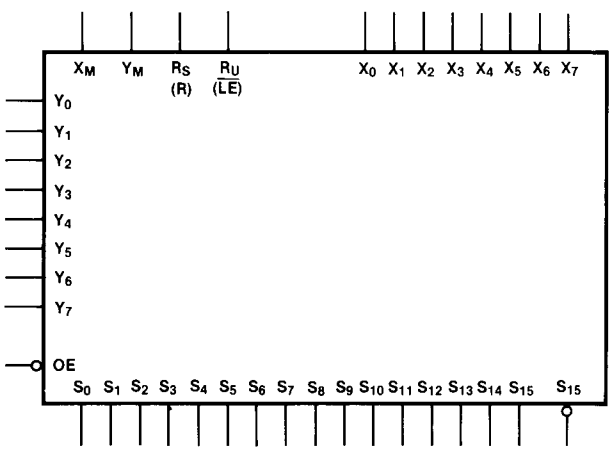
Description

The 'F557 and 'F558 are high-speed combinatorial arrays that multiply two 8-bit unsigned or signed twos complement numbers and provide the 16-bit unsigned or signed product. Each input operand X and Y has a mode control input that determines whether the number is treated as signed or unsigned. Additional inputs, R_S and R_U for the 'F558 or R for the 'F557, allow the addition of a bit for rounding to the best signed or unsigned fractional 8-bit result. For expansion during signed or mixed multiplication, both the true and complement outputs of the most significant bit are available. The 'F557 has output latches that store the results when $\overline{LE}$ is HIGH. Both devices have 3-state outputs for bus applications.

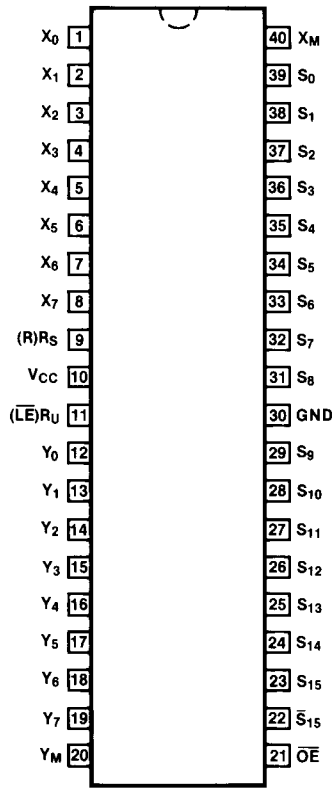
- **Unsigned, Signed or Mixed Multiplication**
- **Full 16-Bit Product Outputs**
- **MSB Complement Output for Signed Expansion**
- **Rounding Inputs for Fractional 8-Bit Product**

Ordering Code: See Section 5

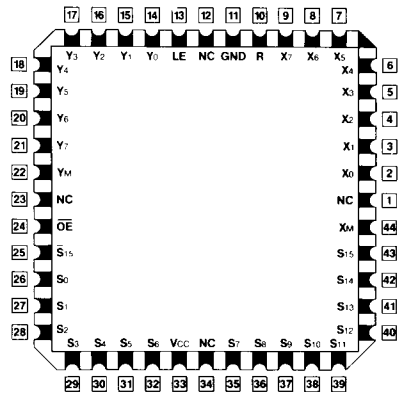
Logic Symbol



Connection Diagrams



Pin Assignment for DIP



Pin Assignment for LCC and PCC

Pin assignments shown are for 'F558. $\overline{LE}$ and R shown in parentheses are pin assignments for 'F557.

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
X_0-X_7	Multiplicand Inputs	0.5/0.5
Y_0-Y_7	Multiplier Inputs	0.5/0.5
X_M	Multiplicand Sign Control Input	0.5/0.5
Y_M	Multiplier Sign Control Input	0.5/0.5
R	Rounding Input ('F557)	0.5/0.5
R_S	Signed Number Rounding Input ('F558)	0.5/0.5
R_U	Unsigned Number Rounding Input ('F558)	0.5/0.5
$\overline{LE}$	Latch Enable Input (Active LOW) ('F557)	0.5/0.5
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.5
S_0-S_{15}	Product Outputs	50/12.5
$\overline{S}_{15}$	MSB Complement Output	50/12.5

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Functional Description

The 'F557 and 'F558 multipliers are 8x8 combinatorial logic arrays capable of multiplying numbers in unsigned, signed twos complement or mixed notation. Each 8-bit input operand X and Y has an associated mode control which determines whether the array treats the number as signed or unsigned. If the mode control X_M or Y_M is HIGH, the operand is treated as a twos complement number with the most significant bit having a negative weight; if the mode control is LOW, the operand is treated as an unsigned number.

The multipliers provide all sixteen product bits generated by the multiplication. For expansion during signed or mixed multiplication, the most significant product bit has both true and complement available. Therefore, an adder may be used as a subtractor in many applications and the need for SSI circuits is eliminated.

The 'F557 has latches that store the product for pipelined operations. When $\overline{LE}$ is HIGH the latches are transparent and their outputs change with their inputs. When $\overline{LE}$ is LOW the latches are in the storage mode and new data cannot enter.

The 3-state output buffers are controlled by the active LOW Output Enable $\overline{OE}$ input. When $\overline{OE}$ is LOW, the outputs are active; when $\overline{OE}$ is HIGH, the outputs are in a high impedance (High Z) state. Several multipliers can be connected on a common bus or used in a pipeline system for multiplications in higher speed systems.

Rounding

The 16-bit product can be truncated to eight bits by using the rounding input(s) to add one in either the 2^7 adder for unsigned numbers or in the 2^6 adder for signed numbers. The 'F558 has separate rounding inputs R_S and R_U for signed or unsigned numbers, respectively. The 'F557 has a single rounding input R and develops the proper rounding by internally combining R with X_M and Y_M as follows:

$R_U = \overline{X}_M \bullet \overline{Y}_M \bullet R$ = unsigned rounding input to 2^7 adder

$R_S = (X_M \pm Y_M)R$ = signed rounding input to 2^6 adder

Rounding input levels and results for the various modes are shown in Tables 1 and 2. Figure a shows how R_S and R_U would normally be used for rounding signed and unsigned fractional multipliers.

Signed Expansion

The most significant product bit has both true and complement outputs available. When building larger signed multipliers the partial products, except at the lower stages, are signed numbers. These unsigned and signed partial products must be added to give the correct signed product. For example, to obtain the correct signed product when using MSI adders, the carry from the previous adder stage must be added to the sum of the two negative most significant partial product bits. The result of this addition must be a positive sum and a negative carry (borrow). The equations are:

$$S = A + B + C$$
$$C_0 = A \bullet B + B \bullet \overline{C} + \overline{C} \bullet A$$

where C is the Carry In and A and B the sign bits of the two partial products.

An adder produces the equations:

$$S = A + B + C$$
$$C_0 = A \bullet B + B \bullet C + C \bullet A$$

Therefore, if the inversion of A and B is used, then the adder produces the inversion of the negative carry since

$$A \bullet B + B \bullet \overline{C} + \overline{C} \bullet A = \overline{\overline{A} \bullet \overline{B} + \overline{B} \bullet C + \overline{A} \bullet C}$$

and the sum remains the same.

Table 1 'F557 Rounding Inputs

Inputs			Adds	
X_M	Y_M	R	2^7	2^6
L	L	H	Yes	No
L	H	H	No	Yes
H	L	H	No	Yes
H	H	H	No	Yes
X	X	L	No	No

Table 2 'F558 Rounding Inputs

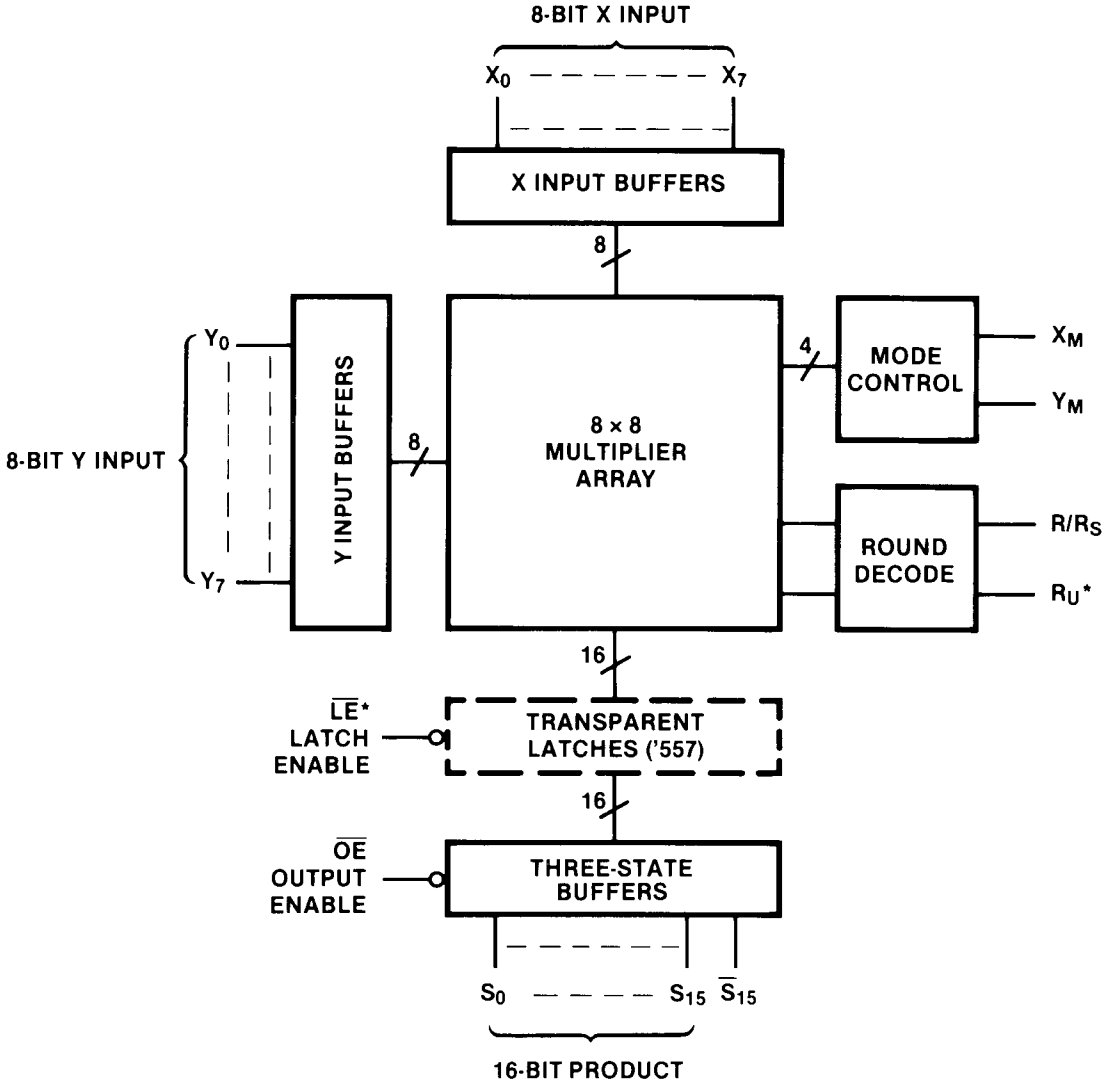
Inputs		Adds		Normally Used With	
R_U	R_S	2^7	2^6	X_M	Y_M
L	L	No	No	X	X
L	H	No	Yes	$X_M + Y_M = H$	
H	L	Yes	No	L	L
H	H	Yes	Yes	*	*

*Most rounding applications require a HIGH level for R_U or R_S, but not both.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Mode Select Table

Operating Mode	Input Data		Mode Control Inputs	
	X_0-X_7	Y_0-Y_7	X_M	Y_M
Unsigned	Unsigned	Unsigned	L	L
Mixed	Unsigned	Twos Complement	L	H
	Twos Complement	Unsigned	H	L
Signed	Twos Complement	Twos Complement	H	H

Block Diagram



$\overline{LE}$ for 'F557 and R_U for 'F558.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		200	280	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay X_n or Y_n to S_n, $\overline{S}_{15}$		70.0 70.0						ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$ to S_n, $\overline{S}_{15}$ ('F557)		20.0 2.0						ns	3-1 3-8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to S_n or $\overline{S}_{15}$		14.0 14.0						ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to S_n or $\overline{S}_{15}$		21.0 14.0							

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW X_n or Y_n to $\overline{LE}$		65.0 65.0						ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW X_n or Y_n to $\overline{LE}$		0 0						ns	3-14
$t_w(L)$	$\overline{LE}$ Pulse Width, LOW		10.0						ns	3-8

Applications

16x16 Twos Complement Multiplier

The 'F558 8x8 multiplier can be used with standard MSI adder circuits to build larger multipliers. Figure b illustrates the use of four 'F558 multipliers and ten 16-pin 4-bit 'F283 adders to form a 16x16-bit twos complement multiplier with a typical multiplication time of 90 ns. The 16-bit operands are split up into 8-bit sections:

$$X \bullet Y = (X_{0\text{-}7} + X_{8\text{-}15}2^8) \bullet (Y_{0\text{-}7} + Y_{8\text{-}15}2^8)$$
$$= X_{0\text{-}7} \bullet Y_{0\text{-}7} + 2^8(X_{0\text{-}7} \bullet Y_{8\text{-}15} + X_{8\text{-}15} \bullet Y_{0\text{-}7})$$
$$= + 2^{16}(X_{8\text{-}15} \bullet Y_{8\text{-}15})$$

Since X_8-X_{15} and Y_8-Y_{15} are signed numbers, the most significant bit of all the partial products (except the first) carries a negative weight. Therefore, at these negative bit positions the partial product bits must be subtracted rather than added. This subtraction is done in the middle of the network at the 2^{15} bit position by using the inverted output of the most significant product bits from the multipliers to obtain a borrow signal from the last sum output of the appropriate 'F283. This borrow is then used to either add zero or minus 1 to the remaining 8-bit adder section. The mode control inputs of the four 'F558 devices are tied to the logic levels required to produce the correctly signed partial products. Rounding to the best 16-bit fractional product is made by tying the R_S input of one of the middle multipliers to V_{CC}. Appropriate connection of the adders and mode control logic levels will yield 16x16 unsigned multiplication.

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Fig. a Rounded Products

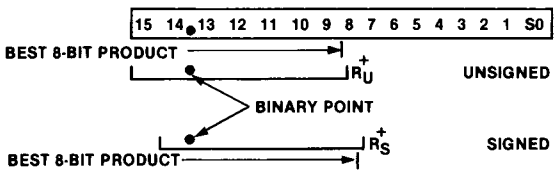

Fig. b High-Speed 16x16 Twos Complement Multiplication