MILITARY DRAM

256K x 1 DRAM

AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-85152
- JAN M38510/246
- MIL-STD-883, Class B

FEATURES

- Industry standard pinout and timing
- All inputs, outputs and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby; 150mW active, typical
- Common I/O capability using "EARLY-WRITE"
- Optional PAGE MODE access cycle
- Refresh modes: $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$, and HIDDEN
- 256-cycle refresh distributed across 4ms
- Specifications guaranteed over full military DRAM temperature range (-55°C to +110°C)

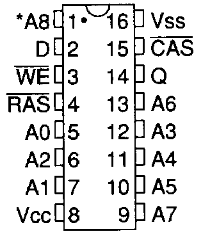
OPTIONS	MARKING
• Timing	
100ns access	-10
120ns access	-12
150ns access	-15
• Packages	
Ceramic DIP	C
Ceramic LCC	EC

GENERAL DESCRIPTION

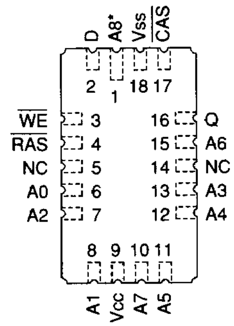
The MT1259 883C is a randomly accessed solid-state memory containing 262,144 bits organized in a x1 configuration. The 18 address bits are entered 9 bits at a time using $\overline{\text{RAS}}$ to latch the first 9 bits and $\overline{\text{CAS}}$ the latter 9 bits. If the $\overline{\text{WE}}$ pin goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin remains open until the next $\overline{\text{CAS}}$ cycle. If $\overline{\text{WE}}$ goes LOW after data reaches the output pin, the output pin is activated and retains the selected cell data as long as $\overline{\text{CAS}}$ remains LOW (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ-MODIFY-WRITE cycle. Data in is latched when $\overline{\text{WE}}$ strobes LOW.

PIN ASSIGNMENT (Top View)

16L/300 DIP
(D-2)



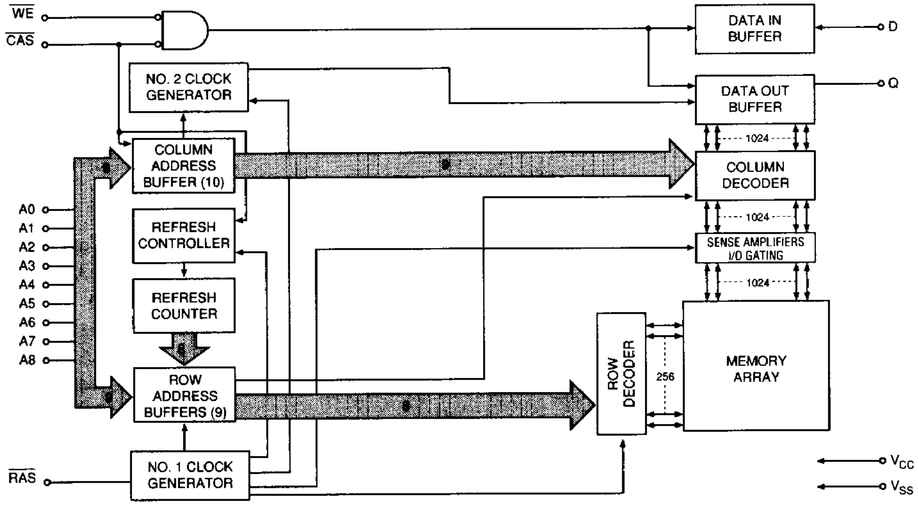
18L/LCC



*Address not used for $\overline{\text{RAS}}$-ONLY REFRESH

By holding $\overline{\text{RAS}}$ LOW, $\overline{\text{CAS}}$ may be toggled to execute several faster READ, WRITE, READ-WRITE or READ-MODIFY-WRITE cycles within the $\overline{\text{RAS}}$ address defined page boundary. Returning $\overline{\text{RAS}}$ HIGH terminates the memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{\text{RAS}}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{\text{RAS}}$ (READ, WRITE, $\overline{\text{RAS}}$-ONLY or HIDDEN REFRESH) cycle so that all 256 combinations of $\overline{\text{RAS}}$ addresses are executed at least every 4ms (regardless of sequence).

FUNCTIONAL BLOCK DIAGRAM
PAGE MODE



TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses		
				^tR	^tC	
Standby	H	H	H	X	X	High-Z
READ	L	L	H	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	ROW	COL	Data Out, Data In
PAGE-MODE READ	L	H→L→H	H	ROW	COL	Data Out, Data Out
PAGE-MODE WRITE	L	H→L→H	L	ROW	COL	Data In, Data In
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Data Out, Data In
$\overline{RAS}$-ONLY REFRESH	L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Data Out
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS}	-1.5V to +7.0V
Storage Temperature Range	-65°C to +150°C
Power Dissipation	1W
Lead Temperature (soldering 5 seconds)	300°C
Junction Temperature (Tj)	+150°C
Short Circuit Output Current	50mA
Thermal Resistance (θjc) 16-Pin DIP	50°C/W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL PERFORMANCE CHARACTERISTICS

(Notes: 4, 6, 7) ($-55°C \le T_C \le +110°C$; $V_{CC} = 5.0V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Current from V_{CC} (Active); $\overline{RAS}$ and $\overline{CAS}$ Cycling; $^{t}RC = {}^{t}RC$ (MIN)	I_{CC1}		55	mA	2
Supply Current from V_{CC} (Active, PAGE MODE); $\overline{RAS} = V_{IL}$, $\overline{CAS}$ Cycling; $^{t}PC = {}^{t}PC$ (MIN)	I_{CC2}		55	mA	2
Supply Current from V_{CC} (Standby); $\overline{RAS}$ and $\overline{CAS} = V_{IH}$	I_{CC3}		8	mA	2
Supply Current from V_{CC} (REFRESH, $\overline{RAS}$-ONLY); $\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$	I_{CC4}		45	mA	2
Supply Current from V_{CC} (REFRESH, $\overline{CAS}$-BEFORE-$\overline{RAS}$); $\overline{RAS}$ and $\overline{CAS}$ Cycling	I_{CC5}		55	mA	2
Output High Voltage ($I_{OH} = -5mA$)	V_{OH}	2.4		V	1
Output Low Voltage ($I_{OL} = 5mA$)	V_{OL}		0.4	V	1
Input Leakage	I_{IH}	-10	10	μA	
Any Input ($0V \le V_{IN} \le V_{CC}$), All Other Pins = 0V	I_{IL}	-10	10	μA	
Output Leakage ($0 \le V_{OUT} \le V_{CC}$)	I_{OZ}	-10	10	μA	

DC OPERATING CONDITIONS

(Notes: 4, 6, 7) ($-55°C \le T_C \le +110°C$; $V_{CC} = 5.0V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} Supply Voltage	V_{CC}	4.5	5.5	V	
V_{SS} Power Supply and Signal Reference	V_{SS}	0.0	0.0	V	1
High-Level Input Voltage (All Inputs)	V_{IH}	2.4	$V_{CC}+1$	V	1
Low-Level Input Voltage (All Inputs)	V_{IL}	-1.0	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: (A0-A8), D	C_{I1}		5	pF	3
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		8	pF	3
Output Capacitance: Q	C_{O}		7	pF	3

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

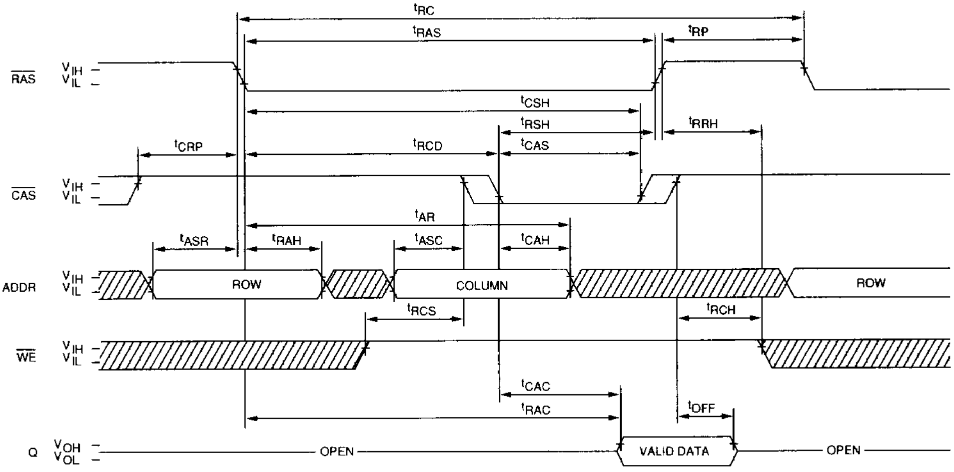
(Notes: 4, 5, 6, 7, 8) (-55°C ≤ T_C ≤ +110°C; Vcc = 5.0V ±10%)

AC CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^{t}RC	195		220		250		ns	
READ-MODIFY-WRITE cycle time	^{t}RWC	230		250		275		ns	18
PAGE MODE cycle time	^{t}PC	90		100		120		ns	18
Access time from $\overline{\text{RAS}}$	^{t}RAC		100		120		150	ns	9
Access time from $\overline{\text{CAS}}$	^{t}CAC		50		60		75	ns	10
$\overline{\text{RAS}}$ pulse width	^{t}RAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{\text{CAS}}$ pulse width	^{t}CAS	50	10,000	60	10,000	75	10,000	ns	
$\overline{\text{RAS}}$ precharge time	^{t}RP	80		90		90		ns	
$\overline{\text{RAS}}$ hold time	^{t}RSH	50		60		75		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	^{t}RCD	30	50	30	60	30	75	ns	20
$\overline{\text{CAS}}$ precharge time	^{t}CPN	25		25		30		ns	18
$\overline{\text{CAS}}$ precharge time (PAGE MODE)	^{t}CP	30		30		35		ns	11
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ setup time	^{t}CRP	5		5		5		ns	
$\overline{\text{CAS}}$ hold time	^{t}CSH	110		120		150		ns	
Row address setup time	^{t}ASR	0		0		0		ns	18
Row address hold time	^{t}RAH	15		20		20		ns	
Column address setup time	^{t}ASC	0		0		0		ns	18
Column address hold time	^{t}CAH	20		30		30		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	^{t}AR	70		80		100		ns	
Read command setup time	^{t}RCS	0		0		0		ns	18
Read command hold time referenced to $\overline{\text{CAS}}$	^{t}RCH	0		0		0		ns	18
Read command hold time referenced to $\overline{\text{RAS}}$	^{t}RRH	10		10		10		ns	
Output disable delay	^{t}OFF	0	40	0	40	0	40	ns	12
Write command setup time	^{t}WCS	0		0		0		ns	13
Write command hold time	^{t}WCH	35		40		45		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	^{t}WCR	85		100		120		ns	
Write command pulse width	^{t}WP	35		40		45		ns	
Write command to $\overline{\text{RAS}}$ lead time	^{t}RWL	35		40		45		ns	
Write command to $\overline{\text{CAS}}$ lead time	^{t}CWL	35		40		45		ns	
Data-in setup time	^{t}DS	0		0		0		ns	14, 18
Data-in hold time	^{t}DH	35		40		45		ns	14
Data-in hold time referenced to $\overline{\text{RAS}}$	^{t}DHR	85		100		120		ns	
$\overline{\text{CAS}}$ to write delay	^{t}CWD	40		50		60		ns	13, 18
$\overline{\text{RAS}}$ to write delay	^{t}RWD	90		110		135		ns	13, 18
Transition time (rise or fall)	^{t}T	3	100	3	100	3	100	ns	18
$\overline{\text{CAS}}$ setup time ($\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH)	^{t}CSR	10		10		10		ns	15
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH)	^{t}CHR	20		25		30		ns	15
Refresh period (256 cycles distributed)	^{t}REFD		4		4		4	ms	16
Refresh period (256 cycles burst)	^{t}REFB		4		4		4	ms	17
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	^{t}RPC	0		0		0		ns	18

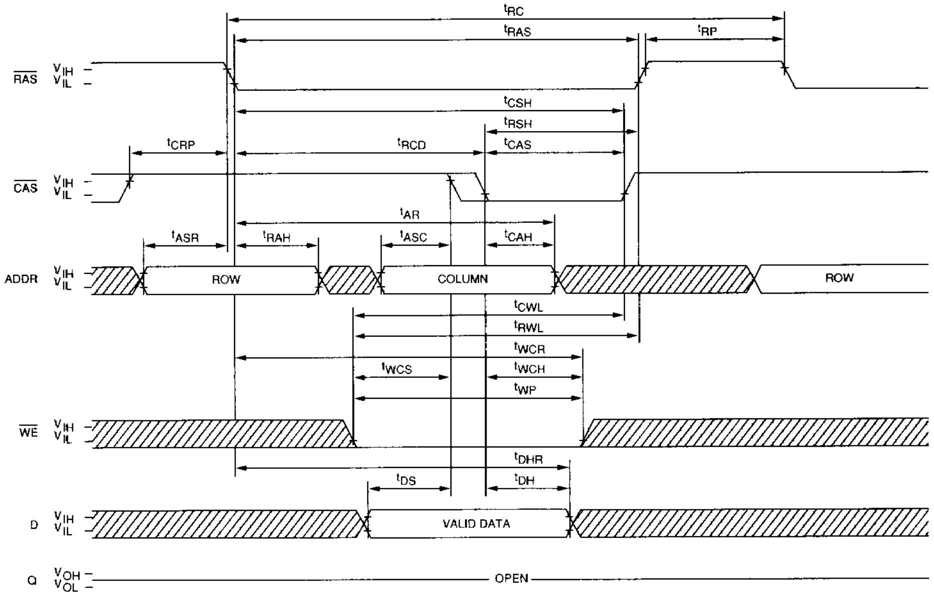
NOTES

1. Vss is common for all voltages.
2. Specified values are obtained with the output load equal to 2TTL loads and 100pF to Vss.
3. This parameter is sampled, not 100% tested. Capacitance is measured with Vcc = 5.0V, f = 1MHz at less than 50mVrms, T_A = 25°C ± 3°C, Vbias = 2.4V applied to each input and output individually with remaining inputs and outputs open.
4. An initial pause of 100µs is required after power-up followed by any eight $\overline{\text{RAS}}$ cycles, (READ, WRITE, READ-MODIFY-WRITE, $\overline{\text{RAS}}$ REFRESH) before proper device operation is assured.
5. AC characteristics assume transition time (^{t}T) = 5ns. This parameter is not measured.
6. V_{IL} (MAX) and V_{IH} (MIN) are reference levels for measuring timing of input signals. Transition times are measured between V_{IL} and V_{IH}.
7. In addition to meeting the transition rate specification, all input signals must transit between V_{IL} and V_{IH} (or between V_{IH} and V_{IL}) in a monotonic manner.
8. If $\overline{\text{CAS}}$ = V_{IH}, data output is High-Z. If $\overline{\text{CAS}}$ = V_{IL}, data output may contain data from the last valid READ cycle.
9. Assumes that ^{t}RCD < ^{t}RCD (MAX).
10. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
11. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{\text{CAS}}$ must be pulsed HIGH for ^{t}CP. Note 8 applies to determine valid data out.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition. ^{t}OFF (MAX) is not referenced to V_{OH} or V_{OL}.
13. ^{t}WCS, ^{t}CWD and ^{t}RWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN) the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}CWD ≥ ^{t}CWD (MIN) and ^{t}RWD ≥ ^{t}RWD (MIN) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{\text{CAS}}$ goes back to V_{IH}) is indeterminate.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY-WRITE cycles and to the $\overline{\text{WE}}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
15. Enable on-chip refresh and address counters.
16. A 256-cycle distributed refresh consists of an address location refresh cycle being performed within 15.625µS so that all 256 $\overline{\text{RAS}}$ address combinations are executed within 4ms (regardless of sequence). Micron recommends distributed refresh.
17. A 256-cycle burst refresh consists of refreshing, as rapidly as minimum cycle time allows, all 256 combinations of $\overline{\text{RAS}}$ addresses (regardless of sequence). The refresh mode must be executed within 4ms.
18. This parameter is a "conditionally" guaranteed parameter that is specified to aid with device application. It is not directly verified by a specific test but is used, with several other parameters, in the performance verification of other attributes.
19. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{\text{WE}}$ = LOW.
20. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.

READ CYCLE



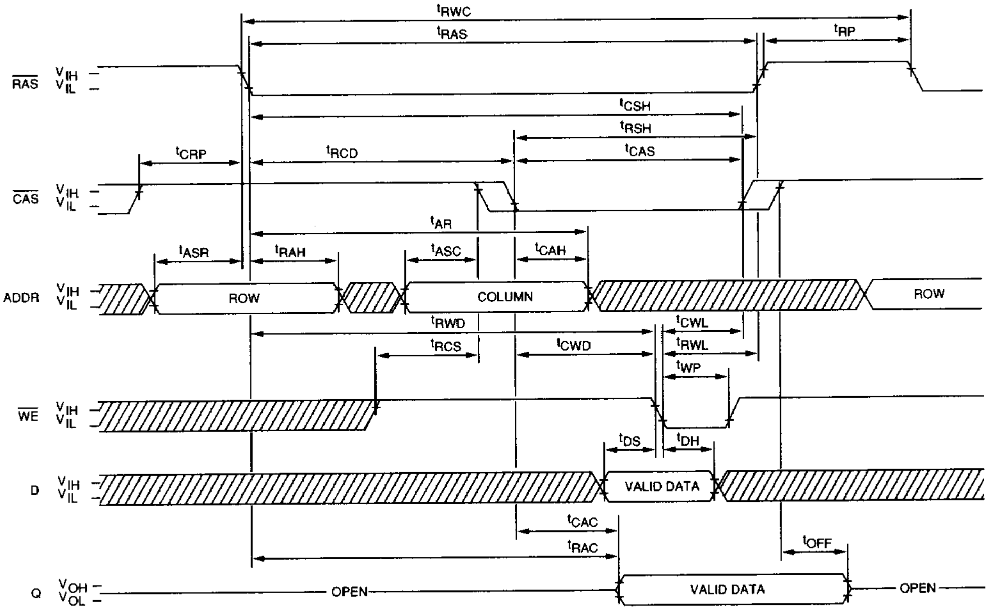
EARLY-WRITE CYCLE



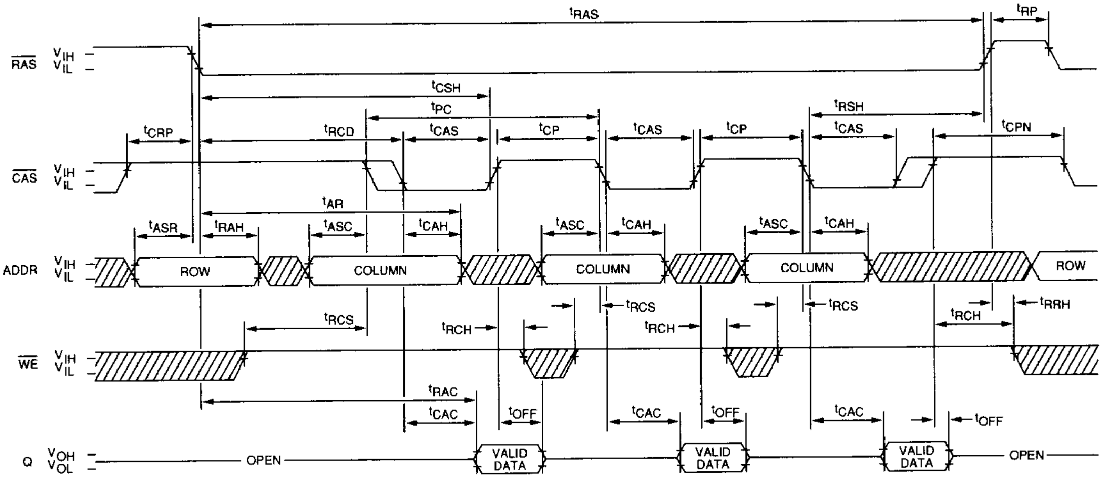
▨ DON'T CARE

▦ UNDEFINED

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



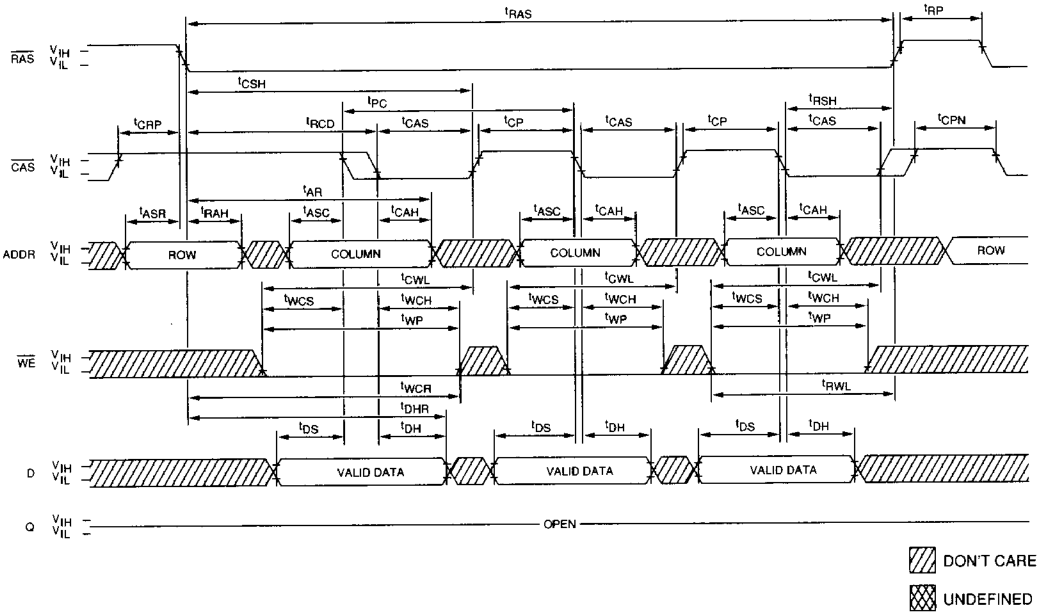
PAGE-MODE READ CYCLE



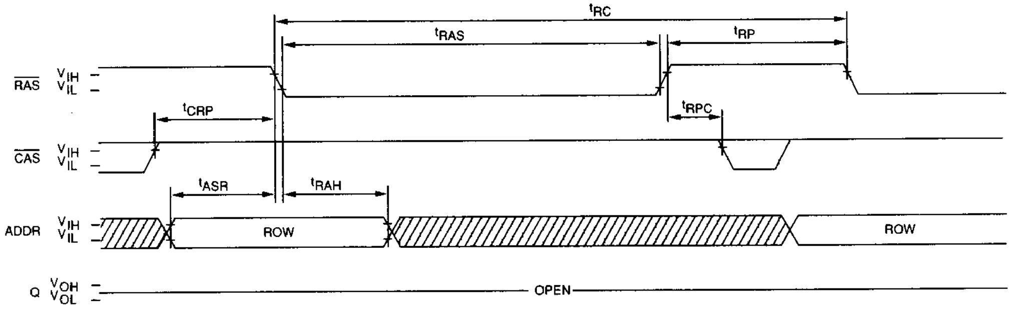
▨ DON'T CARE

▩ UNDEFINED

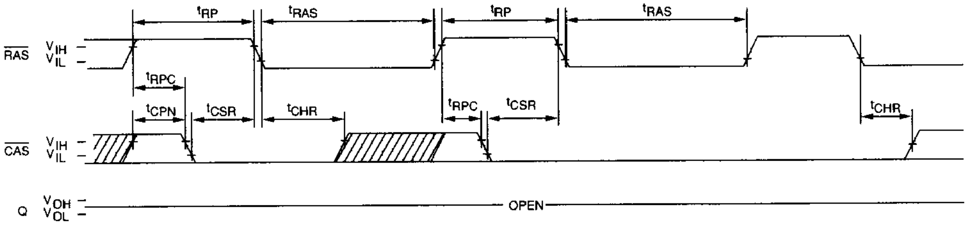
PAGE-MODE EARLY-WRITE CYCLE



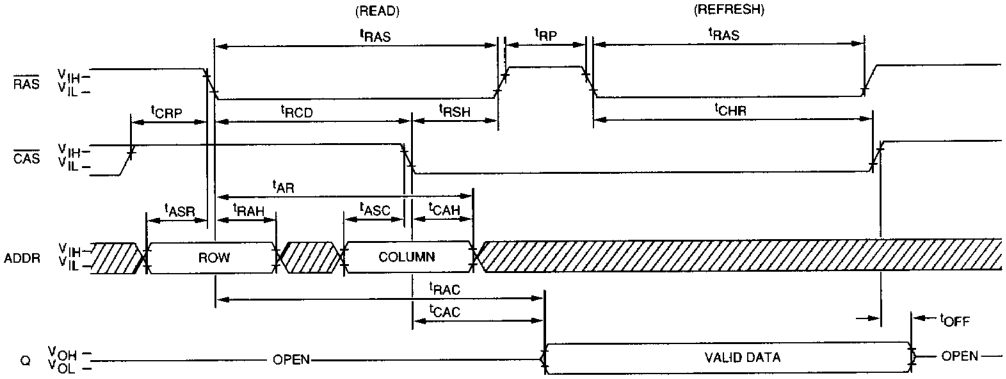
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A7; A8 and $\overline{\text{WE}}$ = DON'T CARE)



$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A8 and $\overline{\text{WE}}$ = DON'T CARE)



HIDDEN REFRESH CYCLE
($\overline{\text{WE}}$ = HIGH)[19]



▨ DON'T CARE
▩ UNDEFINED

ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (per Method 5005, Table I)
INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS (Method 5004)	2, 8A, 10
FINAL ELECTRICAL TEST PARAMETERS (Method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
GROUP A TEST REQUIREMENTS (Method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11

* PDA applies to subgroups 1 and 7.

** Subgroup 4 shall be measured only for initial qualification and after process or design changes which may affect input or output capacitance.