HY51V65164,HY51V64164

4M x 16-bit CMOS DRAM with Extended Data Out

PRELIMINARY

DESCRIPTION

This family is a 64M bit dynamic RAM organized 4,194,304 x 16-bit configuration with Extended Data Out mode CMOS DRAMs. Extended Data Out mode offers high speed random access of memory cells within the same row. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time(50,60 or 70ns) and refresh cycle(8K Ref. or 4K Ref.) and package type(TSOP-II) and power consumption(Normal or Low power with self refresh). Hyundai's advanced circuit design and process technology allow this device to achieve high band-width low power consumption and high reliability.

ORDERING INFORMATION

Part Number	Ref.	Power	Pkg.
HY51V64164TC	8K		TSOP-II
HY51V64164LJC	8K	L-part	TSOP-II
HY51V64164SLTC	8K	SL-part	TSOP-II
HY51V65164TC	4K		TSOP-II
HY51V65164LTC	4K	L-part	TSOP-II
HY51V65164WLTC	4K	SL-part	TSOP-II

* Reverse TSOP-II packages are also available

FEATURES

- Part Number Information
  - HY51V64164 : 8K Ref.
  - HY51V65164 : 4K Ref.
- Max. Active Power Dissipation

Speed	8K	4K
50	504mW	648mW
60	432mW	576mW
70	360mW	504mW

- Fast access time and cycle time

Speed	tRAC	tCAC	tHPC
50ns	50ns	13ns	20ns
60ns	60ns	15ns	25ns
70ns	70ns	20ns	30ns

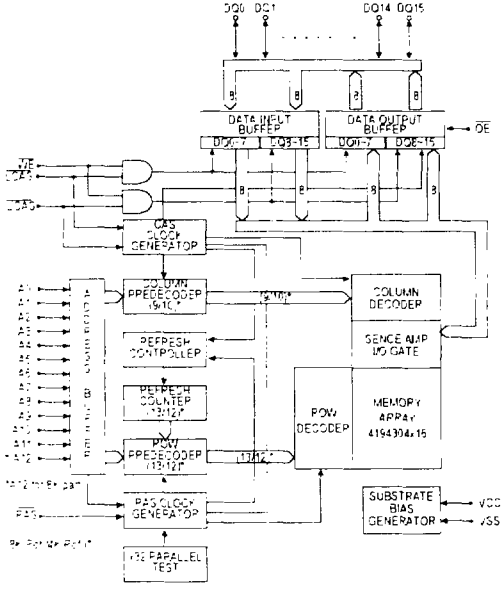
- Extended Data Out Operation
- Single power supply of 3.3V ± 10%
- Read-Modify-Write Capability
- Multi-bit test capability
- LVTTL compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self Refresh Capability
- Refresh cycles

Part No.	Ref	Normal	L-part
HY51V64164	8K*	64ms	128ms
HY51V65164	4K		

* /CAS-before-/RAS refresh Hidden refresh mode 4K cycles / 64ms

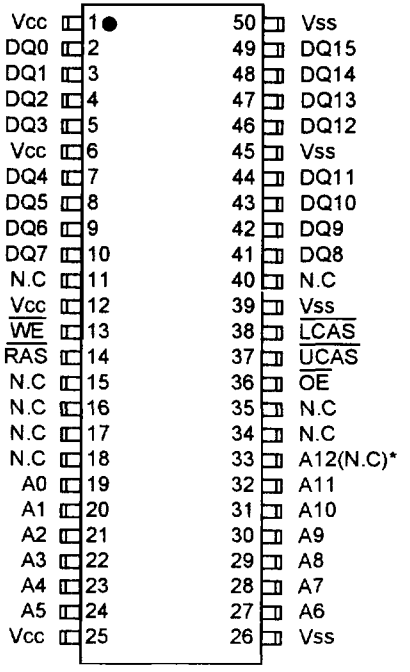
- JEDEC standard pinout
  50-pin Plastic TSOP (II) (400mil)

BLOCK DIAGRAM



64M

PIN CONFIGURATION (Marking Side)



50-pin Plastic TSOP-II (400mil)

(N.C)* : For 4K Refresh product

PIN DESCRIPTION

/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0-A12	Address Input (8K Product)
A0-A11	Address Input (4K Product)
DQ0-DQ15	Data In/Out
VCC	Power (3.3V)
VSS	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature	-55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin relative to V_{SS}	-0.5 to 4.6	V
V_{CC}	Voltage on V_{CC} relative to V_{SS}	-0.5 to 4.6	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	℃ · sec

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0℃to 70 ℃)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

Note: All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(T_A=0℃to 70℃, Vcc=3.3V ± 10%, Vss=0V, unless otherwise noted.)

Symbol	Parameter	Test Conditions	Speed	Max. Current		UNIT
				8K Product	4K Product	
I_{CC1}	Operating Current	/RAS, /CAS Cycling tRC=tRC (min.)	50 60 70	140 120 100	180 160 140	mA
I_{CC2}	LVTTL Standby Current	/RAS = /CAS ≥ V_{IH} other inputs ≥ Vss		1	1	mA
I_{CC3}	/RAS-only Refresh Current	/RAS cycling /CAS = V_{IH} tRC = tRC (min.)	50 60 70	140 120 100	180 160 140	mA
I_{CC4}	EDO Mode Current	/CAS cycling /RAS = V_{IL} tHPC = tHPC (min.)	50 60 70	150 130 110	150 130 110	mA
I_{CC5}	CMOS Standby Current	/RAS = /CAS ≥ Vcc - 0.2V	L-part	500 300	500 300	μA μA
I_{CC6}	/CAS-before-/RAS Refresh Current	tRC=tRC (min.)	50 60 70	180 160 140	180 160 140	mA
I_{CC7}	Battery Back-up Current (L-part)	V_{IH} = Vcc - 0.2V, V_{IL} = 0.2V /CAS = CBR cycling or 0.2V /OE & /WE = V_{IH} = Vcc - 0.2V Address = Don't care DQ0-DQ15 =Open,tRAS≤ 300ns		700	700	μA
I_{CC8}	Self Refresh Current (L-part)	/RAS & /CAS = 0.2V Other pins are same as Icc7		700	700	μA

Symbol	Parameter	Test condition	Min.	Max	UNIT
I_{LI}	Input Leakage current(Any Input)	Vss ≤ V_{IN} ≤ Vcc + 0.3, All other pins not under test=Vss	-1	1	μA
I_{LO}	Output Leakage current(Any Input)	Vss ≤ V_{OUT} ≤ Vcc /RAS & /CAS at V_{IH}	-1	1	μA
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.0mA	2.4	-	V

NOTE

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} dependent on output loading and cycle rates(tRC and tHPC).
2. Specified values are obtained with outputs unloaded.
3. Icc is specified as an average current. In Icc1, Icc3, Icc6, address can be changed only once while /RAS=VIL. In Icc4, address can be changed maximum once while /CAS=V_{IH} within one EDO mode cycle time tHPC.
4. Only tRAS(max.) = 1 μs is applied to refresh of battery backup but tRAS(max.) = 10 μs is to applied to normal functional operation.
5. Icc5(max.) = 200 μA, Icc7 and Icc8 are applied to L-part and SL-part only.
6. V_{OH} = 2.0V, V_{OL} = 0.8V at AC Functional Test.

AC CHARACTERISTICS

(T_A=0℃to 70℃, Vcc=3.3V ± 10%, Vss=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY51V64164 / HY51V658164						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	90	-	110	-	130	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	120	-	140	-	170	-	ns	
3	tHPC	EDO Mode Cycle Time	20	-	25	-	30	-	ns	
4	tHPRWC	EDO Mode Read-Modify-Write Cycle Time	50	-	60	-	75	-	ns	
5	tRAC	Access Time from /RAS	-	50	-	60	-	70	ns	4,5,10,11
6	tCAC	Access Time from /CAS	-	13	-	15	-	20	ns	4,5,10
7	tAA	Access Time from Column Address	-	25	-	30	-	35	ns	4,5,11
8	tCPA	Access Time from /CAS Precharge	-	30	-	35	-	40	ns	4
9	tCLZ	/CAS to Output Low Impedance	0	-	0	-	0	-	ns	3
10	tCEZ	Out Buffer Turn-off delay from /CAS	0	10	0	15	0	15	ns	
11	t_T	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	4
12	tRP	/RAS Precharge Time	30	-	40	-	50	-	ns	
13	tRAS	/RAS Pulse Width	50	10K	60	10K	70	10K	ns	
14	tRASP	/RAS Pulse Width (EDO Mode)	50	100K	60	100K	70	100K	ns	
15	tRSH	/RAS Hold Time	15	-	15	-	20	-	ns	
16	tCSH	/CAS Hold Time	45	-	55	-	65	-	ns	
17	tCAS	/CAS Pulse Width	8	10K	10	10K	15	10K	ns	
18	tRCD	/RAS to /CAS Delay	15	37	20	45	20	50	ns	10
19	tRAD	/RAS to Column Address Delay Time	10	25	15	30	15	35	ns	11
20	tCRP	/CAS to /RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	/CAS Precharge Time	8	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	8	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	8	-	10	-	15	-	ns	
26	tAR	Column Address Hold Time from /RAS	45	-	50	-	55	-	ns	
27	tRAL	Column Address to /RAS Lead Time	25	-	30	-	35	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to /CAS	0	-	0	-	0	-	ns	7
30	tRRH	Read Command Hold Time Referenced to /RAS	0	-	0	-	0	-	ns	7
31	tWCH	Write Command Hold Time	10	-	10	-	10	-	ns	
32	tWCR	Write Command Hold Time from /RAS	40	-	45	-	50	-	ns	
33	tWP	Write Command Pulse Width	10	-	10	-	10	-	ns	
34	tRWL	Write Command to /RAS Lead Time	15	-	15	-	20	-	ns	
35	tCWL	Write Command to /CAS Lead Time	8	-	10	-	15	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	8
37	tDH	Data-In Hold Time	10	-	10	-	10	-	ns	8
38	tDHR	Data-In Hold Time Referenced to /RAS	40	-	45	-	50	-	ns	

AC CHARACTERISTICS

(Continued)

#	SYMBOL	PARAMETER	HY51V64164 / HY51V65164						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
39	tREF	Refresh Period (8192 cycles)	-	64	-	64	-	64	ms	12,13
		Refresh Period (4096 cycles)	-	64	-	64	-	64	ms	12
		Refresh Perion (SL-part)	-	128	-	128	-	128	ms	12,13
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	9
41	tCWD	/CAS to WE Delay Time	34	-	36	-	45	-	ns	9
42	tRWD	/RAS to WE Delay Time	70	-	80	-	95	-	ns	9
43	tAWD	Column Address to /WE Delay Time	45	-	50	-	60	-	ns	9
44	tCSR	/CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	/CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRPC	/RAS to /CAS Precharge Time	5	-	5	-	5	-	ns	
47	tCPT	/CAS Precharge Time (CBR Counter Test)	25	-	30	-	35	-	ns	
48	tROH	/RAS Hold Time Reference to /OE	0	-	0	-	0	-	ns	
49	tOEA	/OE Access Time	-	13	-	15	-	20	ns	
50	tOED	/OE to Data Delay	13	-	15	-	20	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from /OE	0	10	0	15	0	15	ns	6
52	tOEH	/OE Command Hold Time	13	-	15	-	20	-	ns	
53	tCPWD	/WE Delay Time from /CAS Precharge	45	-	54	-	64	-	ns	9
54	tRHCP	/RAS Hold Time from /CAS Precharge	30	-	35	-	40	-	ns	
55	tWRP	/WE to /RAS Precharge Time(CBR cycle)	10	-	10	-	10	-	ns	
56	tWRH	/WE to /RAS Hold Time (CBR cycle)	10	-	10	-	10	-	ns	
57	tWTS	Write Command Set-up Time (Test Mode In)	10	-	10	-	10	-	ns	
58	tWTH	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
59	tRASS	/RAS Pulse Width (Self Refresh)	100K	-	100K	-	100K	-	us	
60	tRPS	/RAS Precharge Time (Self Refresh)	100	-	110	-	130	-	ns	
61	tCHS	/CAS Hold Time (Self Refresh)	-50	-	-50	-	-50	-	ns	
62	tDOH	Output Data Hold Time	5	-	5	-	5	-	ns	
63	tREZ	Output Buffer Turn- off Delay from /RAS	0	10	0	15	0	15	ns	6
64	tWEZ	Output Buffer Turn- off Delay from /WE	0	10	0	15	0	15	ns	6
65	tWED	/WE to Data Delay Time	15	-	15	-	15	-	ns	
66	tOEP	/OE Precharge Time	5	-	5	-	5	-	ns	
67	tWPE	/WE Pulse Width (EDO cycle)	5	-	5	-	5	-	ns	
68	tOCH	/OE to /CAS Hold Time	5	-	5	-	5	-	ns	
69	tCHO	/CAS Hold Time to /OE	5	-	5	-	5	-	ns	

TEST MODE

#	SYMBOL	PARAMETER	HY51V64164 / HY51V65164						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	95	-	115	-	135	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	125	-	145	-	175	-	ns	
3	tHPC	EDO Mode Cycle Time	25	-	30	-	35	-	ns	
4	tHPRWC	EDO Mode Read-Modify-Write Cycle Time	55	-	65	-	80	-	ns	
5	tRAC	Access Time from /RAS	-	55	-	65	-	75	ns	4,5,10,11
6	tCAC	Access Time from /CAS	-	18	-	20	-	25	ns	4,5,10
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,5,11
8	tCPA	Access Time from Column Precharge	-	35	-	40	-	45	ns	4
13	tRAS	/RAS Pulse Width	55	10K	65	10K	75	10K	ns	
14	tRASP	/RAS Pulse Width (EDO Mode)	55	100K	65	100K	75	100K	ns	
15	tRSH	/RAS Hold Time	20	-	20	-	25	-	ns	4
16	tCSH	/CAS Hold Time	50	-	60	-	70	-	ns	
17	tCAS	/CAS Pulse Width	13	10K	15	10K	20	10K	ns	
27	tRAL	Column Address to /RAS Lead Time	30	-	35	-	40	-	ns	
41	tCWD	/CAS to /WE Delay Time	39	-	41	-	50	-	ns	
42	tRWD	/RAS to /WE Delay Time	75	-	85	-	100	-	ns	
43	tAWD	Column Address to /WE Delay Time	50	-	55	-	65	-	ns	9
49	tOEA	/OE Access Time	-	18	-	20	-	25	ns	
50	tOED	/OE to Data Delay	18	-	20	-	25	-	ns	
52	tOEH	/OE Command Hold Time	18	-	20	-	25	-	ns	
53	tCPWD	/WE Delay Time from /CAS Precharge	50	-	59	-	69	-	ns	9

The HY51V64(5)164 is a DRAM organized 4Mx16 bit. It is internally organized 2Mx32 bit. In Test Mode, data are written into 8 sectors(each is composed of 8M bits) in parallel, and each sector receive 4 data from 2 DQ's. Column address A8 is not used(with 4K refresh, A9 is not used). If upon reading, 16 bits data from 4 sectors are equal, then the DQ0 indicates `1`. If they are not equal, then the DQ0 indicates `0`. Similarly, with the rest of 4 sectors the DQ8 indicates `1` or `0` according to. Belowing shows the timing diagram of the HY51V64(5)164 to enter Test Mode. In Test Mode. the 4Mx16 DRAM can be tested as if it were a 2Mx32 DRAM. /WE, /CAS-Before-/RAS cycle(Test Mode in cycle) puts the HY51V64(5)164 into Test Mode and /CAS-Before-/RAS or /RAS-only refresh cycle put it back into Normal Mode. In Test Mode, /WE, /CAS-Before-/RAS cycle shall be used for the refresh operation. The Test Mode function reduces test time (1/2 in case of N test pattern).

NOTE

1. An initial pause of 200 μs is required after power-up followed by 8 /RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 /CAS-before-/RAS initialization cycles instead of 8 /RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode during initialization.
2. If /RAS=Vss during power-up, the HY51V64164, HY51V65164 could begin an active cycle. This condition results in higher current than necessary current which is demanded from the power supply during power-up.
3. It is recommended that /RAS and /CAS track with Vcc during power-up or be held at a valid V_{IH} in order to minimize the power-up current.
4. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min.) and V_{IL}(max.), and are assumed to be 5ns for all inputs.
5. Measured at V_{OH}=2.0V and V_{OL}=0.8V with a load equivalent to 1 TTL loads and 100pF.
6. tWEZ, tREZ, tCEZ and tOEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to /CAS leading edge in early write cycles and to /WE leading edge in Read-Modify-Write cycles and late Write cycle.
9. tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS $\geq$ tWCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If tRWD $\geq$ tRWD(min.), tCWD $\geq$ tCWD(min.), tAWD $\geq$ tAWD(min.), and tCPWD $\geq$ tCPWD(min.), the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
10. Operation within the tRCD(max.) limit ensures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
11. Operation within the tRAD(max.) limit ensures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
12. tREF(max.)=128ms is applied to L-parts and SL-parts.
13. A burst of 8192 /CAS-before-/RAS refresh cycles must be executed within 64ms (128ms for L-parts) after exiting self refresh. (CBR refresh & Hidden refresh : 4K cycle/64ms)

CAPACITANCE

(T_A=0℃ to 70℃, Vcc=3.3V ± 10%, Vss=0V, f = 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0 - A12)	-	5	pF
C_{IN1}	Input Capacitance (/RAS, /CAS, /WE, /OE)	-	7	pF
C_{DQ}	Data Input /Output Capacitance (DQ0 - DQ15)	-	7	pF