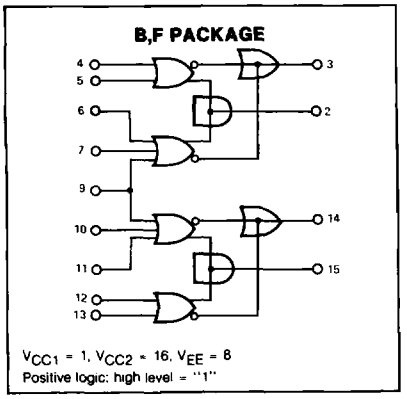
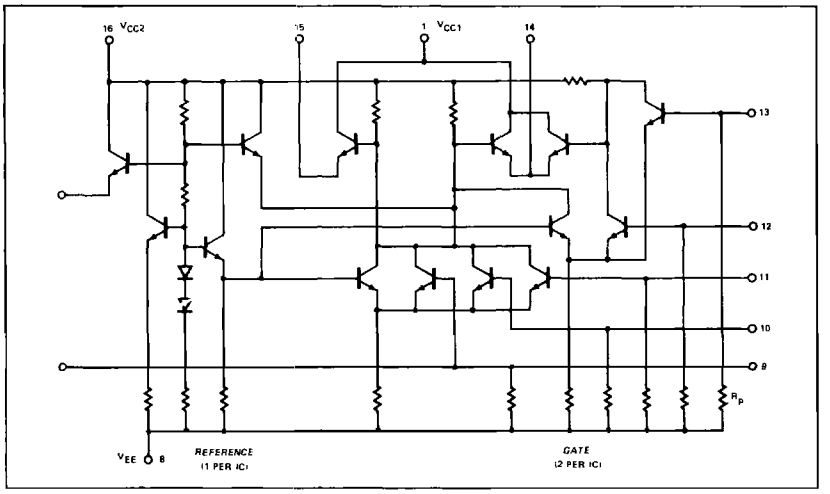
10117-B,F

LOGIC DIAGRAM



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
Positive logic: high level = "1"

CIRCUIT SCHEMATIC

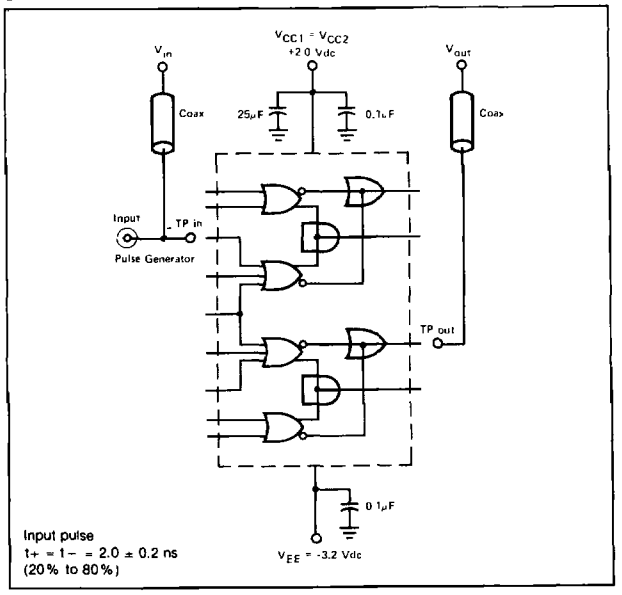


FEATURES

- **Fast propagation delay for two logic levels = 2.3 ns TYP**
- **Power dissipation = 100 mW/package TYP (no load)**
- **Very high fanout capability — can drive 50Ω lines**
- **High Z inputs — 50 kΩ pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2V ±5% recommended**
- **Open emitters for bussing and logic capability**
- **Outputs may be cross coupled back to inputs to make a latch function**

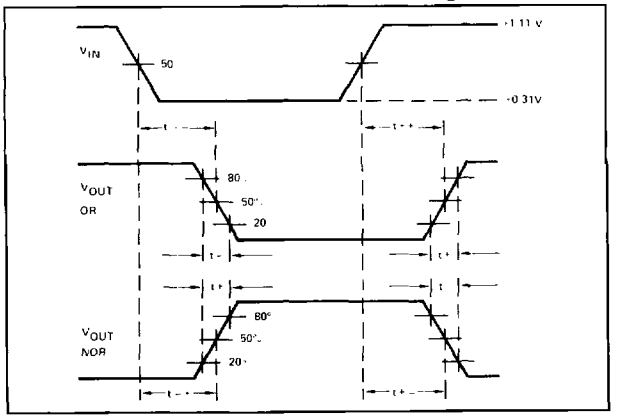
LOGIC

SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25° C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < ¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.