November 21, 2006

Notice – PMC Product Support Scope for Specified HDMP Part Numbers

Distribution:

This notice has been added to the front of the datasheets for the “Devices Affected” listed below.

Description:

PMC-Sierra has acquired the Fibre Channel/Storage and Gigabit Ethernet Port Bypass Controllers and SERDES/PHY products of Agilent/Avago Technologies. This notice is to inform customers that PMC-Sierra is supporting these devices for existing production designs only. PMC-Sierra will only provide support for the migration of an existing design from a Pb package to a Pb-free package. The devices are not intended for new designs and PMC-Sierra will not provide support for new designs.

Devices Affected:

Device	Data Sheet	Device	Data Sheet	Device	Data Sheet
HDMP-0421G	PMC-2060481*	HDMP-1022G	PMC-2060487	HDMP-1638G	PMC-2060490
HDMP-0422G	PMC-2060482*	HDMP-1024G	PMC-2060487	HDMP-1646AG	PMC-2060491
HDMP-0450G	PMC-2060483	HDMP-1032AG	PMC-2060488	HDMP-1646AGR1	PMC-2060491
HDMP-0451G	PMC-2060484	HDMP-1034AG	PMC-2060488	HDMP-1687G	PMC-2060493
HDMP-0452G	PMC-2060485*	HDMP-1536AG	PMC-2060489	HDMP-T1636AG	PMC-2060491
HDMP-0480G	PMC-2062505*	HDMP-1636AG	PMC-2060491		
HDMP-0482G	PMC-2060486	HDMP-1636AGR1	PMC-2060491		

* Note – These data sheets have part numbers that reference Pb packaging. All part numbers listed above are for Pb-free packaging.

Customer Response

This notice is for customer information only and no customer response is required. If you have any questions or concerns please contact your local PMC-Sierra Sales Representative listed at this link http://www.pmc-sierra.com/contactSales/

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HDMP-0482G
Octal Cell Port Bypass Circuit with CDR and Data Valid Detection
Data Sheet

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Description

The HDMP-0482G is an Octal Cell Port Bypass Circuit (PBC) with Clock and Data Recovery (CDR) and data valid detection capability included. This device minimizes part count, cost and jitter accumulation while repeating incoming signals. Port Bypass Circuits are used in hard disk arrays constructed in Fibre Channel Arbitrated Loop (FC-AL) configurations. By using Port Bypass Circuits, hard disks may be pulled out or swapped while other disks in the array are available to the system.

A Port Bypass Circuit (PBC) consists of multiple 2:1 multiplexers daisy chained along with a CDR. Each port has two modes of operation: "disk in loop" and "disk bypassed". When the "disk in loop" mode is selected, the loop goes into and out of the disk drive at that port. For example, data goes from the HDMP-0482G's TO_NODE[n]± differential output pins to the Disk Drive Transceiver IC's (e.g. an HDMP-1636AG) Rx± differential input pins. Data from the Disk Drive Transceiver IC's Tx± differential outputs goes to the HDMP-0482G's FM_NODE[n]± differential input pins. When the "disk bypassed" mode is selected, the disk drive is either absent or non-functional and the loop bypasses the hard disk.

The "disk bypassed" mode is enabled by pulling the BYPASS[n]- pin low. Leave BYPASS[n]- floating to enable the "disk in loop" mode. HDMP-0482G's may be cascaded with other members of the HDMP-04XXG/HDMP-05XXG family through the FM_NODE and TO_NODE pins to accommodate any number of hard disks. The unused cells in this PBC may be bypassed by using pulldown resistors on the BYPASS[n]- pins for these cells.

An HDMP-0482G may also be used as eight 1:1 buffers, one with a CDR and seven without. For example, an HDMP-0482G may be placed in front of a CMOS ASIC to clean the jitter of the outgoing signal (CDR path) and to better read the incoming signal (non-CDR path). In addition, the HDMP-0482G may be configured as four 2:1 multiplexers or as four 1:2 buffers.

CAUTION: As with all semiconductor ICs, it is advised that normal static precautions be taken in the handling and assembly of this component to prevent damage and/or degradation which may be induced by electrostatic discharge (ESD).

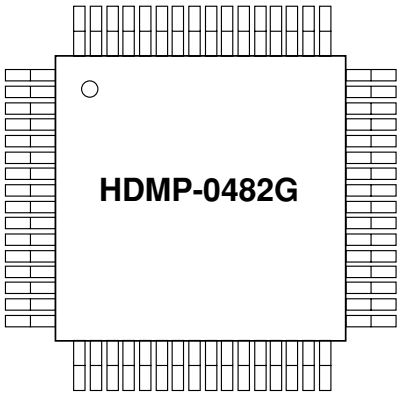
Features

- **Supports 1.0625 GBd fibre channel operation**
- **Supports 1.25 GBd Gigabit Ethernet (GE) operation**
- **Octal cell PBC/CDR in one package**
- **CDR location determined by choice of cable input/output**
- **Amplitude valid detection on FM_NODE[7] input**
- **Data valid detection on FM_NODE[0] input**
  - **– Run length violation detection**
  - **– Comma detection**
  - **– Configurable for both single-frame and multi-frame detection**
- **Equalizers on all inputs**
- **High speed LVPECL I/O**
- **Buffered Line Logic (BLL) outputs (no external bias resistors required)**
- **1.09 W typical power at Vcc=3.3V**
- **64 Pin, 14 mm, low cost plastic QFP package**

This part is RoHS compliant and Pb-free.

Applications

- **RAID, JBOD, BTS cabinets**
- **Four 2:1 muxes**
- **Four 1:2 buffers**
- **1 = > N gigabit serial buffer**
- **N = > 1 gigabit serial mux**



The HDMP-0482G design allows for CDR placement at any location with respect to the hard disk slots. For example, if the BYPASS[0]- pin is floating and hard disk slots A to G are connected to PBC cells 1 to 7, respectively, the CDR function will be performed before entering the hard disk at slot A. To obtain a CDR function after slot G, BYPASS[1]- must be floating and hard disk slots A to G must be connected to PBC cells 2,3,4,5,6,7 and 0, respectively. Table 1 shows all possible connections.

For configurations where the CDR is before slot A, a Data Valid (FM_NODE[0]_DV) pin indicates whether the incoming data on FM_NODE[0]± is valid Fibre Channel data. In addition, an Amplitude Valid (FM_NODE[7]AV) pin shows the status of the signal at FM_NODE[7].

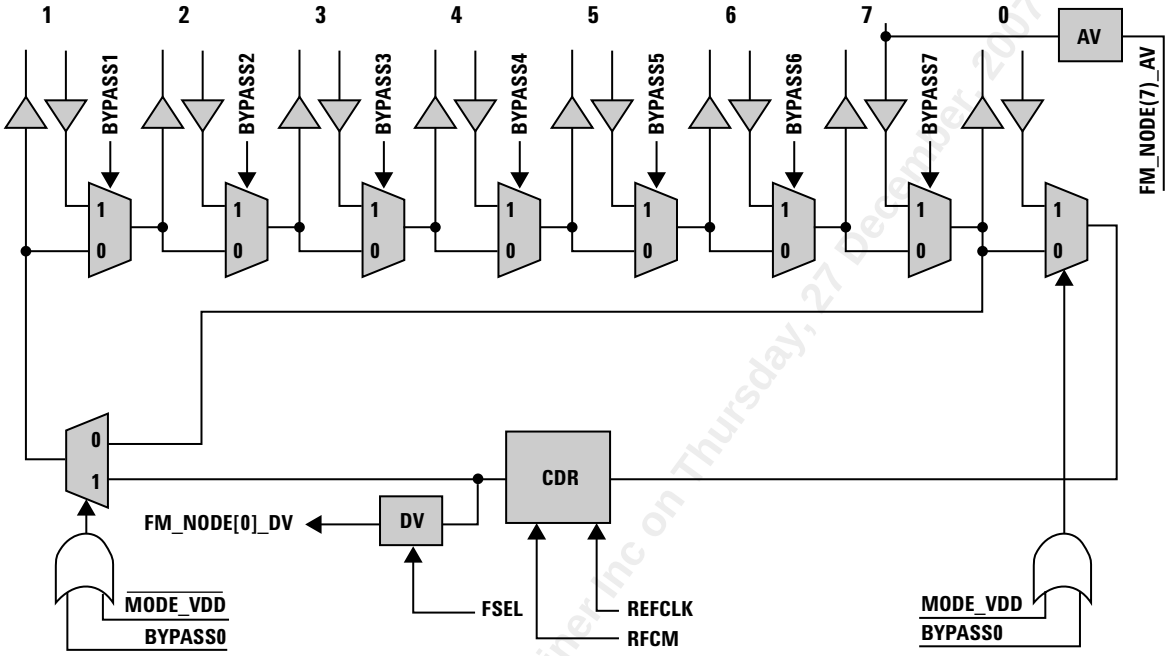


Figure 1. Block Diagram of HDMP-0482G.

HDMP-0482G Block Diagram

CDR

The Clock and Data Recovery (CDR) block is responsible for frequency and phase locking onto the incoming serial data stream and resampling the incoming data based on the recovered clock. An automatic locking feature allows the CDR to lock onto the input data stream without external training controls. It does this by continually frequency locking onto the 106.25 MHz reference clock (REFCLK) and then phase locking onto the input data stream. Once bit locked, the CDR generates a high-speed sampling clock. This clock is used to sample or repeat the incoming data to produce the CDR output. The CDR jitter specifications listed in this data sheet assume an input that has been 8B/10B encoded.

DV Output

The Data Valid (DV) block detects if the incoming data on FM_NODE[0]± is valid Fibre Channel data. The DV checks for sufficient K28.5+ characters (per Fibre Channel framing rules) and for run length violations (per 8B/10B encoding) on the data coming out of the CDR. The FM_NODE[0]_DV output is pulled low if a run length violation (RLV) occurs, or if there are no commas detected (NCD) in a sufficient time. It is pulled high if no errors are found. A RLV error is defined as any consecutive sequence of 1s or 0s greater than five in the serial data bit stream. A NCD error indicates the absence of a seven-bit pattern (0011111) present in the positive disparity comma (K28.5+) character. A K28.5+ character should occur at the beginning of every Fibre Channel frame of 2148 bytes (or 21480 serial bits), as well as many times within and between frames. If this seven-bit pattern is not found within a 2^{15} bit (~31 µs) interval, an NCD error is generated.

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When the DV is configured in single-frame mode (FSEL low), any RLV and NCD errors stored during this 2^{15} bit interval cause FM_NODE[0]_DV to be pulled low on the next subsequent interval. FM_NODE[0]_DV remains low until after an entire 2^{15} bit interval in which no RLVs occur and at least one comma is detected. At that time, FM_NODE[0]_DV is pulled high. A multi-frame mode (FSEL high) configuration of the DV is also available. When in multi-frame mode, the FM_NODE[0]_DV output is only pulled low when four consecutive 2^{15} bit intervals of bad data have been transmitted. Once low, FM_NODE[0]_DV does not go high again until four consecutive 2^{15} bit intervals of good data are transmitted.

AV Output

The Amplitude Valid (AV) block detects if the incoming data on FM_NODE[7]± is valid by examining the differential amplitude of that input. The incoming data is considered valid, and FM_NODE[7]_AV is driven high, as long as the amplitude is greater than 400 mV (differential peak-to-peak). FM_NODE[7]_AV is driven low as long as the amplitude of the input signal is less than 100 mV (differential peak-to-peak). When the amplitude of the input signal is between 100–400 mV (differential peak-to-peak), FM_NODE[7]_AV is unpredictable. The FM_NODE[7]_AV output is latched in with an internally generated 2^{15} bit clock. Similar to the DV function, the AV can be configured for single-frame or multi-frame operation.

BLL Output

All TO_NODE[n]± high-speed differential outputs are driven by a Buffered Line Logic (BLL) circuit that has on-chip source termination, so no external bias resistors are required. The BLL Outputs on the HDMP-0482G are of equal strength and can drive in excess of 120 inches of FR-4 PCB trace. Unused outputs should not be left unconnected. Ideally, unused outputs should have their differential pins shorted together with a short PCB trace. If transmission lines are connected to the output pins, the lines should be differentially terminated with an appropriate resistor. The value of the termination resistor should match the PCB trace differential impedance.

EQU Input

All FM_NODE[n]± high-speed differential inputs have an Equalization (EQU) buffer to offset the effects of skin loss and dispersion on PCBs. An external termination resistor is required across all high-speed inputs.

BYPASS[N]- Input

The active low BYPASS[n]- inputs control the data flow through the HDMP-0482G. All BYPASS pins are LVTTL and contain internal pull-up circuitry. To bypass a port, the appropriate BYPASS[n]- pin should be connected to GND through a 1kΩ resistor. Otherwise, the BYPASS[n]- inputs should be left to float. In this case, the internal pull-up circuitry will force them high.

REFCLK Input

The LVTTL REFCLK input provides a reference oscillator for frequency acquisition of the CDR. The REFCLK frequency should be within ±100 ppm of one-tenth or one-twentieth of the incoming data rate in baud (106.25 MHz ±100 ppm, or 53.125 MHz ±100 ppm for FC-AL running at 1.0625 GBd).

RFCM Input

The LVTTL RFCM input configures the CDR to accept a REFCLK at either one-tenth or one-twentieth of the incoming data rate in baud. The RFCM input has internal pull-up circuitry, so the user should connect the pin to GND through a 1kΩ resistor for a REFCLK at one-twentieth the incoming data rate. For a REFCLK at one-tenth the incoming data rate, let RFCM float high.

MODE_VDD Input

The active high valid data detect mode pin selects data checking of the FM_NODE [0] +/- inputs. When high, MODE_VDD overides BYPASS [0] and forces the incoming data into the CDR for error checking. When low, the chip can be configured for CDR anywhere capability. Refer to Figures 2 & 3 for high and low MODE_VDD configuration.

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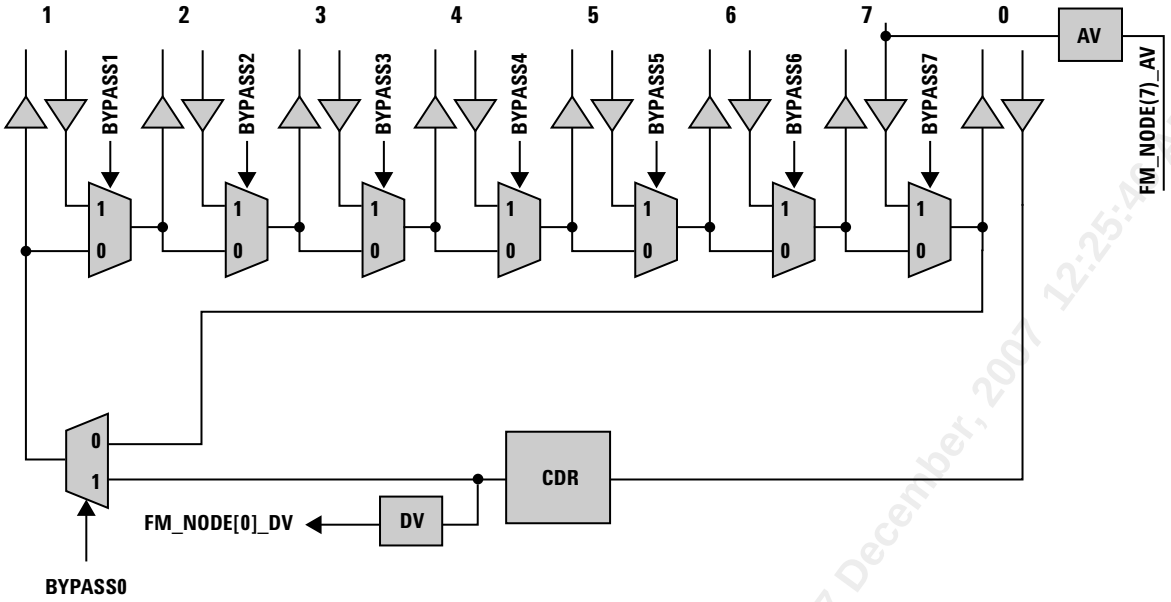

Figure 2. Block Diagram of HDMP-0482G, MODE_VDD is HIGH.

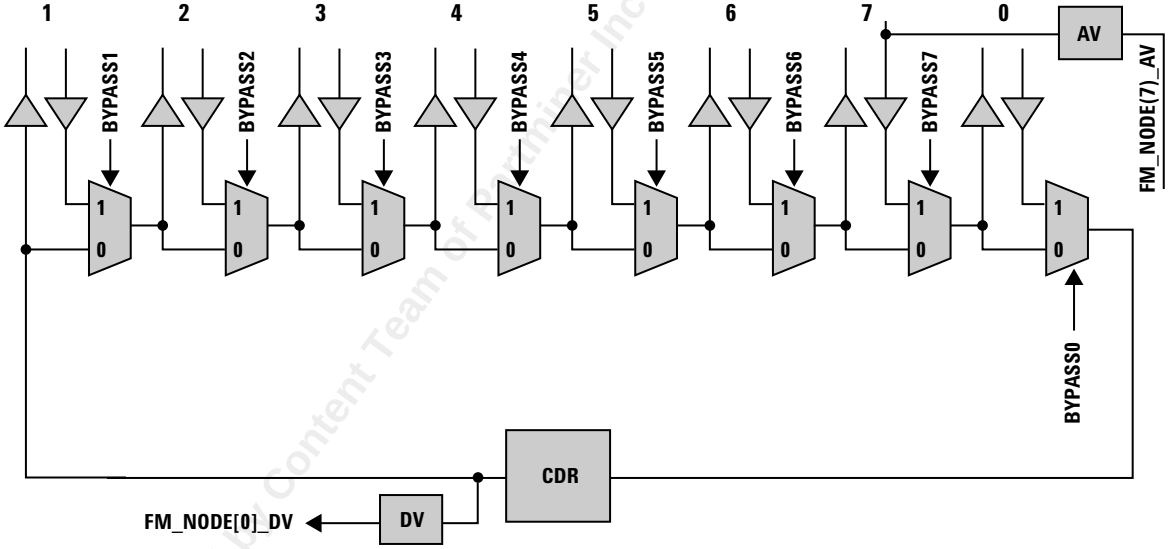

Figure 3. Block Diagram of HDMP-0482G, MODE_VDD is LOW.

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Table 1. Pin Connection Diagram to Achieve Desired CDR Location.

Hard Disk	A B C D E F G	A B C D E F G	A B C D E F G	A B C D E F G
Connection to PBC Cell	1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4
CDR Position (x)	xA B C D E F G	AxB C D E F G	A BxC D E F G	A B CxD E F G
Cell Connection to Cable	0	7	6	5

Hard Disk	A B C D E F G	A B C D E F G	A B C D E F G	A B C D E F G
Connection to PBC Cell	5 6 7 0 1 2 3	4 5 6 7 0 1 2	3 4 5 6 7 0 1	2 3 4 5 6 7 0
CDR Position (x)	A B C DxE F G	A B C D ExF G	A B C D E FxG	A B C D E F Gx
Cell Connection to Cable	4	3	2	1

x denotes CDR position with respect to hard disks.

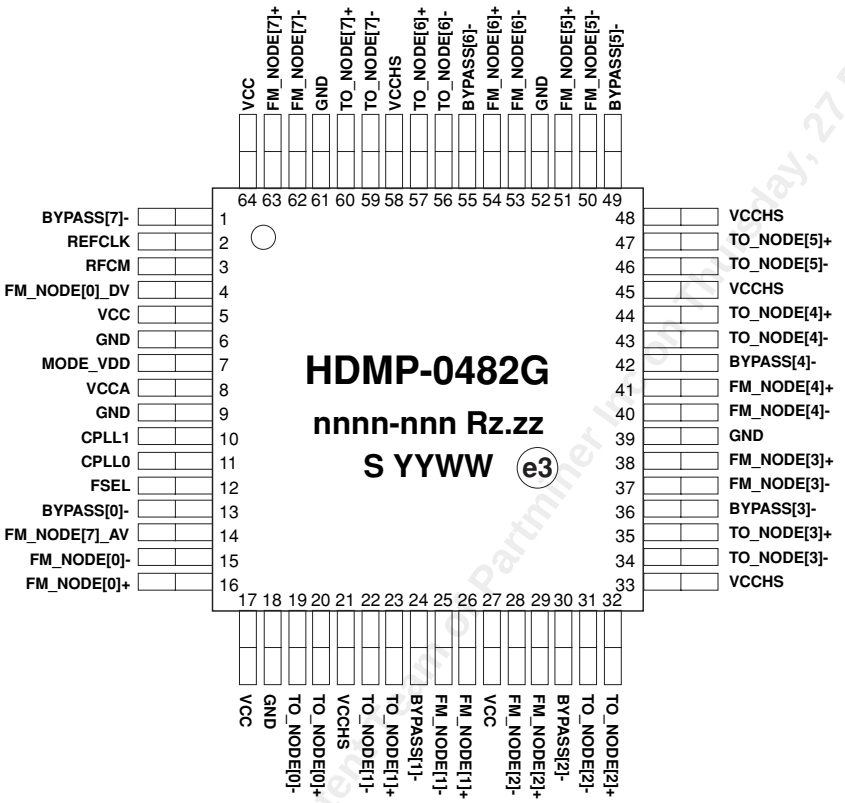

Figure 4. HDMP-0482G Package Layout and Marking, Top View.
nnnn-nnn = wafer lot - build number; Rz.zz = Die Revision; S = Supplier Code; YYWW = Date Code (YY = year, WW = work week); (e3) = JESD97 Pb-free category; COUNTRY = country of manufacture (on back side).

Table 2. I/O Type Definitions.

I/O Type	Definition
I-LVTTL	LVTTL Input
O-LVTTL	LVTTL Output
HS_OUT	High Speed Output, LVPECL Compatible
HS_IN	High Speed Input
C	External circuit node
S	Power supply or ground

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Table 3. Pin Definitions for HDMP-0482G.

Pin Name	Pin	Pin Type	Pin Description
TO_NODE[0]+ TO_NODE[0]- TO_NODE[1]+ TO_NODE[1]- TO_NODE[2]+ TO_NODE[2]- TO_NODE[3]+ TO_NODE[3]- TO_NODE[4]+ TO_NODE[4]- TO_NODE[5]+ TO_NODE[5]- TO_NODE[6]+ TO_NODE[6]- TO_NODE[7]+ TO_NODE[7]-	20 19 23 22 32 31 35 34 44 43 47 46 57 56 60 59	HS_OUT	**Serial Data Outputs**: High-speed outputs to a hard disk drive or to a cable input.
FM_NODE[0]+ FM_NODE[0]- FM_NODE[1]+ FM_NODE[1]- FM_NODE[2]+ FM_NODE[2]- FM_NODE[3]+ FM_NODE[3]- FM_NODE[4]+ FM_NODE[4]- FM_NODE[5]+ FM_NODE[5]- FM_NODE[6]+ FM_NODE[6]- FM_NODE[7]+ FM_NODE[7]-	16 15 26 25 29 28 38 37 41 40 51 50 54 53 63 62	HS_IN	**Serial Data Inputs**: High-speed inputs from a hard disk drive or from a cable output.
BYPASS[0]- BYPASS[1]- BYPASS[2]- BYPASS[3]- BYPASS[4]- BYPASS[5]- BYPASS[6]- BYPASS[7]-	13 24 30 36 42 49 55 1	I-LVTTL	**Bypass Inputs**: For "disk bypassed" mode, connect BYPASS[n]- to GND through a1kΩ resistor. For "disk in loop" mode, float HIGH.
REFCLK	2	I-LVTTL	**Reference Clock**: A user-supplied clock reference used for frequency acquisition in the Clock and Data Recovery (CDR) circuit.
CPLL1 CPLL0	10 11	C	**Loop Filter Capacitor**: A loop filter capacitor for the internal Clock and Data Recovery (CDR) circuit must be connected across the CPLL1 and CPLL0 pins. Recommended value is 0.1 μF.
FM_NODE[7]_AV	14	O-LVTTL	**Amplitude Valid**: Indicates acceptable signal amplitude on the FM_NODE[7]± inputs. If (FM_NODE[7]+ - FM_NODE[7]-) >= 400 mV peak-to-peak, FM_NODE[7]_AV = 1 If 400 mV > (FM_NODE[7]+ - FM_NODE[7]-) > 100 mV, FM_NODE[7]_AV = unpredictable If 100 mV >= (FM_NODE[7]+ - FM_NODE[7]-), FM_NODE[7]_AV = 0
FM_NODE[0]_DV	4	O-LVTTL	**Data Valid**: Indicates valid Fibre Channel Data on the FM_NODE[0]± inputs when HIGH. Indicates either run length violation error or no comma detected when LOW.
RFCM	3	I-LVTTL	**Reference Clock Mode**: To configure a one-twentieth-rate reference clock, connect RFCM to GND through a 1kΩ resistor. To configure a one-tenth-rate reference clock, float RFCM HIGH.
MODE_VDD	7	I_LVTTL	**Valid Data Detect Mode**: To allow data valid detection, float MODE_VDD HIGH. To configure chip for "CDR anywhere" capability, connect MODE_VDD to GND through a 1kΩ resistor.
FSEL	12	I_LVTTL	**Frame Select**: To configure single-frame operation of the data valid and amplitude valid detection circuits, connect FSEL to GND through a 1k resistor. To configure multi-frame (4-frame) operation of the data valid and amplitude valid detection circuits, float FSEL HIGH.

Table 3 is continued on next page.

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Table 3, continued. Pin Definitions for HDMP-0482G.

Pin Name	Pin	Pin Type	Pin Description
GND	6 9 18 39 52 61	S	**Ground**: Normally 0 volts. See Figure 11 for Recommended Power Supply Filtering.
VCCA	8	S	**Analog Power Supply**: Normally 3.3 volts. Used to provide a clean supply line for the Clock and Data Recovery (CDR) circuit. See Figure 11 for Recommended Power Supply Filtering.
VCCHS[0,1] VCCHS[2,3] VCCHS[4] VCCHS[5] VCCHS[6,7]	21 33 45 48 58	S S S S S	**High Speed Supply**: Normally 3.3 volts. Used only for high-speed outputs (TO_NODE[n]). See Figure 11 for Recommended Power Supply Filtering.
VCC	5 17 27 64	S S S S	**Logic Power Supply**: Normally 3.3 volts. Used for internal logic. See Figure 11 for Recommended Power Supply Filtering.

HDMP-0482G Absolute Maximum Ratings

T_a=25° C, except as specified. Operation in excess of any of these conditions may result in permanent damage to this device. T_a refers to the ambient temperature for the board upon which the parametric measurements were taken.

Symbol	Parameters	Min.	Max.	Units
V_{CC}	Supply Voltage	-0.7	4.0	V
$V_{IN, LVTTL}$	LVTTL Input Voltage	-0.7	4.0	V
V_{IN, HS_IN}	HS_IN Input Voltage	1.3	V_{CC}	V
$I_{O, LVTTL}$	LVTTL Output Voltage		±13	mA
T_{stg}	Storage Temperature	-65	+150	°C
T_j	Junction Temperature	0	+125	°C

HDMP-0482G Guaranteed Operating Rates, T_a = 0°C to +70°C, V_{CC} = 3.15V to 3.45V

Serial Clock Rate FC (MBd)		Serial Clock Rate GE (MBd)	
Min.	Max.	Min.	Max.
1,040	1,080	1,240	1,260

HDMP-0482G CDR Reference Clock Requirements, T_a = 0°C to +70°C, V_{CC} = 3.15V to 3.45V

Symbol	Parameter	Min.	Typ.	Max.	Units
f	Nominal Frequency (Fibre Channel)		106.25		MHz
f	Nominal Frequency (Gigabit Ethernet)		125		MHz
Ftol	Frequency Tolerance	-100		100	ppm
Symm	Symmetry (duty cycle)	40		60	%

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HDMP-0482G DC Electrical Specifications, T_a = 0°C to +70°C, V_{CC} = 3.15V to 3.45V

Symbol	Parameter	Min.	Typ.	Max.	Units
$V_{IH,LVTTL}$	LVTTL Input High Voltage Range	2.0		4.0	V
$V_{IL,LVTTL}$	LVTTL Input Low Voltage Range	0		0.8	V
$V_{OH,LVTTL}$	LVTTL Output High Voltage Range, I_{OH} = -400 µA	2.2		3.45	V
$V_{OL,LVTTL}$	LVTTL Output Low Voltage Level, I_{OL} = 1 mA	0		0.6	V
$I_{IH,LVTTL}$	Input High Current (Magnitude), V_{IN} = 2.4 V, V_{CC} = 3.45 V		.003	40	µA
$I_{IL,LVTTL}$	Input Low Current (Magnitude), V_{IN} = 0.4 V, V_{CC} = 3.45 V		300	600	µA
I_{CC}	Total Supply Current, T_a = 25°C		330	400	mA

HDMP-0482G AC Electrical Specifications, T_a = 0°C to +70°C, V_{CC} = 3.15V to 3.45V

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{loop}	Total Loop Latency from FM_NODE[0] to TO_NODE[0]		2.8	4.2	ns
t_{cell}	Per Cell Latency from FM_NODE[7] to TO_NODE[0]		0.5	0.8	ns
$t_{r,LVTTLin}$	Input LVTTL Rise Time Requirement, 0.8 V to 2.0 V		2		ns
$t_{f,LVTTLin}$	Input LVTTL Fall Time Requirement, 2.0 V to 0.8 V		2		ns
t_{rs,HS_OUT}	HS_OUT Single-Ended Rise Time, 20%-80%		200	350	ps
t_{fs,HS_OUT}	HS_OUT Single-Ended Rise Time, 20%-80%		200	350	ps
t_{rd,HS_OUT}	HS_OUT Differential Rise Time, 20%-80%		200	350	ps
t_{fd,HS_OUT}	HS_OUT Differential Rise Time, 20%-80%		200	350	ps
V_{IP,HS_IN}	HS_IN Input Peak to Peak Required Differential Voltage Range	400	1200	2000	mV
V_{OP,HS_OUT}	HS_OUT Output Pk-Pk Diff. Voltage Range (Z0 = 75Ω, Fig. 9)	1100	1400	2000	mV

HDMP-0482G Power Dissipation, T_a = 0°C to +70°C, V_{CC} = 3.15V to 3.45V

Symbol	Parameter	Unit	Typ.	Max.
P_D	Power Dissipation	mW	1090	1380

HDMP-0482G Output Jitter Characteristics, T_a = 0°C to +70°C, V_{CC} = 3.15V to 3.45V

Symbol	Parameter	Unit	Typ.	Max.
RJ	Random Jitter at TO_NODE pins (1 sigma rms)	ps	5	
DJ	Deterministic Jitter at TO_NODE pins (pk-pk)	ps	24	

Please refer to Figures 6 and 7 for jitter measurement setup information.

HDMP-0482G Locking Characteristics, T_a = 0°C to +70°C, V_{CC} = 3.15V to 3.45V

Parameter	Unit	Max.
Bit Sync Time (phase lock)	bits	2500
Frequency Lock at Powerup	µs	500

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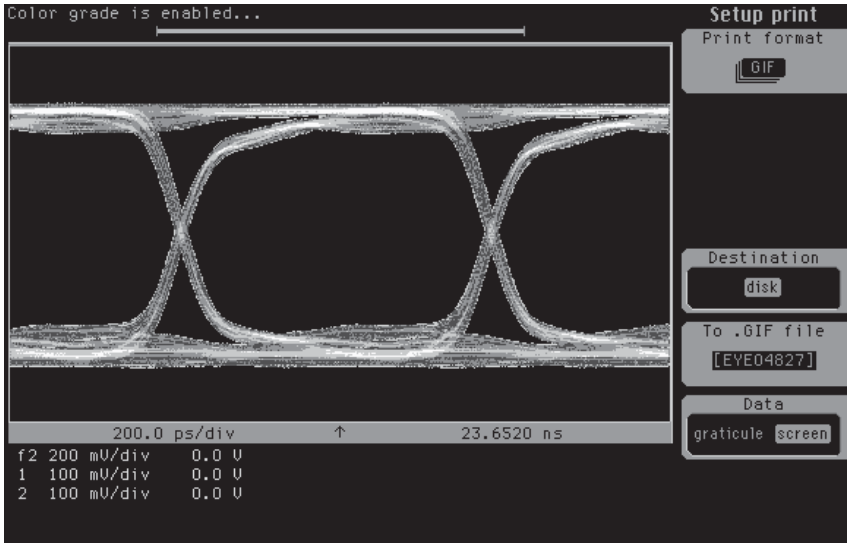

Figure 5. Eye Diagram of TO_NODE[1]± High Speed Differential Output.

Note: Measurement taken with a 2^7-1 PRBS input to FM_NODE[0]±.

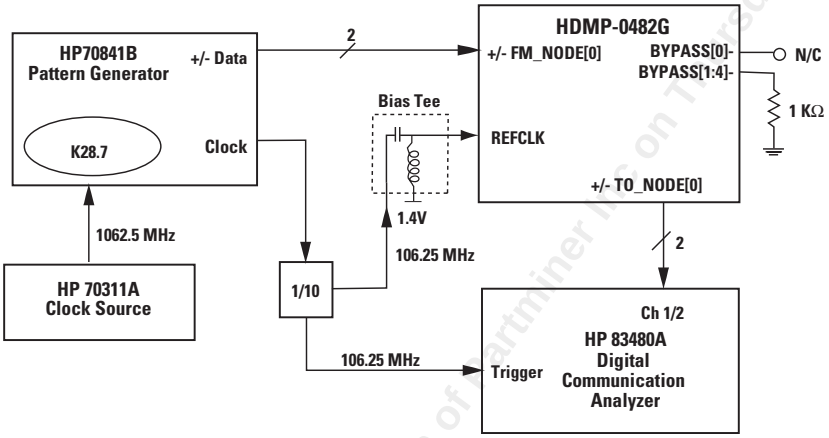

Figure 6. Setup for Measurement of Random Jitter.

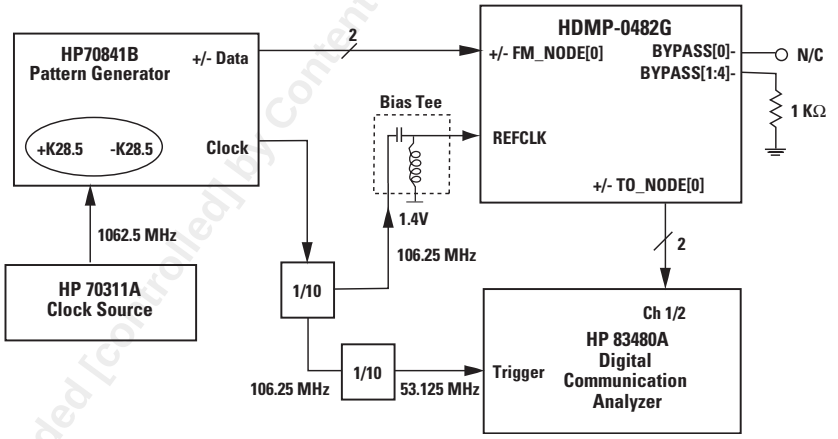

Figure 7. Setup for Measurement of Deterministic Jitter.

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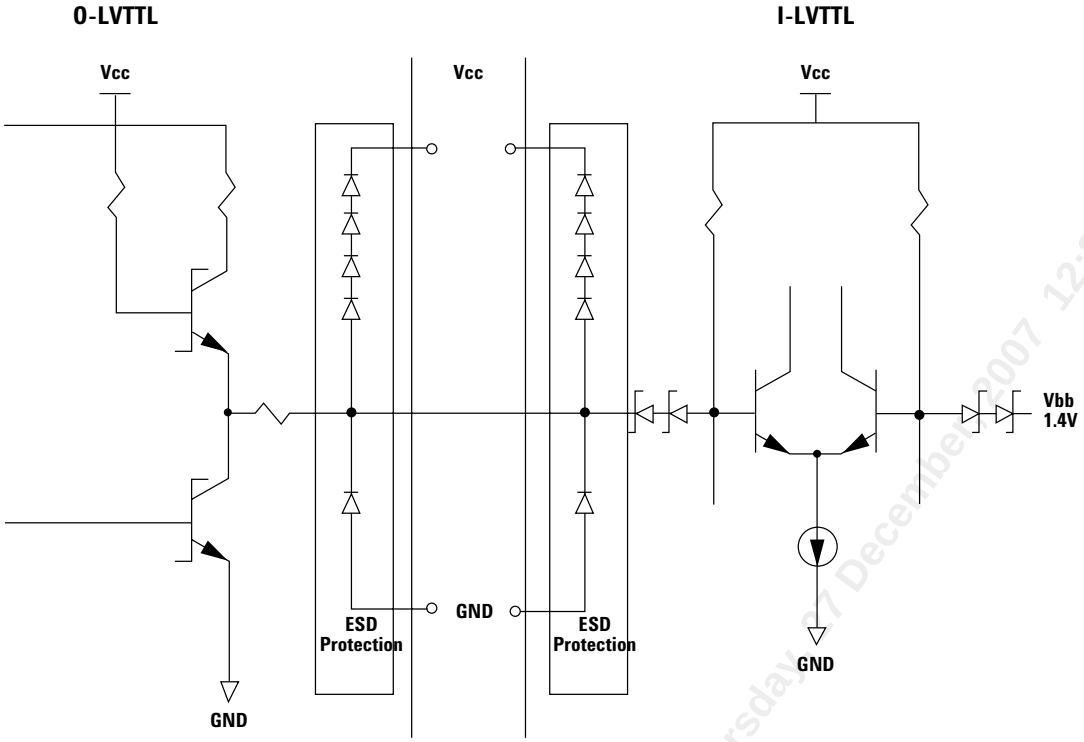

Figure 8. O_LVTTL and I_LVTTL Simplified Circuit Schematic.

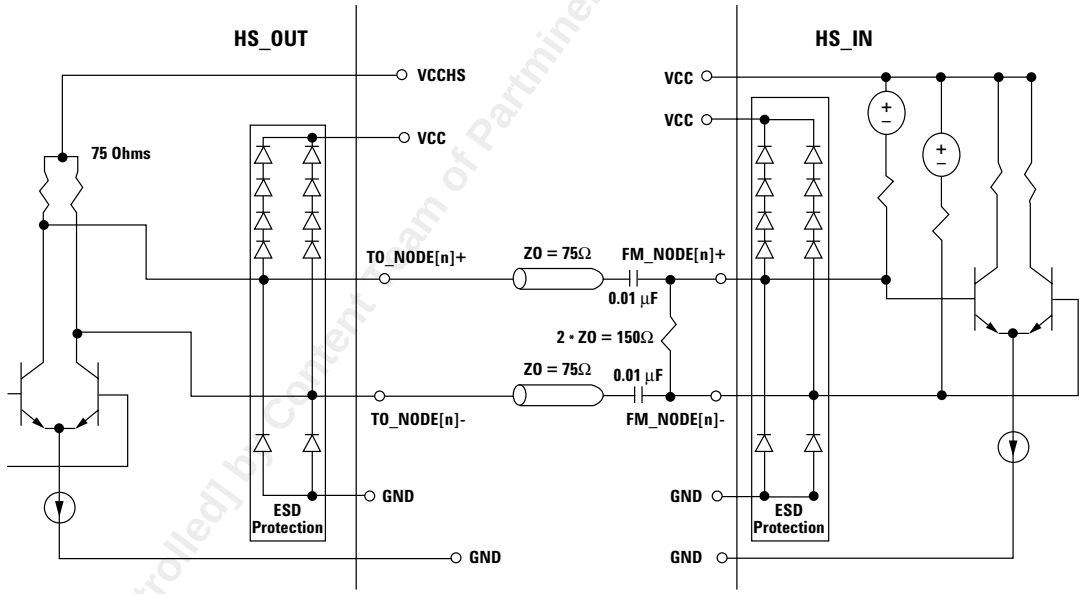

Figure 9. HS_OUT and HS_IN Simplified Circuit Schematic.

Note: FM_NODE[n] inputs should never be connected to ground as permanent damage to the device may result.

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Package Information

HDMP-0482G Thermal Characteristics, T_C = 0°C to 85°C, V_{CC} = 3.15V to 3.45V

Symbol	Parameter	Unit	Typ.	Max.
θ_{jc}	Thermal Resistance, Junction to Case	°C/W	9.5	—

Note: Based on independent testing by Avago. θ_{ja} for these devices is 39.4°C/W for the HDMP-0482G. θ_{ja} is measured on a standard 3x3" FR4 PCB in a still air environment. To determine the actual junction temperature in a given application, use the following equation: $T_j = T_C + (\theta_{jc} \times P_D)$, where T_C is the case temperature measured on the top center of the package, and P_D is the power being dissipated.

Item	Details
Package Material	Plastic
Lead Finish Material	100% Tin (Matte)
Lead Finish Thickness	10 μm min.
Lead Skew	0.20 mm max.
Lead Coplanarity (Seating Plane Method)	0.10 mm max.
Max safe process temperature	260°C, 20s

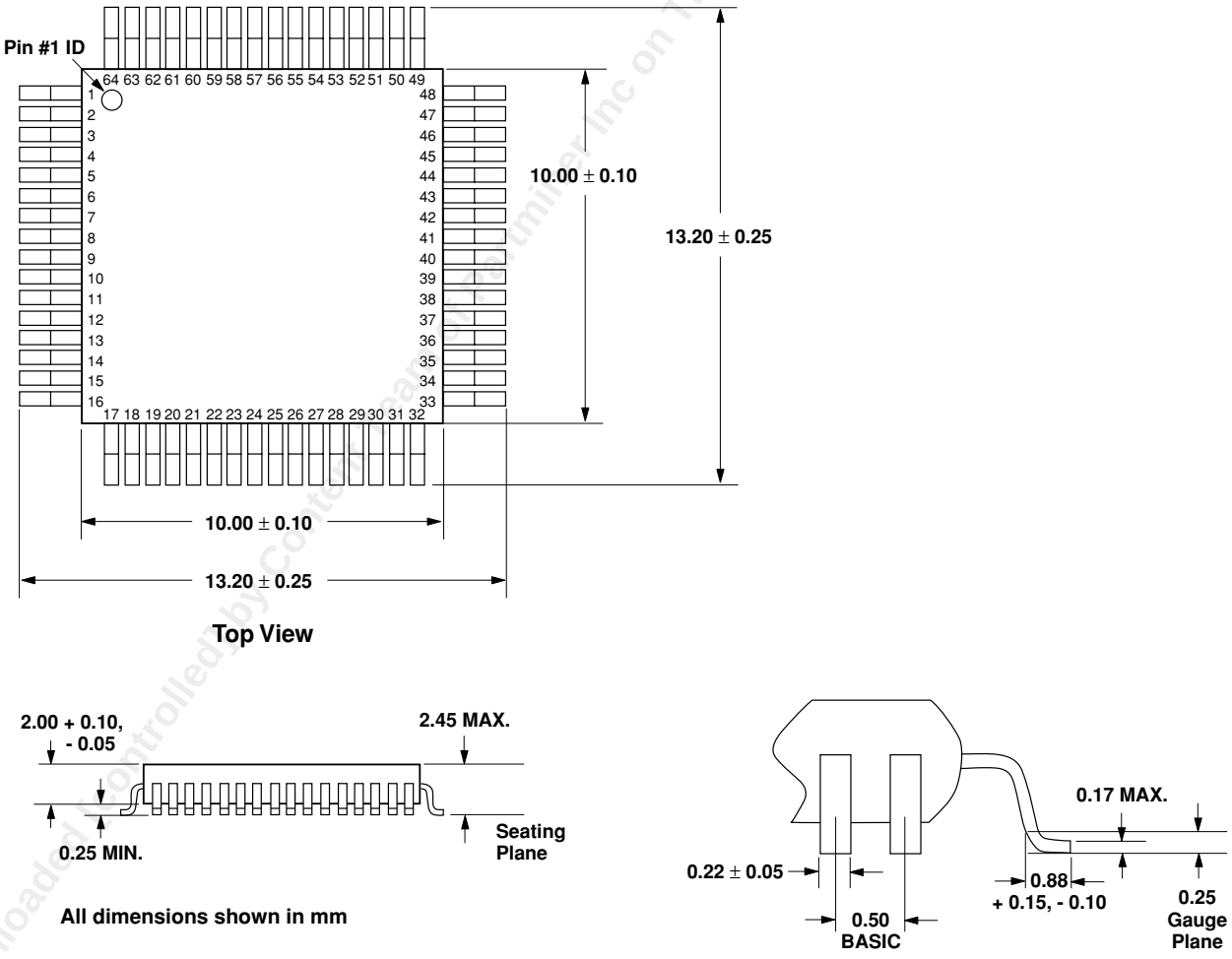

Figure 10. HDMP-0482G Package Drawing.

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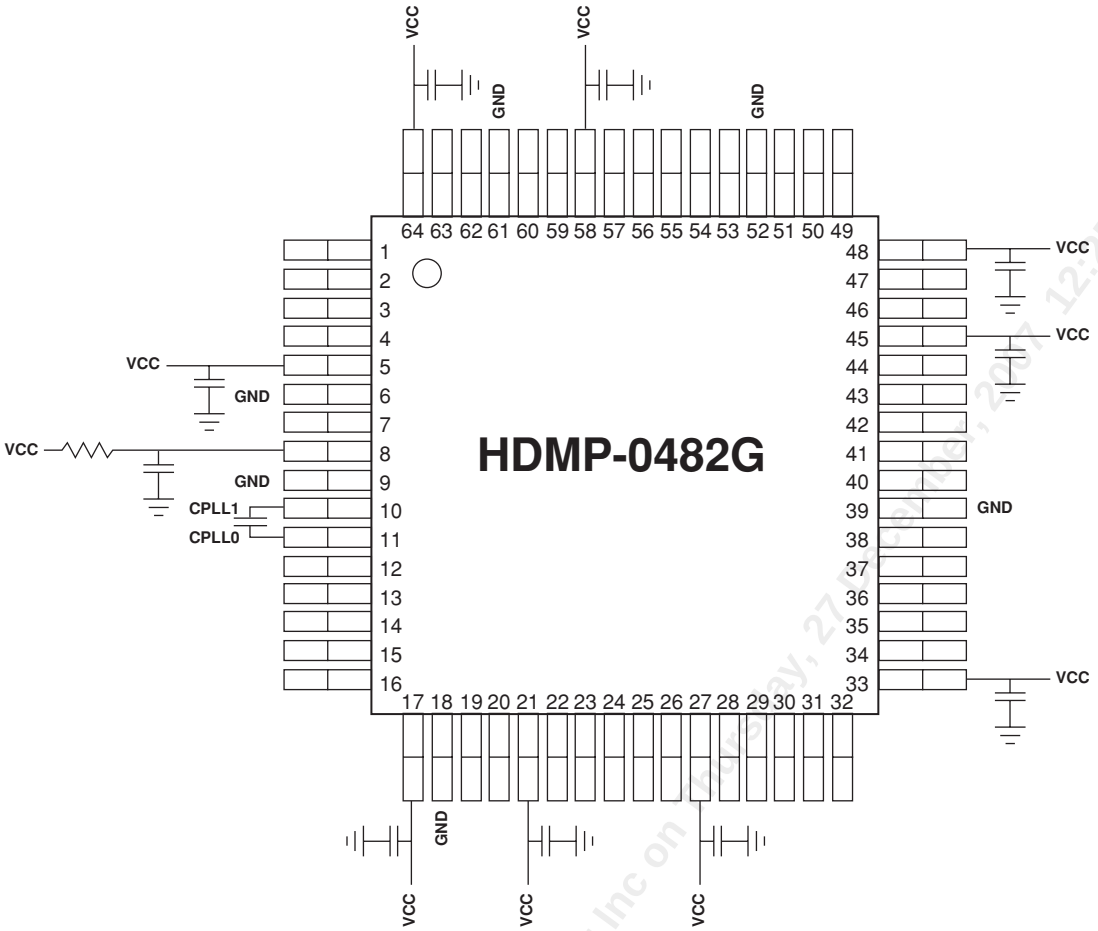

Figure 11. Recommended Power Supply Filtering. Capacitors = 0.1 µF, Resistor = 10Ω.

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