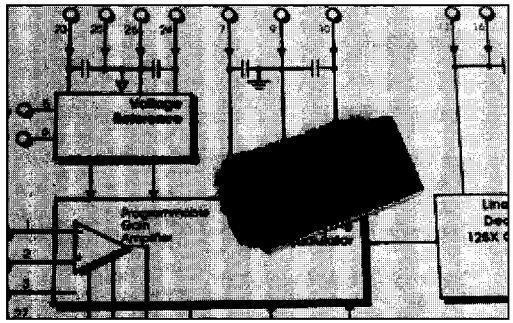
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP4630
20-Bit, 2KSPS Oversampling PGA/ADC

FEATURES

- 20-Bit Resolution at 2K Samples/Second
- 950Hz Signal Bandwidth
- 85dB Linear-phase Anti-alias Protection
- 104dB SNR
- 112dB Dynamic Range
- ±0.6 LSB DNL Error at 20 Bits
- Programmable Gain, Differential Input Amplifier
- ±0.32V, ±0.16V and ±0.08V FSR Inputs
- 200mW Power Dissipation
- Internal Reference
- Internal Decimation Filter



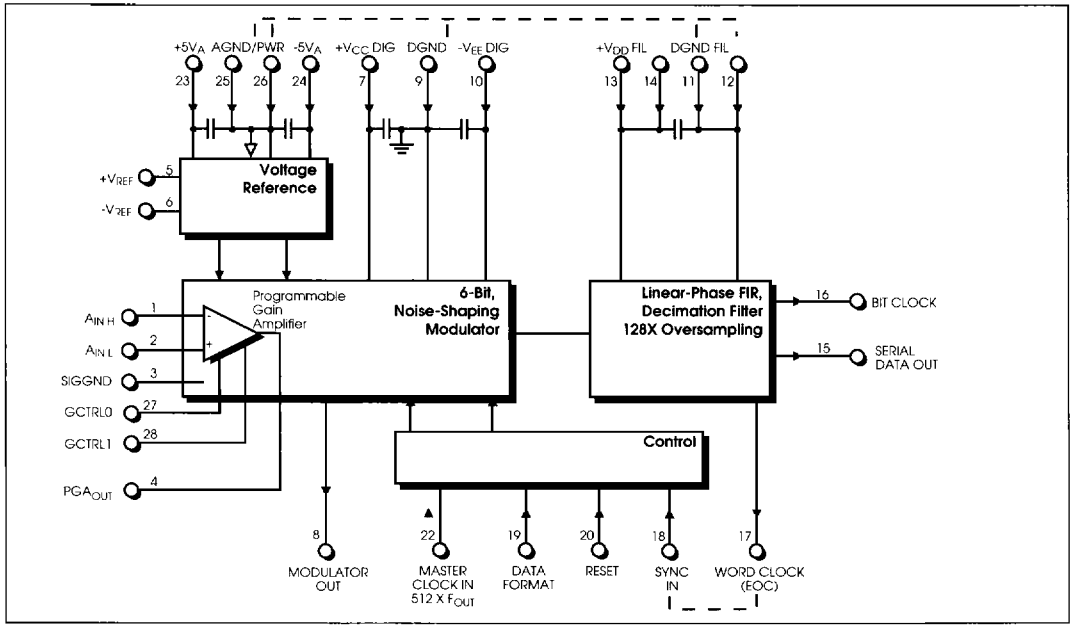
APPLICATIONS

- Geoseismic Data Acquisition
- Electro-optical Instrumentation
- Analytical Instrumentation
- Weighing Systems
- Biomedical Instrumentation

DESCRIPTION

The **SP4630** is a complete, low-power 20-bit oversampling A/D converter optimized for applications requiring wide dynamic range. A differential input, programmable gain (G= 1, 2, 3, 4) instrumentation amplifier allows direct connection to low-level transducer outputs to maximize system signal integrity.

The **SP4630** is very simple to use. Bipolar 5V power supplies, a single 1.024MHz clock



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SPECIFICATIONS

(T_A = 27°C and ±4.75V nominal supply voltages unless otherwise specified)

	MIN.	TYP.	MAX.	UNIT	CONDITIONS
RESOLUTION	20			Bits	Note 1
ANALOG INPUT					
Input Full Scale Range		±320		mV	Gain = 1; Note 1
		±160		mV	Gain = 2
		±106.7		mV	Gain = 3
		±80		mV	Gain = 4
Impedance	1.95	2.0		MΩ	A_{INH} to SIG GND; Note 1
		10,000		KΩ	A_{INH} to A_{INL}; Note 1
Capacitance		5		pF	A_{INH}, A_{INL}; Note 1
Bias Currents		1	10	nA	A_{INH}, A_{INL}; Note 1
Offset Currents		0.1	5	nA	A_{INH}, A_{INL}; Note1
Common Mode Volage	±2.5	+2.6/-2.8		V	A_{INH} = A_{INL} ; Note 1
Common Mode Rejection					Notes 2 & 4, F_{IN} = 70Hz,
Gain = 1	85	90		dB	V_{IN} = 5.00V_{PK-PK};
Gain = 2	90	96		dB	
Gain = 4	95	102		dB	
Offset PSRR					Differential, ±4.5V to ±5.0V
Gain = 1		±1		ppm/V	
Gain = 2		±2		ppm/V	
Gain = 4		±4		ppm/V	
Gain PSRR					Single-ended, ±4.5V to
Gain = 1		+0.032		%	±5.0V
Gain = 2		+0.0005		%	
Gain = 3		-0.029		%	
Gain = 4		-0.038		%	
DC TRANSFER CHARACTERISTICS					
Integral Linearity Error		±0.01		%	From full scale SINAD
Differential Linearity Error		±0.5	±0.75	LSB	Histogram method, Note 3
No Missing Codes	20			bits	Histogram method, Note 1
Gain Error					Single-ended, Notes 2 & 5;
Gain = 1		±0.01	±0.024	%	A_{INH} = signal,
Gain = 2		±0.015	±0..036	%	A_{INL} = SIG GND
Gain = 4		±0.02	±0.048	%	
Offset Error					Single-ended, Notes 2 & 6;
Gain = 1		±10	±20	µV	A_{INH} = signal,
Gain = 2		±40	±50	µV	A_{INL} = SIG GND
Gain = 4		±60	±80	µV	
DYNAMIC CHARACTERISTICS					
Sample Rate	1.8	2.0	2.2	ksps	Notes 1 & 7
Bandwidth		950		Hz	-3dB, F_S = 2ksps; Note 1
Droop	-1.80	-1.86	-1.92	dB	at 800Hz; Note 1
Attenuation			-85	dB	F_{IN} >1.2kHz; Note 1
DC (Idling) Noise					0.5Hz to 1kHz; Note 8
Gain = 1		1.05	1.6	µV rms	referred to input; Note 2
Gain = 2		0.67	1.1	µV rms	referred to input; Note 2
Gain = 4		0.52	0.671	µV rms	referred to input; Note 2

SPECIFICATIONS *(continued)*

(T_A = 27°C and ±4.75V nominal supply voltages unless otherwise specified)

	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DYNAMIC CHARACTERISTICS					
SINAD					Differential
Gain = 1	102	104		dBc	555Hz, 0dBFS; Note 2
	68	78		dBc	70Hz, 0dBFS
		84		dBc	70Hz, -6dBFS
		85		dBc	70Hz, -12dBFS
		85.5		dBc	70Hz, -18dBFS
		81		dBc	70Hz, -24dBFS
		70		dBc	70Hz, -36.1dBFS
		34		dBc	70Hz, -72.2dBFS
		7		dBc	70Hz, -100dBFS
Gain = 2	100	102		dBc	555Hz, 0dBFS
	68	77		dBc	70Hz, 0dBFS
Gain = 4	97	99.5		dBc	555Hz, 0dBFS
	68	76		dBc	70Hz, 0dBFS; Note 2
Spurious-Free Dynamic Range					Differential
Gain = 1	105	115		dBFS	555Hz, 0dBFS; Note 2
	70	80		dBFS	70Hz, 0dBFS
		92		dBFS	70Hz, -6dBFS
		99.5		dBFS	70Hz, -12dBFS
		108		dBFS	70Hz, -18dBFS
		115		dBFS	70Hz, -24dBFS
		127		dBFS	70Hz, -36.1dBFS
		129		dBFS	70Hz, -72.2dBFS
		130		dBFS	70Hz, -100dBFS
Gain = 2	68	77		dBFS	70Hz, 0dBFS
Gain = 4	68	76		dBFS	70Hz, 0dBFS; Note 2
STABILITY					
Offset Temperature Coefficient					Notes 10 & 11
Gain = 1		+0.31		µV/°C	
Gain = 2		+0.42		µV/°C	
Gain = 4		+0.44		µV/°C	
Offset					Notes 2 & 10
Gain = 1		-35/+3	±50	µV	
Gain = 2		-13/+40	±80	µV	
Gain = 4		-0/+60	±100	µV	
Gain Temperature Coefficient					Differential, 2MΩ to signal;
Gain = 1		-60		ppm/°C	Note 2
Gain = 2		-71		ppm/°C	
Gain = 4		-79		ppm/°C	
Gain Error					Differential, 2MΩ to signal;
Gain = 1		-0.25/+0.5	±0.75	%	Note 2
Gain = 2		-0.35/+0.55	±0.85	%	
Gain = 4		-0.4/+0.6	±0.90	%	
DIGITAL INPUT/OUTPUT					
Digital Inputs					V_{CCD} = V_{DDFIL} =4.75V
V_{IL}	0		1.4	V	I_{IL} < 2µA; Note 2
V_{IH}	3.4		+V_{DD}	V	I_{IH} < 2µA; Note 2
I_{IL}		0.5	0.6	mA	RESET (pin 20) input low; 10kΩ pullup
Digital Outputs					V_{DDFIL} = 4.75V
V_{OL}		0.1	0.4	V	I_{OL} = 2.9mA; Note 2
V_{OH}	4.4	4.7		V	I_{OH} = 2.9mA; Note 2

SPECIFICATIONS *(continued)*

(T_A = 27°C and ±4.75V nominal supply voltages unless otherwise specified)

	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DIGITAL INPUT/OUTPUT					
Output Coding	Bit serial, MSB first Offset Binary 2's Complement				DATA FORMAT = "1" DATA FORMAT = "0"
POWER REQUIREMENTS					
Supplies					
$V_{CCA}/V_{CCD}/V_{DDFIL}$	+4.5	+4.75	+5.0	V	Specified; Note 2
V_{CCA}/V_{CCD}	+4.0		+6.0	V	Operating
V_{DDFIL}	+3.0		+6.0	V	Operating
V_{EEA}/V_{EED}	-4.5	-4.75	-5.0	V	Specified; Note 2
V_{EEA}/V_{EED}	-4.0		-6.0	V	Operating
Static Power					Note 12
I_{DDFIL}		20.1		mA	V_{NOM} = 4.75V
$I_{CCA} + I_{CCD}$		10.7		mA	V_{NOM} = 4.75V
$I_{EEA} + I_{EED}$		8.2		mA	V_{NOM} = -4.75V
P_D		185	200	mW	Note 2
		150		mW	V = ±4.5V, 85°C
		244	260	mW	V = ±5.0V, -40°C
Dynamic Power					Note 13
I_{DDFIL}		21.0		mA	V_{NOM} = 4.75V
$I_{CCA} + I_{CCD}$		11.3		mA	V_{NOM} = 4.75V
$I_{EEA} + I_{EED}$		8.9		mA	V_{NOM} = -4.75V
P_D		196		mW	Note 2
		158		mW	V = ±4.5V, 85°C
		258		mW	V = ±5.0V, -40°C
ENVIRONMENTAL					
Centrifuge	5,000			G's	Worst axis; Note 2
Operating Temperature	-40		+85	°C	Note 2
Storage Temperature	-65		+150	°C	Note 1
Power-on Time	65			ms	Notes 1 & 9
MECHANICAL					
Case	28-pin metal				

Notes:

1. Guaranteed by design
2. 100% tested parameter
3. Sample tested parameter
4. Dynamic CMRR is laser-trimmed with 5.00V_{pk-pk}, 70Hz applied. It is tested by applying the same signal and recording peak-to-peak excursion of output codes. Codes are converted to equivalent input voltages, and these are ratioed to applied input level to obtain CMRR in dB.
5. Gain is measured with respect to A_{INH} input at Gain = 1. Offset at A_{INL} may not match offset from A_{INH} when measured on a single-ended DC tester. Maximum offset is measured over temperature on a single-ended DC tester at DC final test by forcing, then measuring the input voltage required to obtain the mid-scale output code.
6. Offset is laser-trimmed with respect to the A_{INH} input at Gain = 1. Offset at the A_{INL} input may not match the offset from A_{INH} when measured on a single-ended DC tester. Maximum offset is measured over temperature on a single-ended DC tester at DC final test by forcing, then measuring the input voltage required to obtain the mid-scale output code.
7. Sample rate is the MASTER CLOCK frequency divided by 512. A 2ksps sampling rate requires a MASTER CLOCK of 1.024MHz. All tests are performed at a 2ksps sampling rate. Bandwidth, droop and attenuation are primarily digital filter parameters, and they will scale with the MASTER CLOCK and sampling rates.
8. DC idling Noise is measured in differential mode (200Ω from A_{INH} to A_{INL}, 100kΩ from each to SIG GND) on the dynamic test system. Differential DC offset is also measured under these same conditions as part of the noise test, and thus includes effects of input offset currents through the external resistors, as well as any thermoelectric potentials between A_{INH} and A_{INL}.
9. SP4630 is not functional until after RESET (pin 20) has been applied. RESET must be held at a logic "0" (low) for 1024 periods of the MASTER CLOCK, minimum. At 2ksps, the MASTER CLOCK = 1.024MHz, and RESET must therefore be held low for 1.0ms. Pipeline delay for valid data is 64ms, thus the Power-on Time is given as 65ms minimum. note that the SP4630 requires approximately one minute to thermally stabilize the offset voltages in the input amplifiers, and that the offset voltages are specified after a minimum of one minute warm-up.
10. Differential, A_{INH} = A_{INL} ; 2MΩ to signal; -40°C to +85°C
11. Refer to graph
12. V_{IN} = GND, V_{CCA}/V_{CCD}, V_{EEA}/V_{EED} strapped
13. V_{IN} = FS sinewave, V_{CCA}/V_{CCD}, V_{EEA}/V_{EED} strapped

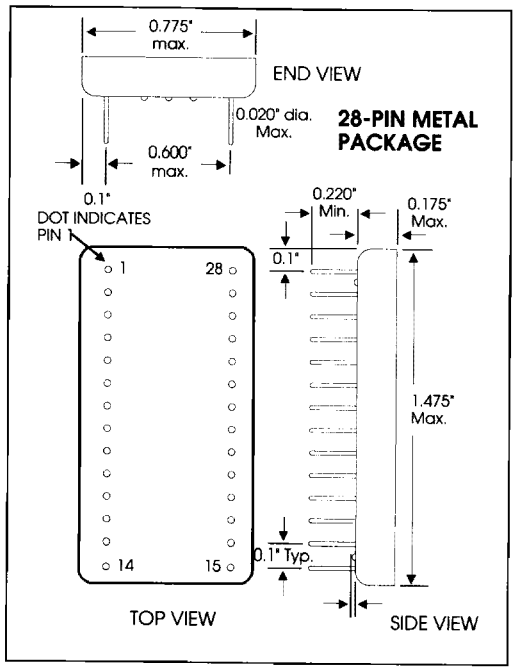
DESCRIPTION(*continued from Page 1*)

and an input signal are all that is required to obtain 20-bit data at a 2KSPS rate. Internal linear-phase anti-alias filtering of 85dB eliminates the need for expensive, pc board real-estate-hungry analog anti-aliasing filters. Output data from the internal decimation filter is a serial bit stream synchronized to a bit clock output.

A proprietary multi-bit oversampling modulator insures freedom from idle pattern problems, and guarantees excellent low-level signal fidelity.

The **SP4630** is available for specified performance over the commercial 0°C to +70°C and industrial -40°C to +85°C temperature ranges. It is packaged in a 28-pin, double-width DIP.

MECHANICAL DIMENSIONS



PIN ASSIGNMENTS

1.	$A_{IN\,H}$	28.	$GCTRL_1$
2.	$A_{IN\,L}$	27.	$GCTRL_0$
3.	SIGGND	26.	AGND/PWR RTN
4.	PGA_{OUT}	25.	AGND/PWR RTN
5.	$+V_{REF\,OUT}$	24.	$-5V_A$
6.	$-V_{REF\,OUT}$	23.	$+5V_A$
7.	$+V_{CC}$ DIG	22.	MASTER CLK IN
8.	MDLTR OUT	21.	NO CONNECTION
9.	DGND	20.	RESET
10.	$-V_{EE}$ DIG	19.	DATA FORMAT
11.	DGND FIL	18.	SYNC IN
12.	DGND FIL	17.	WORD CLK/EOC
13.	$+V_{DD}$ FIL	16.	BIT CLK OUT
14.	$+V_{DD}$ FIL	15.	SERIAL DATA OUT

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Ordering Information	
20-Bit, 2KSPS Oversampling ADC . . .	
SP4630-I	-40°C to +85°C

PINOUT

The functions of the various pins of the **SP4630** are described below. Refer to the Mechanical Dimensions and Pin Assignment information on page 3 of this data sheet.

Pin 1 — A_{INH} — Non-inverting, high impedance, differential analog input.

Pin 2 — A_{INL} — Inverting, high impedance, differential analog input.

Pin 3 — SIGGND — Signal return for the ana-log input.

Pin 4 — PGA_{OUT} — Programmable gain amplifier output. Used for test only.

Pins 5 & 6 — $+V_{REF}$ & $-V_{REF}$ — Internal positive (+1.25V nominal) and negative (-1.245V nom-inal) reference voltages. These should be buffered for use outside the **SP4630**.

Pins 7 — $+V_{CC}$ DIG — Digital +5V power sup-ply input for the front-end modulator portion of the **SP4630**. Internally tied to $+5V_A$.

Pin 8 — MDLTR OUT — Modulator Output. Used for test and trim. Normally left open.

Pin 9 — DGND — Digital ground for the front-end modulator portion of the **SP4630**.

Pins 10 — $-V_{EE}$ DIG — Digital -5V power supply input for the front-end modulator portion of the **SP4630**.

Pins 11 & 12 — DGND FIL — Digital ground for the decimation filter portion of the **SP4630**.

Pins 13 & 14 — $+V_{DD}$ FIL — The +5V digital power supply for the decimation filter portion of the **SP4630**.

Pin 15 — SERIAL DATA OUT — This is the 20-bit digital output data in serial form. The data is presented in a 32-bit field with the MSB first. The data is shifted out at the BIT CLOCK rate of 64kHz. The last 12 bit positions are at logic low.

Pin 16 — BIT CLK OUT — This clock output is used to synchronize the serial data from the SERIAL DATA OUT, pin 15. The serial data changes state on the high-to-low transition of the BIT CLOCK.

Pin 17 — WORD CLOCK/EOC — This pin supplies a clock at the 2kHz sampling rate. This output clock signal should be tied directly to pin 18, SYNC IN if the ADC is not synchronized to another **SP4630**.

Pin 18 — SYNC IN — This input accepts a 2kHz sampling rate clock taken either direct-ly from the **SP4630** WORD CLOCK/ EOC OUTPUT, Pin 17, or from the WORD CLOCK/EOC output from another **SP4630**.

Pin 19 — DATA FORMAT — Selects output data format; logic "0" selects 2's complement, while logic "1" selects offset binary output data format.

Pin 20 — RESET — Active low, accepts a power-on-reset signal from the system. Resets the digital filters to their initial operating state. Must be held low for minimum of 512 cycles of AUXILLIARY CLOCK OUTPUT (2.0ms nominal).

Pin 21 — NO CONNECTION

Pin 22 — MASTER CLOCK IN — Accepts the 1.024MHz nominal master clock timing reference signal.

Pin 23 — $+5V_A$ — Analog power supply voltage input.

Pin 24 — $-5V_A$ — Analog power supply voltage input.

Pins 25 & 26 — AGND/PWR RTN — $\pm 5V_A$ analog power supply return.

Pin 27 — GCTRL0 — Used with pin 28, gain select; CMOS compatible.

Pin 28 — GCTRL1 — Used with pin 27, gain select; CMOS compatible.

USING THE SP4630

Power Supplies

The **SP4630** requires three power supply volt-ages — ±5V analog, ±5V digital for the modulator, and +5V digital for the decimation filter. The +5V supply connected to pins 13 and 14 may be the same one used to supply +5V power to pin 7, although for best noise performance, the two +5V digital supplies should be separate. The +5V supplied to pin 7 must be derived from the $+5V_A$ supplied at pin 23. This can be achiev-

ed by isolating pin 7 from 23 by a 10ohm resistor or ferrite beads.

Grounding

Analog and digital grounds are not internally tied together in the **SP4630**. These should be tied to a ground plane. SIGGND (pin 3) should be tied to externally to the AGND pin connected to power return.

Digital I/O

Normally, the WORD CLOCK OUT (pin 17) is tied to the SYNC INPUT (pin18). To allow synchronizing multiple **SP4630**s, the WORD CLOCK OUT (pin 17) of a "master" **SP4630** is connected to the SYNC INPUT (pin 18) of any other **SP4630**s that are to be synchronized with it. The RESET pin (20) of all units should be tied together.

Output Format Options

The DATA FORMAT pin (19) is used to determine the format of the serial output data. A logic low ("0") sets the output data to a 2's complement format, while a logic high ("1") set the output data to offset binary.

Serial output data is presented on the SERIAL DATA OUT pin (15), synchronized with the BIT CLOCK output on pin 16. The data is output as a 32-bit field, MSB first, with the last 12 bits at logic "0". The data changes state on the high-to-low transition of the BIT CLOCK signal. The bit rate in kHz is determined by multiplying the 32 bit field by the sampling rate clock. Thus, for a 2kHz data sampling rate, the bit clock is 32x2kHz, or 64kHz. *Figure 1, "Serial Data Output Timing"* shows the timing relationship for serial data output from the **SP4630**.

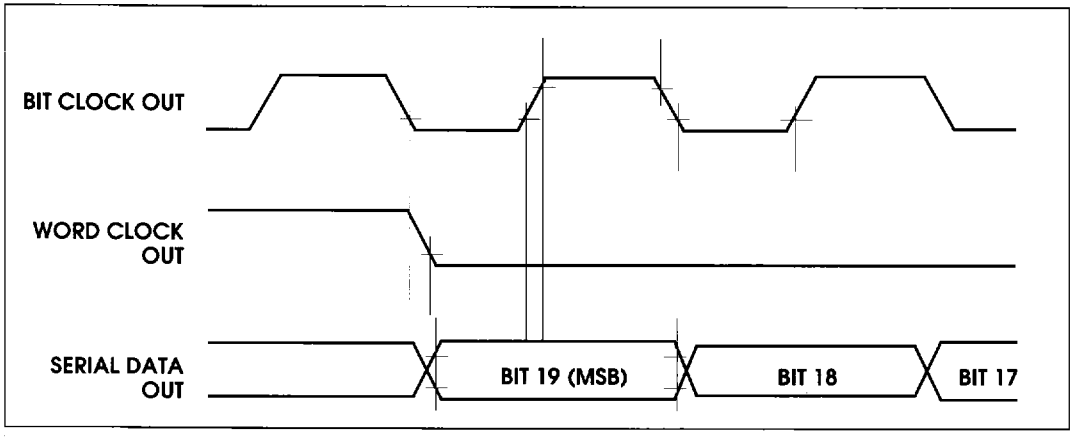

Figure 1. Serial Data Output Timing

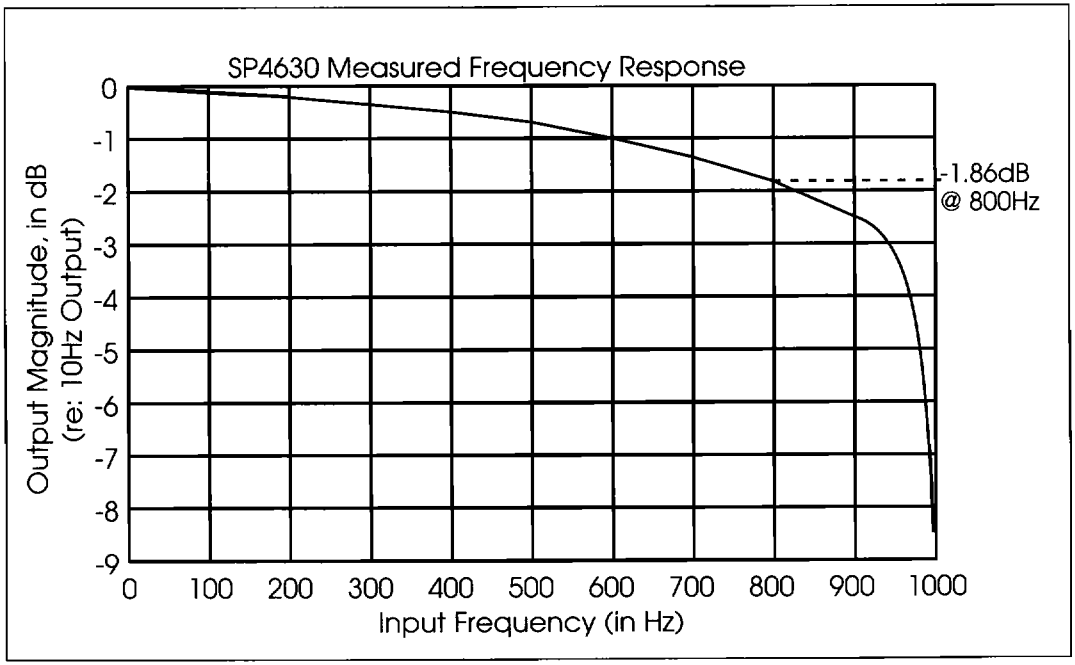

Figure 2. SP4630 Frequency Response

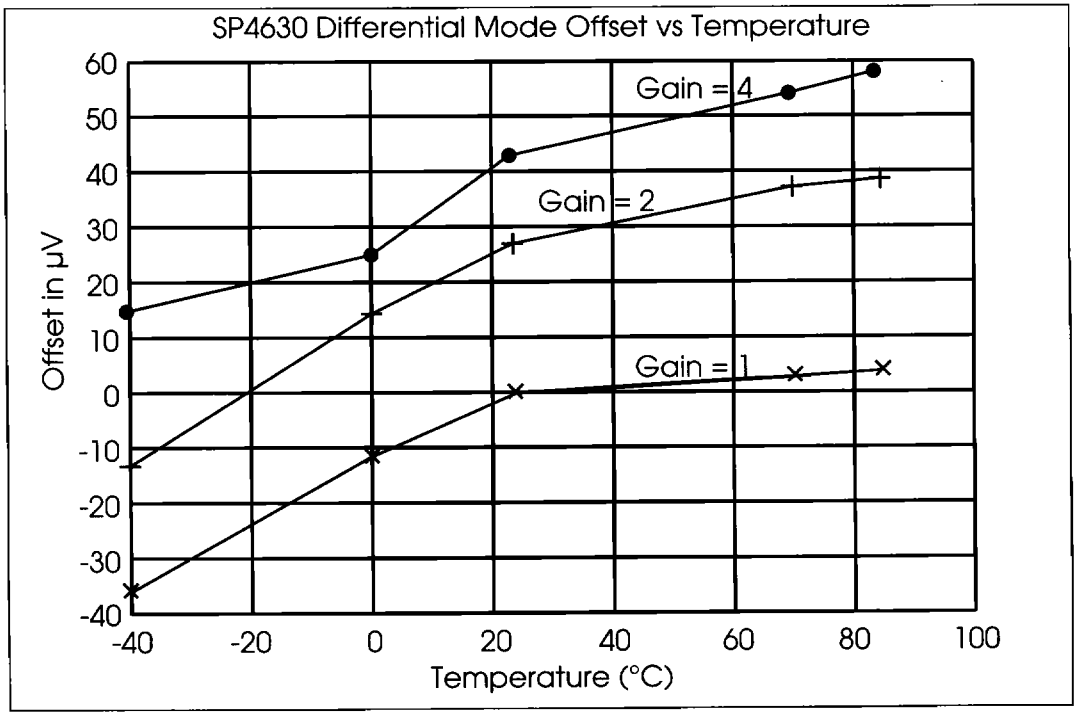

Figure 3. Offset Voltage Temperature Coefficient

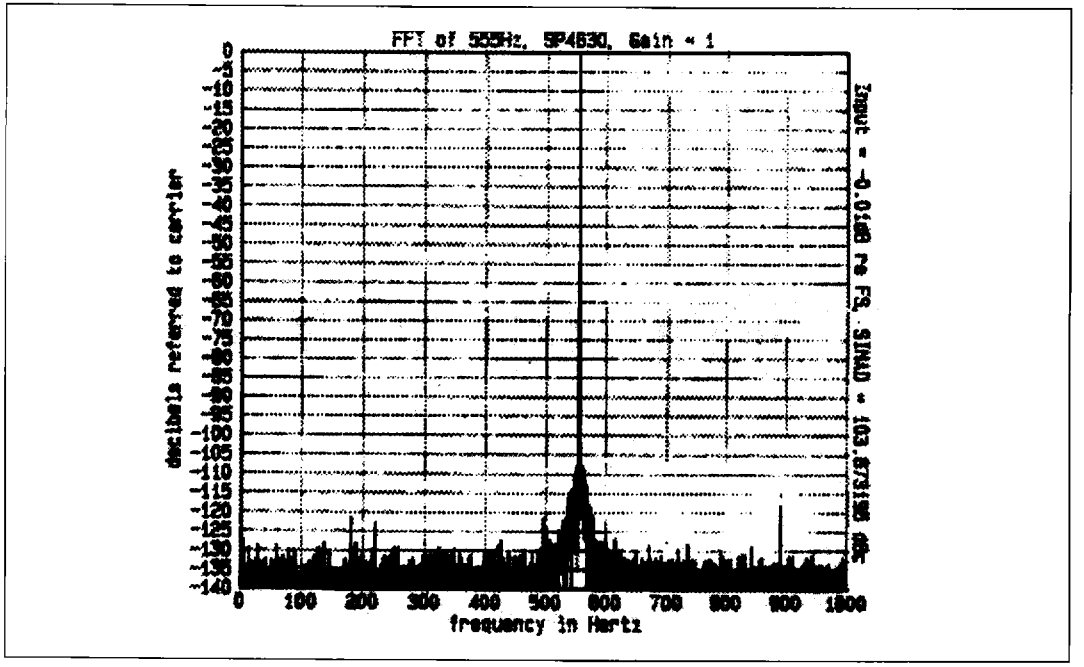

Figure 4. FFT; F_{IN} = 555Hz @ -0.1dB ; Gain = 1

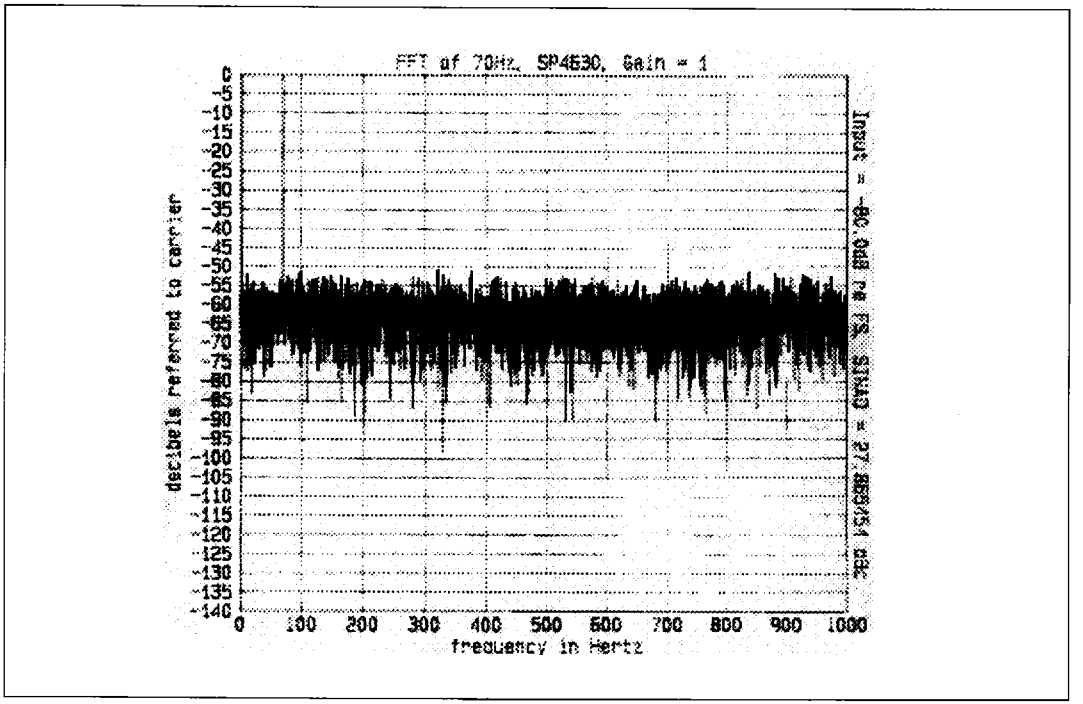

Figure 5. FFT; F_{IN} = 70Hz @ -80.0dB ; Gain = 1

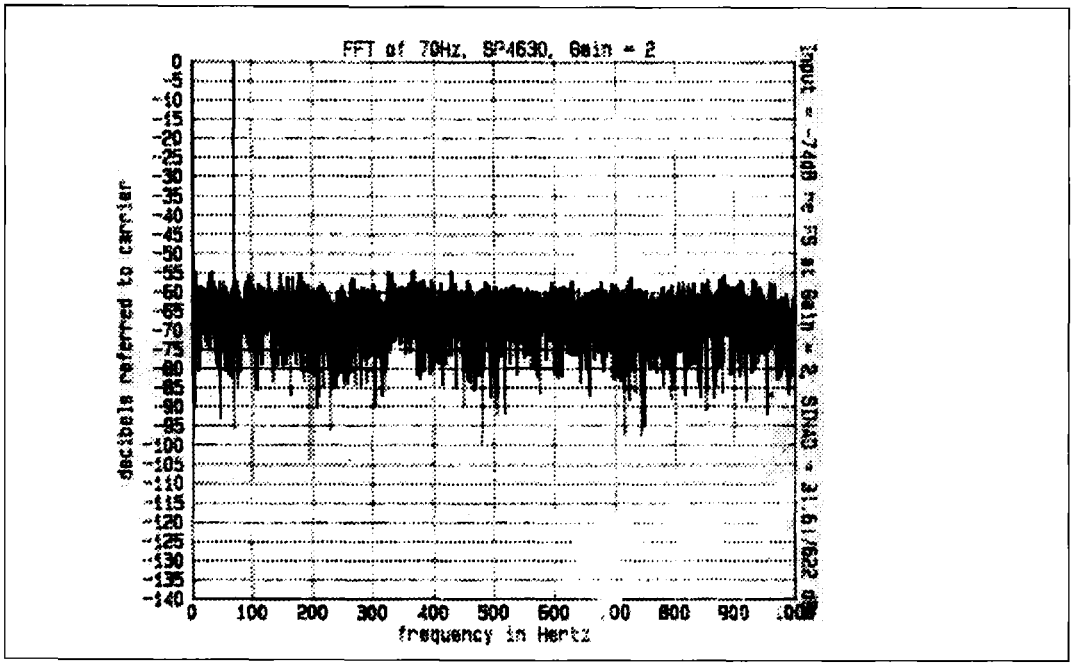

Figure 6. FFT; F_{IN} = 70Hz @ -74.0dB ; Gain = 2

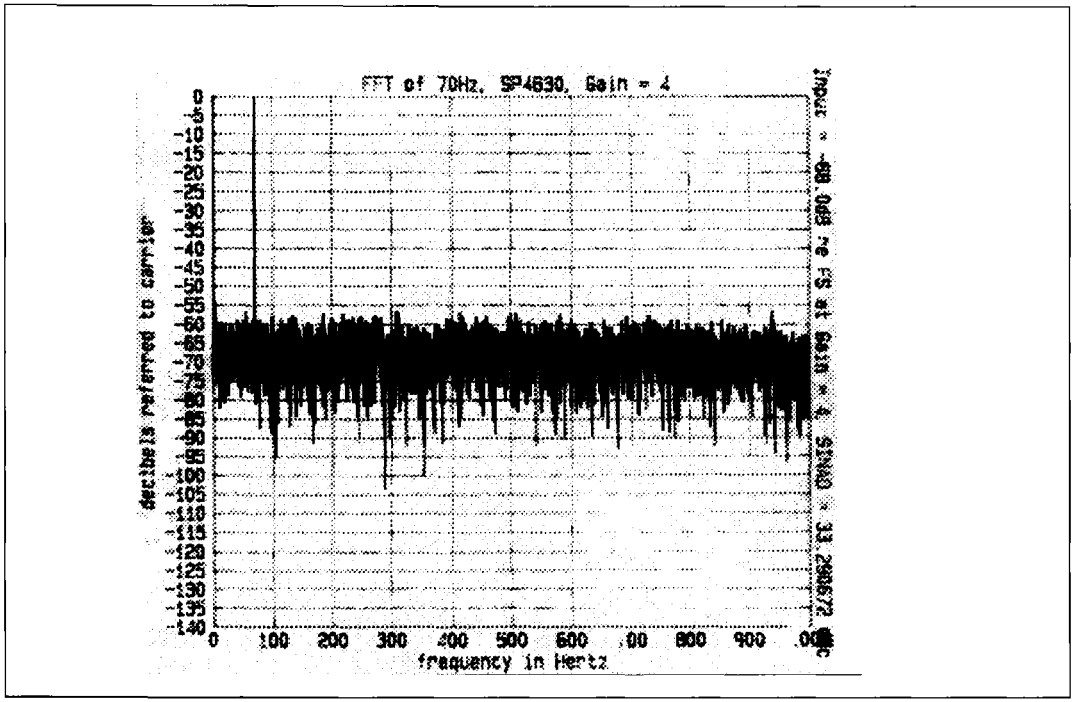

Figure 7. FFT; F_{IN} = 70Hz @ -68.0dB ; Gain = 4