August 1992
Edition 1.0A

FUJITSU

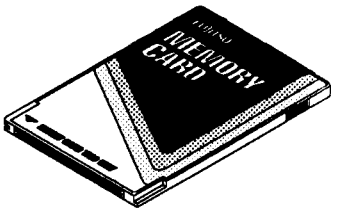
DATA SHEET

MB98A5101x-, 5111x-, 5121x-, 5131x-, and 5141x-25 Mask ROM Memory Card IM-, 2M-, 4M-, 8M-, and 16M-BYTE

The Fujitsu MB98A5101x, MB98A5111x, MB98A5121x, MB98A5131x and MB98A5141x are Mask Programmable Read Only Memory (Mask ROM) cards capable of storing and retrieving large amounts of data. The memory circuits are housed in a credit-card sized 68-pin package. Internal circuitry is protected by two metal panels, one at the top and the bottom of the card, that help to reduce chip damage from electrostatic discharge.

A unique feature of the Fujitsu memory cards allows the user to organize the card as either an 8-bit or a 16-bit bus configuration. All cards are portable and operate on low power at high speed.

In accordance with the Personal Computer Memory Card International Association (PCMCIA) and Japan Electrical Industry Development Association (JEIDA) industry standard specification, Mask ROM cards offer additional EEPROM memory that is used to store attribute data. The attribute memory is a Mask ROM card option. (See pages 2 and 3 for a description of the three available options.)



68 pin Memory Card
(CRD-68P-M02)

- PCMCIA and JEIDA industry standard for 68-pin memory card
- Credit card size dimensions: 85.6mm (length) x 54.0mm (width) x 3.3mm (thick)
- PCMCIA / JEIDA industry standard, two–piece 68-pin connector (with a two-row built-in 68-pin receptacle)
- An additional EEPROM memory for storing attribute data (optional feature)
- Complete static operation: No clock required
- TTL compatible inputs/outputs

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to V_{CC} +0.5	V
Output Voltage	$V_{I/O}$	–0.5 to V_{CC} +0.5	V
Temperature Under Bias	T_{BIAS}	–10 to +60	°C
Storage Temperature	T_{STG}	–30 to +70	°C

— Note —

Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ATTRIBUTE MEMORY OPTIONS

PCMCIA and JEIDA standard memory cards from Fujitsu provide a separate EEPROM memory address space for recording fundamental card information. It is used by card manufacturers to record basic configuration information such as device type, size, speed, etc.

The attribute memory is selected by asserting the $\overline{REG}$ pin on the card interface. Option descriptions as follows:

OPTION 1: Attribute memory is not supported. $\overline{REG}$ Pin : Not Connected

Part Number	Main Memory		Attribute Memory		Memory Organizaiton *
	Memory Device	Access Time	Memory Device	Access Time	
MB98A51011	MB838200 x 1 pc	250 ns	N / A	N / A	1 M x 8 bits/512K x 16 bits
MB98A51111	MB838200 x 2 pcs	250 ns	N / A	N / A	2 M x 8 bits/ 1 M x 16 bits
MB98A51211	MB838200 x 4 pcs	250 ns	N / A	N / A	4 M x 8 bits/ 2 M x 16 bits
MB98A51311	MB838200 x 8 pcs	250 ns	N / A	N / A	8 M x 8 bits/ 4 M x 16 bits
MB98A51411	MB838200 x 16 pcs	250 ns	N / A	N / A	16 M x 8 bits/ 8 M x 16 bits

OPTION 2: Attribute memory in a separate location is not supported.

When the $\overline{REG}$ line is asserted, "FF" is output to the data bus to indicate that attribute data may be stored in main memory.

Part Number	Main Memory		Attribute Memory		Memory Organizaiton *
	Memory Device	Access Time	Memory Device	Access Time	
MB98A51012	MB838200 x 1 pc	250 ns	N / A	N / A	1 M x 8 bits/512K x 16 bits
MB98A51112	MB838200 x 2 pcs	250 ns	N / A	N / A	2 M x 8 bits/ 1 M x 16 bits
MB98A51212	MB838200 x 4 pcs	250 ns	N / A	N / A	4 M x 8 bits/ 2 M x 16 bits
MB98A51312	MB838200 x 8 pcs	250 ns	N / A	N / A	8 M x 8 bits/ 4 M x 16 bits
MB98A51412	MB838200 x 16 pcs	250 ns	N / A	N / A	16 M x 8 bits/ 8 M x 16 bits

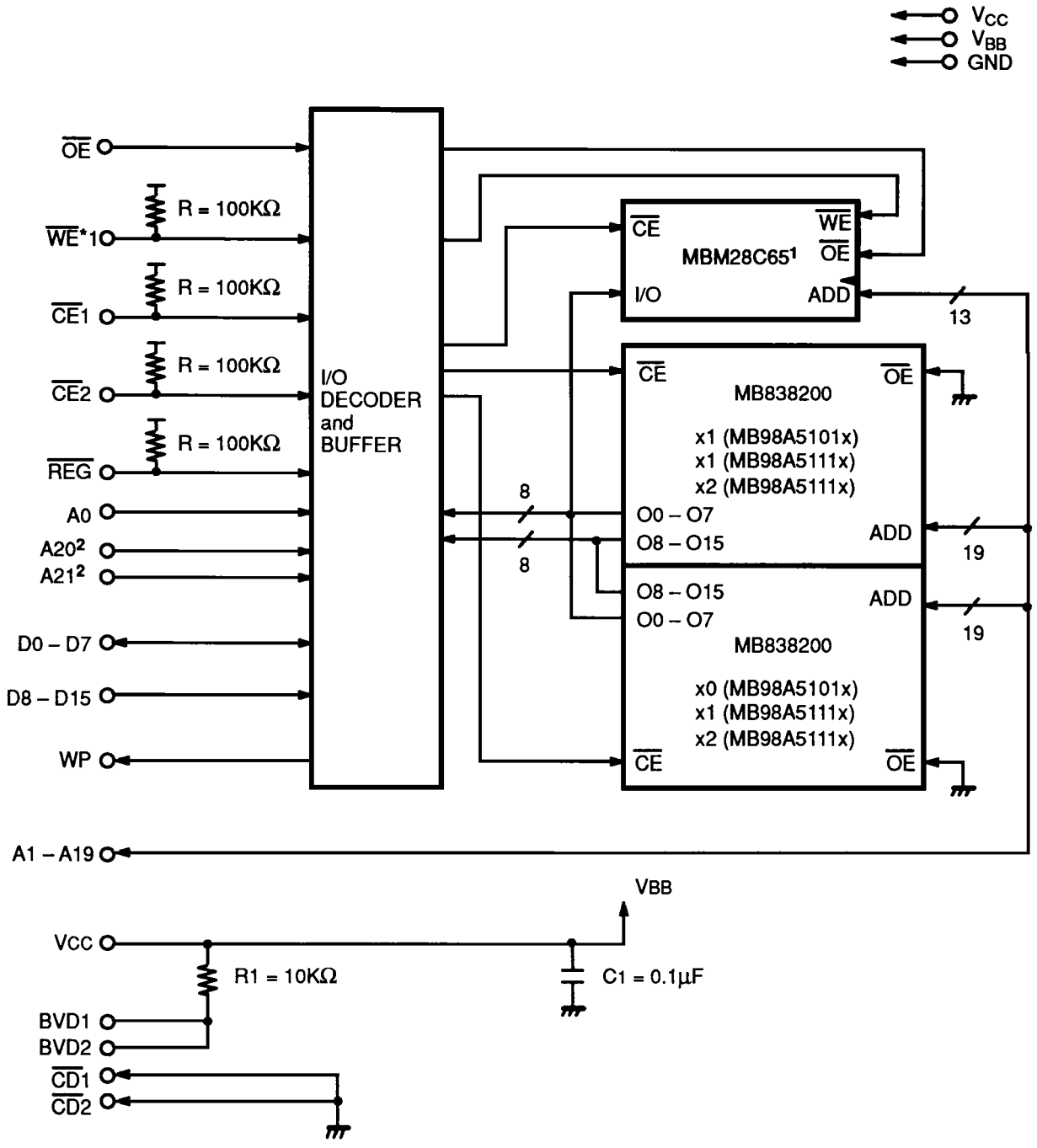
OPTION 3: Attribute memory is supported. The data is stored in an 8K-bit EEPROM.

When the $\overline{REG}$ line is asserted, data stored in EEPROM is output to the data bus.

Part Number	Main Memory		Attribute Memory		Memory Organizaiton *
	Memory Device	Access Time	Memory Device	Access Time	
MB98A51013	MB838200 x 1 pc	250 ns	MBM28C65 x 1 pc	300 ns	1 M x 8 bits/512K x 16 bits
MB98A51113	MB838200 x 2 pcs	250 ns	MBM28C65 x 1 pc	300 ns	2 M x 8 bits/ 1 M x 16 bits
MB98A51213	MB838200 x 4 pcs	250 ns	MBM28C65 x 1 pc	300 ns	4 M x 8 bits/ 2 M x 16 bits
MB98A51313	MB838200 x 8 pcs	250 ns	MBM28C65 x 1 pc	300 ns	8 M x 8 bits/ 4 M x 16 bits
MB98A51413	MB838200 x 16 pcs	250 ns	MBM28C65 x 1 pc	300 ns	16 M x 8 bits/ 8 M x 16 bits

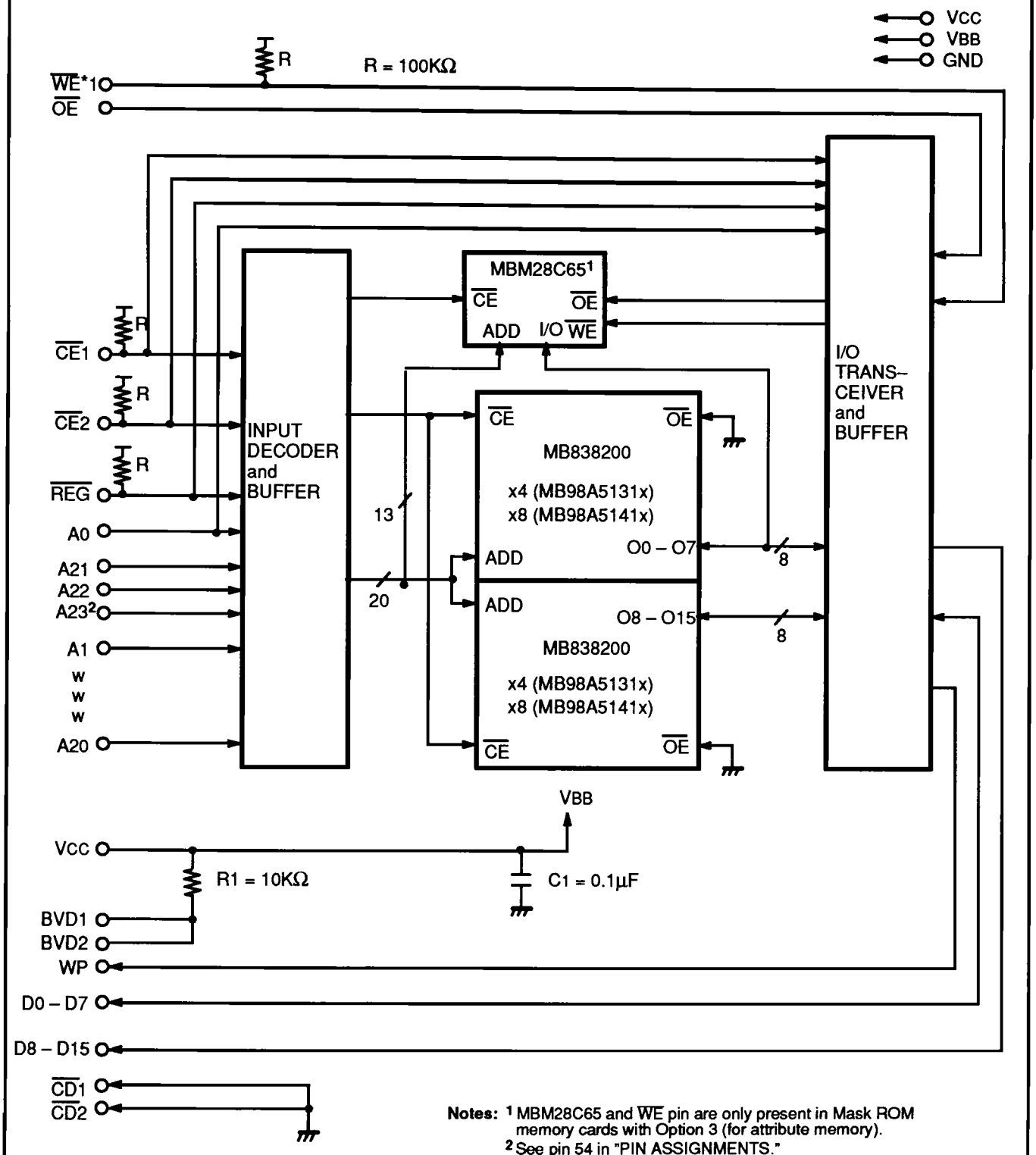
Note: * To be configured by user.

Figure 1. MB98A5101x, 5111x, and 5121x BLOCK DIAGRAM



Notes: [1] MBM28C65 and WE pin are only present in Mask ROM memory cards with Option 3 (for attribute memory).
[2] See pins 49 and 50 in "PIN ASSIGNMENTS."

Figure 2. MB98A5131x and 5141x BLOCK DIAGRAM



Notes: [1] MBM28C65 and $\overline{WE}$ pin are only present in Mask ROM memory cards with Option 3 (for attribute memory).
[2] See pin 54 in "PIN ASSIGNMENTS."

PIN ASSIGNMENTS

MB98A5101x	MB98A5111x	MB98A5121x	Pin No.		MB98A5101x	MB98A5111x	MB98A5121x
GND	GND	GND	1	35	GND	GND	GND
D3	D3	D3	2	36	$\overline{CD1}$	$\overline{CD1}$	$\overline{CD1}$
D4	D4	D4	3	37	D11	D11	D11
D5	D5	D5	4	38	D12	D12	D12
D6	D6	D6	5	39	D13	D13	D13
D7	D7	D7	6	40	D14	D14	D14
$\overline{CE1}$	$\overline{CE1}$	$\overline{CE1}$	7	41	D15	D15	D15
A10	A10	A10	8	42	$\overline{CE2}$	$\overline{CE2}$	$\overline{CE2}$
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	9	43	NC	NC	NC
A11	A11	A11	10	44	NC	NC	NC
A9	A9	A9	11	45	NC	NC	NC
A8	A8	A8	12	46	A17	A17	A17
A13	A13	A13	13	47	A18	A18	A18
A14	A14	A14	14	48	A19	A19	A19
$\overline{WE}$ (NC)	$\overline{WE}$ (NC)	$\overline{WE}$ (NC)	15	49	NC	A20	A20
NC	NC	NC	16	50	NC	NC	A21
Vcc	Vcc	Vcc	17	51	Vcc	Vcc	Vcc
NC	NC	NC	18	52	NC	NC	NC
A16	A16	A16	19	53	NC	NC	NC
A15	A15	A15	20	54	NC	NC	NC
A12	A12	A12	21	55	NC	NC	NC
A7	A7	A7	22	56	NC	NC	NC
A6	A6	A6	23	57	NC	NC	NC
A5	A5	A5	24	58	NC	NC	NC
A4	A4	A4	25	59	NC	NC	NC
A3	A3	A3	26	60	NC	NC	NC
A2	A2	A2	27	61	$\overline{REG}$	$\overline{REG}$	$\overline{REG}$
A1	A1	A1	28	62	BVD2	BVD2	BVD2
A0	A0	A0	29	63	BVD1	BVD1	BVD1
D0	D0	D0	30	64	D8	D8	D8
D1	D1	D1	31	65	D9	D9	D9
D2	D2	D2	32	66	D10	D10	D10
WP	WP	WP	33	67	$\overline{CD2}$	$\overline{CD2}$	$\overline{CD2}$
GND	GND	GND	34	68	GND	GND	GND

PIN ASSIGNMENTS (Continued)

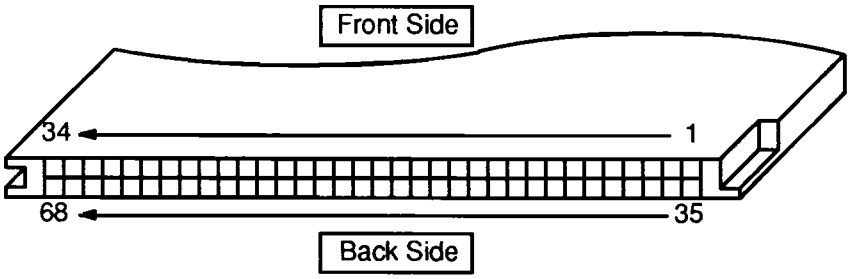
MB98A5131x	MB98A5141x	Pin No.		MB98A5131x	MB98A5141x
GND	GND	1	35	GND	GND
D3	D3	2	36	$\overline{CD1}$	$\overline{CD1}$
D4	D4	3	37	D11	D11
D5	D5	4	38	D12	D12
D6	D6	5	39	D13	D13
D7	D7	6	40	D14	D14
$\overline{CE1}$	$\overline{CE1}$	7	41	D15	D15
A10	A10	8	42	$\overline{CE2}$	$\overline{CE2}$
$\overline{OE}$	$\overline{OE}$	9	43	NC	NC
A11	A11	10	44	NC	NC
A9	A9	11	45	NC	NC
A8	A8	12	46	A17	A17
A13	A13	13	47	A18	A18
A14	A14	14	48	A19	A19
$\overline{WE}$ (NC)	$\overline{WE}$ (NC)	15	49	A20	A20
NC	NC	16	50	A21	A21
VCC	VCC	17	51	VCC	VCC
NC	NC	18	52	NC	NC
A16	A16	19	53	A22	A22
A15	A15	20	54	NC	A23
A12	A12	21	55	NC	NC
A7	A7	22	56	NC	NC
A6	A6	23	57	NC	NC
A5	A5	24	58	NC	NC
A4	A4	25	59	NC	NC
A3	A3	26	60	NC	NC
A2	A2	27	61	$\overline{REG}$	$\overline{REG}$
A1	A1	28	62	BVD2	BVD2
A0	A0	29	63	BVD1	BVD1
D0	D0	30	64	D8	D8
D1	D1	31	65	D9	D9
D2	D2	32	66	D10	D10
WP	WP	33	67	$\overline{CD2}$	$\overline{CD2}$
GND	GND	34	68	GND	GND

PIN DESCRIPTIONS

Symbol	Pin Name	Input / Output	Function
A0 to A23	Address Input	Input	Address Inputs, A0–A23
D0 to D15	Data Input/Output	Input / Output	Data Inputs and Outputs. The data bus size (8-bit or 16-bit) is selected with CE1 and CE2.
$\overline{CE1}$	Card Enable for Lower Byte	Input	Active Low. –Lower byte (D0–D7) is selected for read/write function of Mask ROM cards.
$\overline{CE2}$	Card Enable for Upper Byte	Input	Active Low. –Upper byte (D8–D15) is selected for read/write function of Mask ROM cards.
$\overline{REG}$	Attribute Memory Select	Input	Active Low. –Attribute memory is selected for the read / write function of the identification data of the Mask ROM cards. (NC or "FF" data or attribute data.)
$\overline{OE}$	Output Enable	Input	Active Low. –Output enable for Mask ROM cards.
$\overline{WE}$	Write Enable	Input	Active Low. –Write enable for an attribute memory.
$\overline{CD1}$, $\overline{CD2}$	Card Detect	Output	These pins detect if the card has been correctly inserted. Both pins are tied to GND internally.
WP	Write Protect	Output	This pin outputs high level for Mask ROM cards and low level for an attribute memory.
BVD1, BVD2	Battery Voltage Detect	Output	Both pins are tied to V_{CC} internally.
V_{CC}	Power Supply	–	Power Supply Voltage (+5.0V ±5%)
GND	Ground	–	System Ground
NC	No Connection	–	

PIN LOCATIONS

Figure 3. BOTTOM VIEW (Connector Side)



FUNCTION TRUTH TABLE

MAIN MEMORY FUNCTION[1] ($\overline{REG}$=VIH)

$\overline{CE2}$	$\overline{CE1}$	A0 (Byte)	$\overline{OE}$	$\overline{WE}$	Mode	Data Input / Output	
						D15–D8	D7–D0
H	H	X	X	H[2]	Standby	High–Z	
H	L	L	L	H[2]	Read (x8)	High–Z	D_{OUT} (Lower Byte)
H	L	H	L	H[2]	Read (x8)	High–Z	D_{OUT} (Upper Byte)
L	H	X	L	H[2]	Read (x8)	D_{OUT} (Upper Byte)	High–Z
L	L	X	L	H[2]	Read (x16)	DOUT	
X	X	X	H	H[2]	Output Disable	High–Z	

ATTRIBUTE MEMORY FUNCTION[1] ($\overline{REG}$=VIL)[3]

$\overline{CE2}$	$\overline{CE1}$	A0 (Byte)	$\overline{OE}$	$\overline{WE}$	Mode	Data Input / Output	
						D15–D8	D7–D0
H	H	X	X	X	Standby	High–Z	
H	L	L	L	H	Read (x8)	High–Z	D_{OUT}[4] (Lower Byte)
H	L	H	L	H	Read (x8)	High–Z	H
H	L	L	H	L	Write (x8)	High–Z	D_{IN} (Lower Byte)
H	L	H	H	L	Write (x8)	High–Z	X
L	H	X	L	H	Read (x8)	H	High–Z
L	H	X	H	L	Write (x8)	X	High–Z
L	L	X	L	H	Read (x16)	H	D_{OUT}[4] (Lower Byte)
L	L	X	H	L	Write (x16)	X	D_{IN} (Lower Byte)
X	X	X	H	H	Output Disable	High–Z	

Notes: [1] H = VIH, L = VIL, X = Either VIL or VIH
[2] X is available for MB98A51011, MB98A51012, MB98A51111, MB98A51112, MB98A51211, MB98A51212, MB98A51311, MB98A51312, MB98A51411, and MB98A51412.
[3] NC for MB98A51011, MB98A51111, MB98A51211, MB98A51311, and MB98A51411.
[4] H-level is output for MB98A51012, MB98A51112, MB98A51212, MB98A51312, and MB98A51412.

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Ground	GND		0		V
Input High Voltage	V_{IH}	2.4		V_{CC}+0.3	V
Input Low Voltage	V_{IL}	–0.3		0.8	V
Ambient Temperaure	T_A	0		55	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Standby Supply Current	$\overline{CE1}$, $\overline{CE2} \geq V_{CC}$ –0.2V	I_{SB1}			100	µA
	$\overline{CE1}$, $\overline{CE2} = V_{IH}$	I_{SB2}			10	mA
Active Supply Current	$V_{IN} = V_{IH}$ or V_{IL} $\overline{CE1}$, $\overline{CE2} = V_{IL}$, I_{OUT} = 0mA	I_{CC1}			100	mA
Operating Supply Current	$V_{IN} = V_{IH}$ or V_{IL}, Cycle = Min. Duty = 100%, I_{OUT} = 0mA	I_{CC2}			120	mA
Input Leakage Current[1]	V_{IN} = 0V to V_{CC}	I_{LI}	–10		10	µA
Output Leakage Current[2]	V_{OUT} = 0V to V_{CC}, $\overline{CE1}$, $\overline{CE2}$=V_{IH} or $\overline{OE} = V_{IH}$	ILI/O	–10		10	µA
Output High Voltage[3]	I_{OH} = –1.0mA	V_{OH}	2.4			V
Output Low Voltage[4]	I_{OL} = 2.1mA	V_{OL}			0.4	V

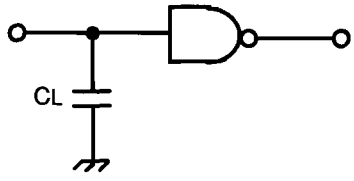
Notes: [1] This value does not apply to $\overline{CE1}$, $\overline{CE2}$, $\overline{REG}$ and $\overline{WE}$.
[2] This value does not apply to BVD1, BVD2, $\overline{CD1}$, $\overline{CD2}$ and WP.
[3] This value does not apply to BVD1 and BVD2.
[4] This value does not apply to $\overline{CD1}$ and $\overline{CD2}$.

CAPACITANCE (T_A=25°C, f=1MHz, V_{IN}=$V_{I/O}$=GND)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance[1]	C_{IN}			50	pF
I/O Capacitance[2]	C_{OUT}			50	pF

Notes: [1] This value does not apply to $\overline{CE1}$, $\overline{CE2}$, $\overline{REG}$ and $\overline{WE}$.
[2] This value does not apply to BVD1, BVD2, $\overline{CD1}$, $\overline{CD2}$ and WP.

Figure 4. AC TEST CONDITIONS



- Input Pulse Levels: 0.6V to 2.6V
- Input Pulse Rise and Fall Times: 5ns (Transition between 0.8V and 2.4V)
- Timing Reference Levels
  Input: V_{IL} = 0.8V, V_{IH} = 2.4V
  Output: V_{OL} = 0.8V, V_{OH} = 2.0V
- Output Load: 1TTL gate + CL (100pF)

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY READ CYCLE

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	t_{RC}	250		ns
Address Access Time	t_{AA}		250	ns
Card Enable Access Time	t_{CE}		250	ns
Output Enable Access Time	t_{OE}		120	ns
Output Disable Time[1]	t_{DF}		100	ns
Output Hold Time	t_{OH}	0		ns

Note: [1] t_{DF} is specified from the rising edge of $\overline{OE}$, $\overline{CE1}$ and $\overline{CE2}$, whichever occurs first. t_{DF} is defined as the point where data is no longer driven.

ATTRIBUTE MEMORY READ CYCLE[2]

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	t_{RRC}	300		ns
Address Access Time	t_{RAA}		300	ns
Card Enable Access Time	t_{RCE}		300	ns
Output Enable Access Time	t_{ROE}		150	ns
Output Disable Time[1]	t_{RDF}		100	ns
Output Hold Time	t_{ROH}	0		ns

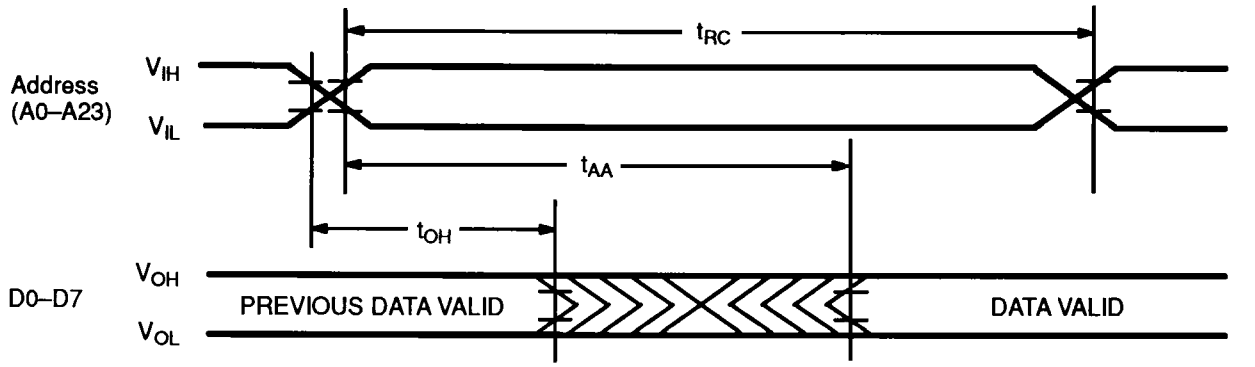
Notes: [1] t_{DF} is specified from the rising edge of $\overline{OE}$, $\overline{CE1}$ and $\overline{CE2}$, whichever occurs first. t_{DF} is defined as the point where data is no longer driven.
[2] This parameter is for MB98A51013, MB98A51113, MB98A51213, MB98A51313, and MB98A51413.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

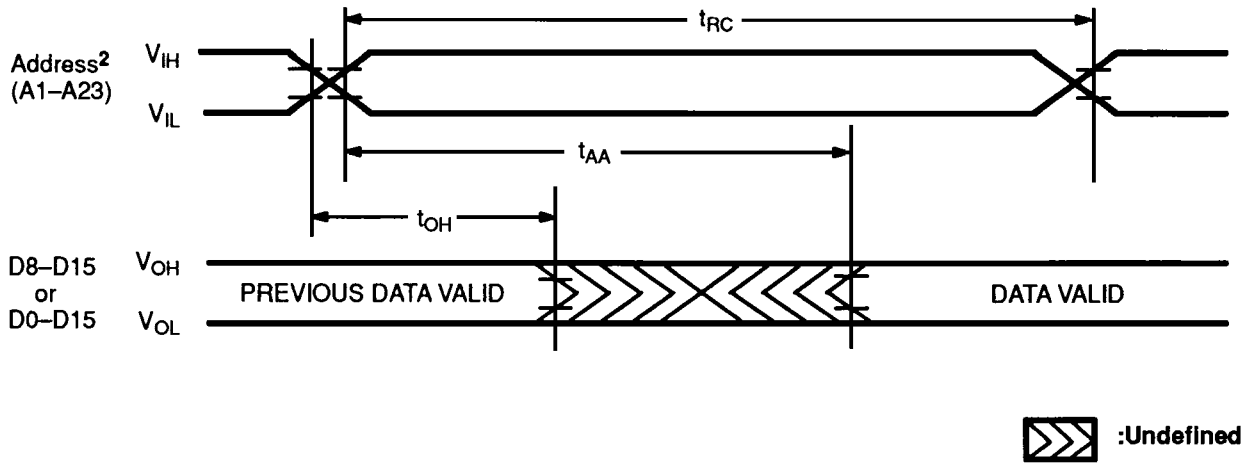
MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = V_{IH}[1], $\overline{REG}$ = V_{IH})

READ CYCLE 1: $\overline{CE1}$ = $\overline{OE}$ = V_{IL}, $\overline{CE2}$ = V_{IH}: x 8-bit Bus Organization



READ CYCLE 2: $\overline{CE1}$ = V_{IH}, $\overline{CE2}$ = $\overline{OE}$ = V_{IL}: x 8-bit Bus Organization

$\overline{CE1}$ = $\overline{CE2}$ = $\overline{OE}$ = V_{IL}: x 16-bit Bus Organization



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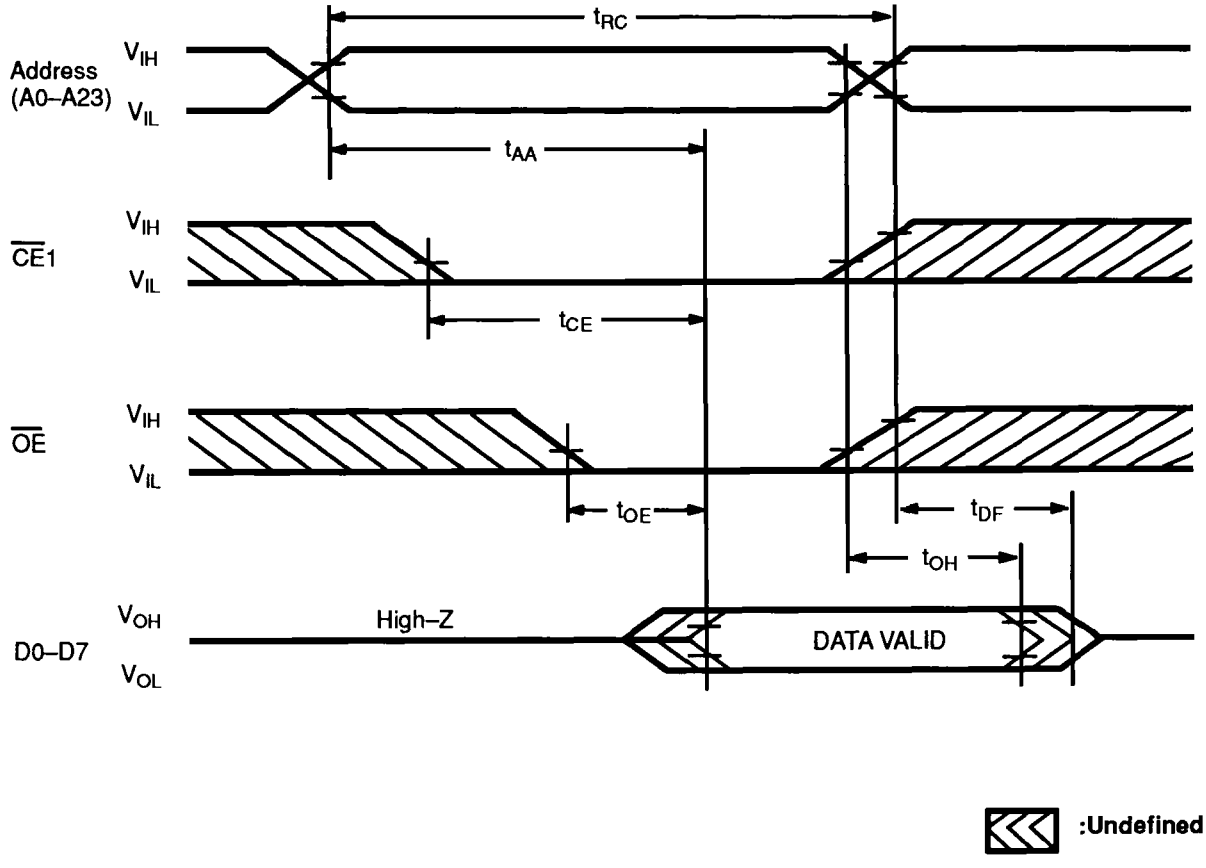
Notes: [1] This condition is for MB98A51013, MB98A51113, MB98A51213, MB98A51313, and MB98A51413.
[2] A0 = Either V_{IH} or V_{IL}.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = V_{IH}[1], $\overline{REG}$ = V_{IH})

READ CYCLE 3: $\overline{CE2}$ = V_{IH}: x 8–bit Bus Organization



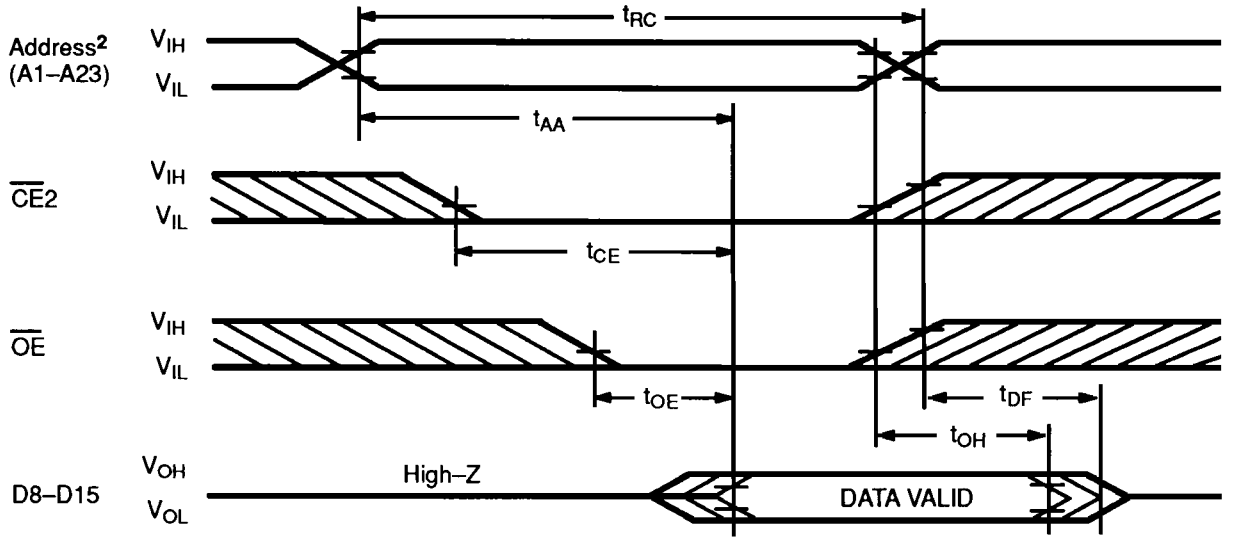
Note: [1] This condition is for MB98A51013, MB98A51113, MB98A51213, MB98A51313, and MB98A51413.

AC CHARACTERISTICS (Continued)

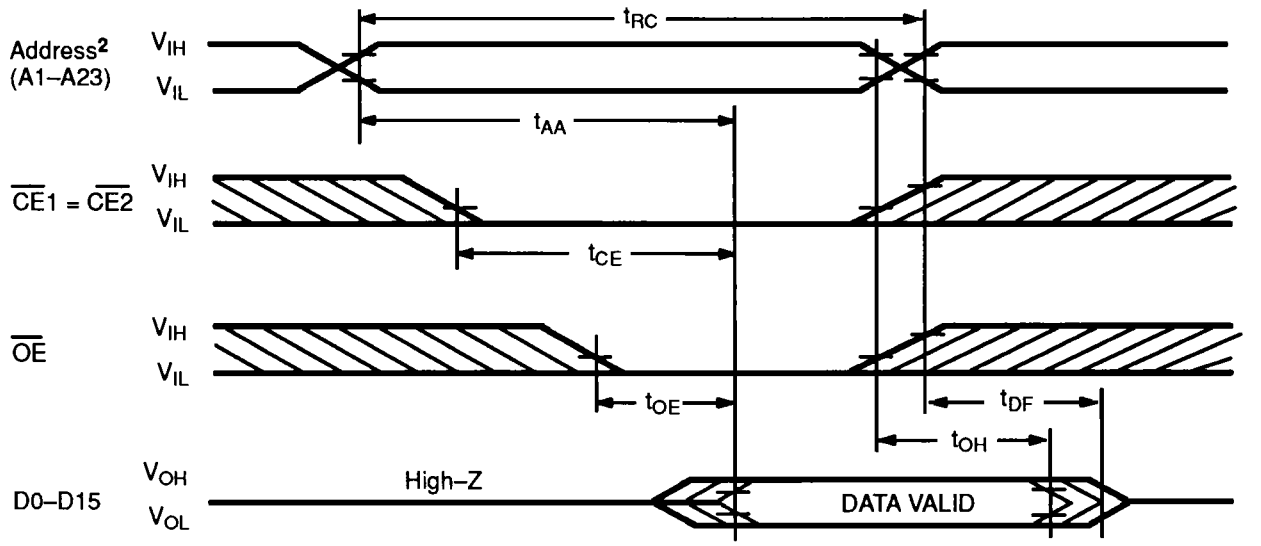
(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = V_{IH}[1], $\overline{REG}$ = V_{IH})

READ CYCLE 4: $\overline{CE1}$ = V_{IH}: x 8-bit Bus Organization



READ CYCLE 5: $\overline{CE1}$ = $\overline{CE2}$: x 16-bit Bus Organization



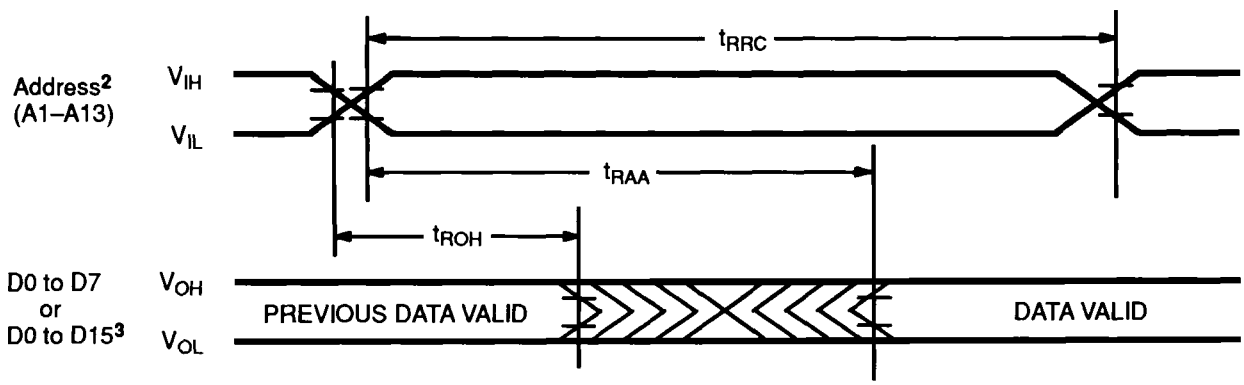
Notes: [1] This condition is for MB98A51013, MB98A51113, MB98A51213, MB98A51313, and MB98A51413.
[2] A0 = Either V_{IH} or V_{IL}.

AC CHARACTERISTICS (Continued)

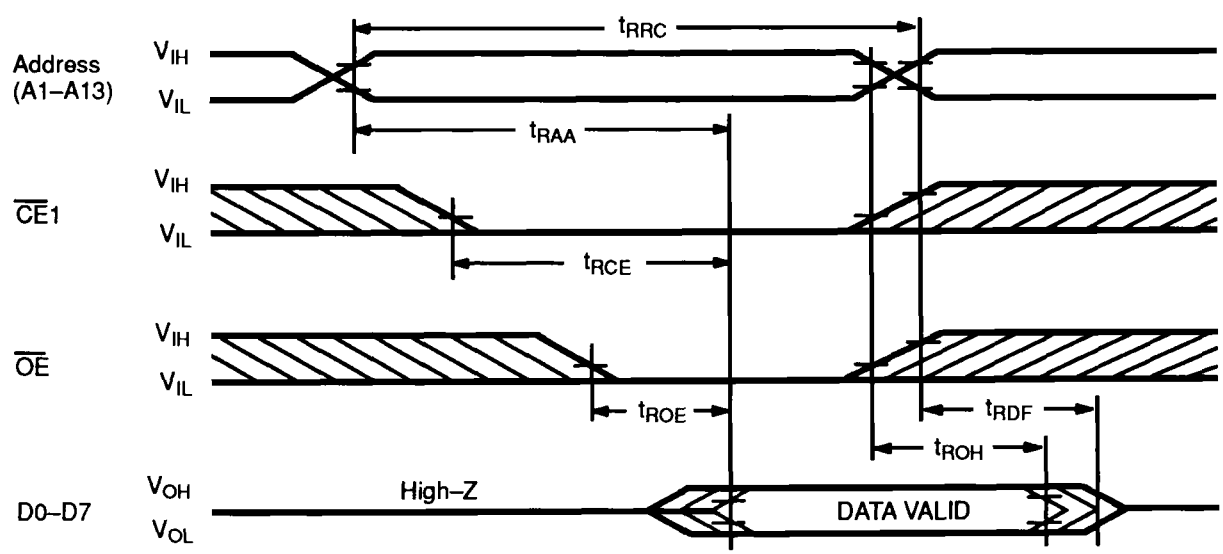
(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = V_{IH}, $\overline{REG}$ = V_{IL})[1]

READ CYCLE 1: $\overline{CE1}$ = $\overline{OE}$ = V_{IL}, $\overline{CE2}$ = V_{IH} : x 8–bit Bus Organization
$\overline{CE1}$ = $\overline{CE2}$ = $\overline{OE}$ = V_{IL} : x 16–bit Bus Organization



READ CYCLE 2: $\overline{CE2}$ = V_{IH}: x 8–bit Bus Organization



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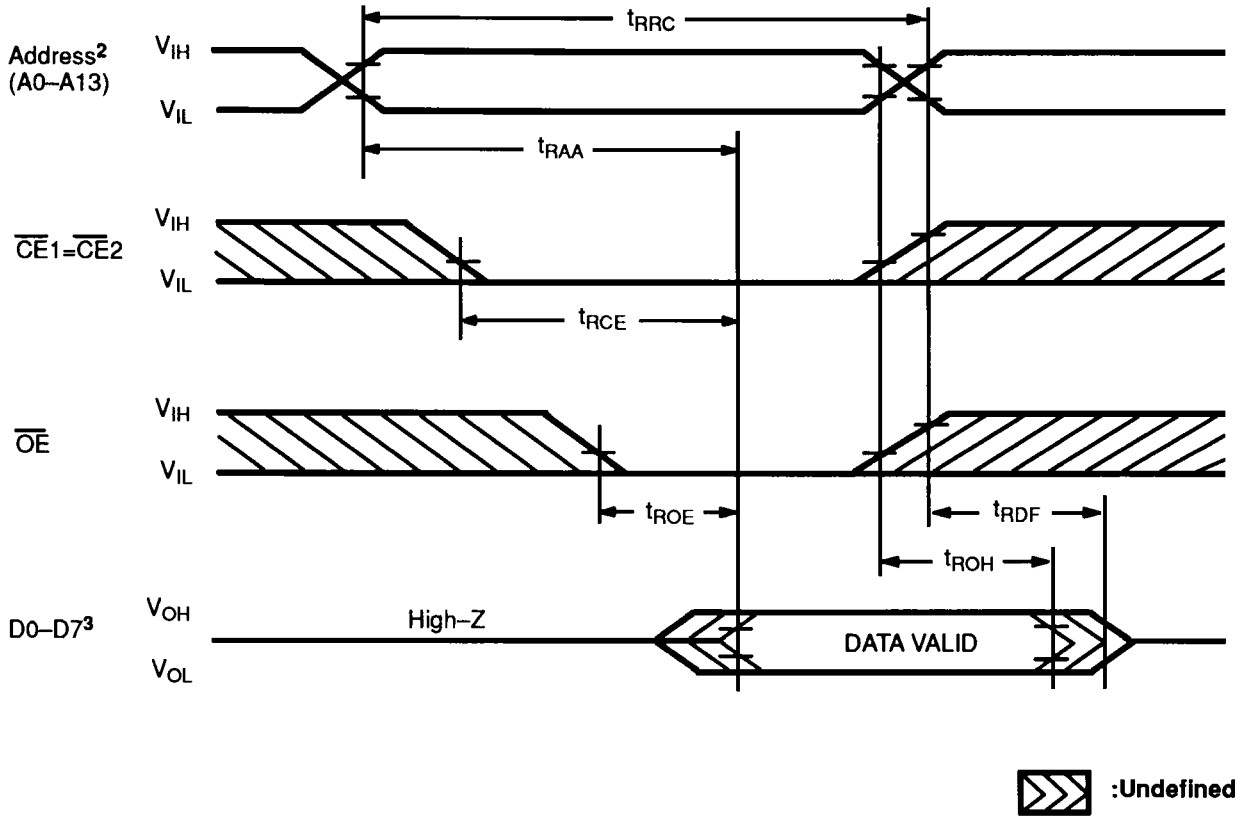
Notes: [1] These timing diagram and conditions are for MB98A51013, MB98A51113, MB98A51213, MB98A51313, and MB98A51413. "FF" data is available on MB98A51012, MB98A51112, MB98A51212, MB98A51313, and MB98A51412 only.
[2] A0 = Either V_{IH} or V_{IL} during 16 bits bus organization.
[3] H-level is output from D8 to D15.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$= V_{IH}, $\overline{REG}$ = V_{IL})[1]

READ CYCLE 3: $\overline{CE}1 = \overline{CE}2$: x 16–bit Bus Organization



Notes: [1] These timing diagram and conditions are for MB98A51013, 51113, 51213, 51313, and 51413. "FF" data is available on MB98A51012, MB98A51112, MB98A51212, MB98A51313, and MB98A51412 only.

[2] A0 = Either V_{IH} or V_{IL} during 16 bits bus organization.

[3] H-level is output from D8 to D15.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE[1]

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t_{RWR}		10	ms
Address Setup Time	t_{RAS}	20		ns
Chip Enable Setup Time	t_{RCS}	0		ns
Output Enable Setup Time	t_{ROES}	20		ns
Write Pulse Width	t_{RWP}	100		ns
Address Hold Time	t_{RAH}	50		ns
Data Setup Time	t_{RDS}	50		ns
Data Hold Time	t_{RDH}	20		ns
Chip Enable Hold Time	t_{RCH}	0		ns
Output Enable Hold Time	t_{ROEH}	20		ns
Write Recovery Time	t_{RRE}	50		ns
End of Write to Output Time	t_{RRBO}		100	ns
Number of Write per Byte	N	10000		Times
Write Enable Hold Time	t_{RWEH}	10		ns

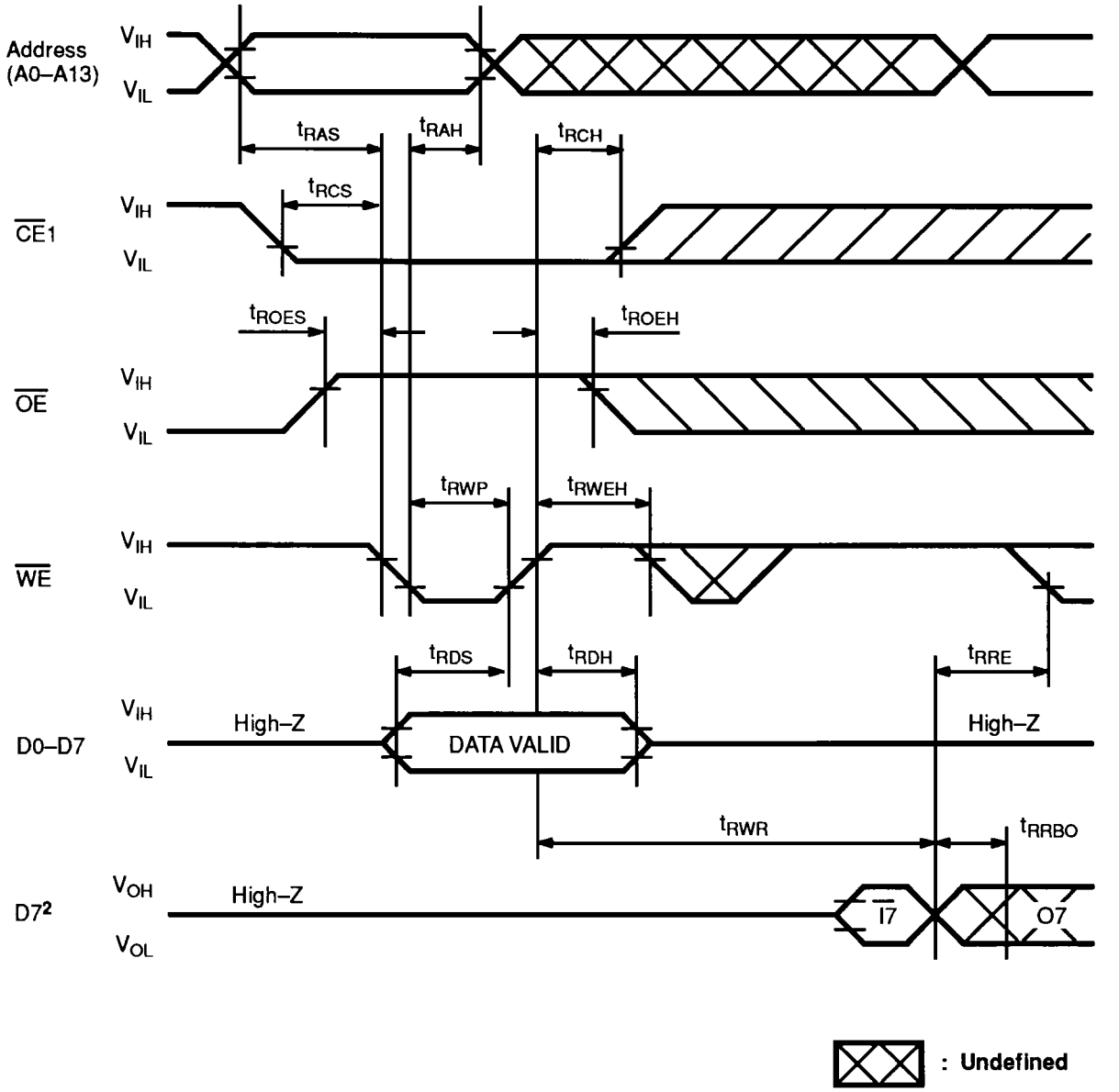
Note: [1] This parameter is for MB98A51013, MB98A51113, MB98A51213, MB98A51313, and MB98A51413.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED, $\overline{REG}$ = V_{IL})[1]

WRITE CYCLE 1: $\overline{CE2}$ = V_{IH} : x 8-bit Bus Organization

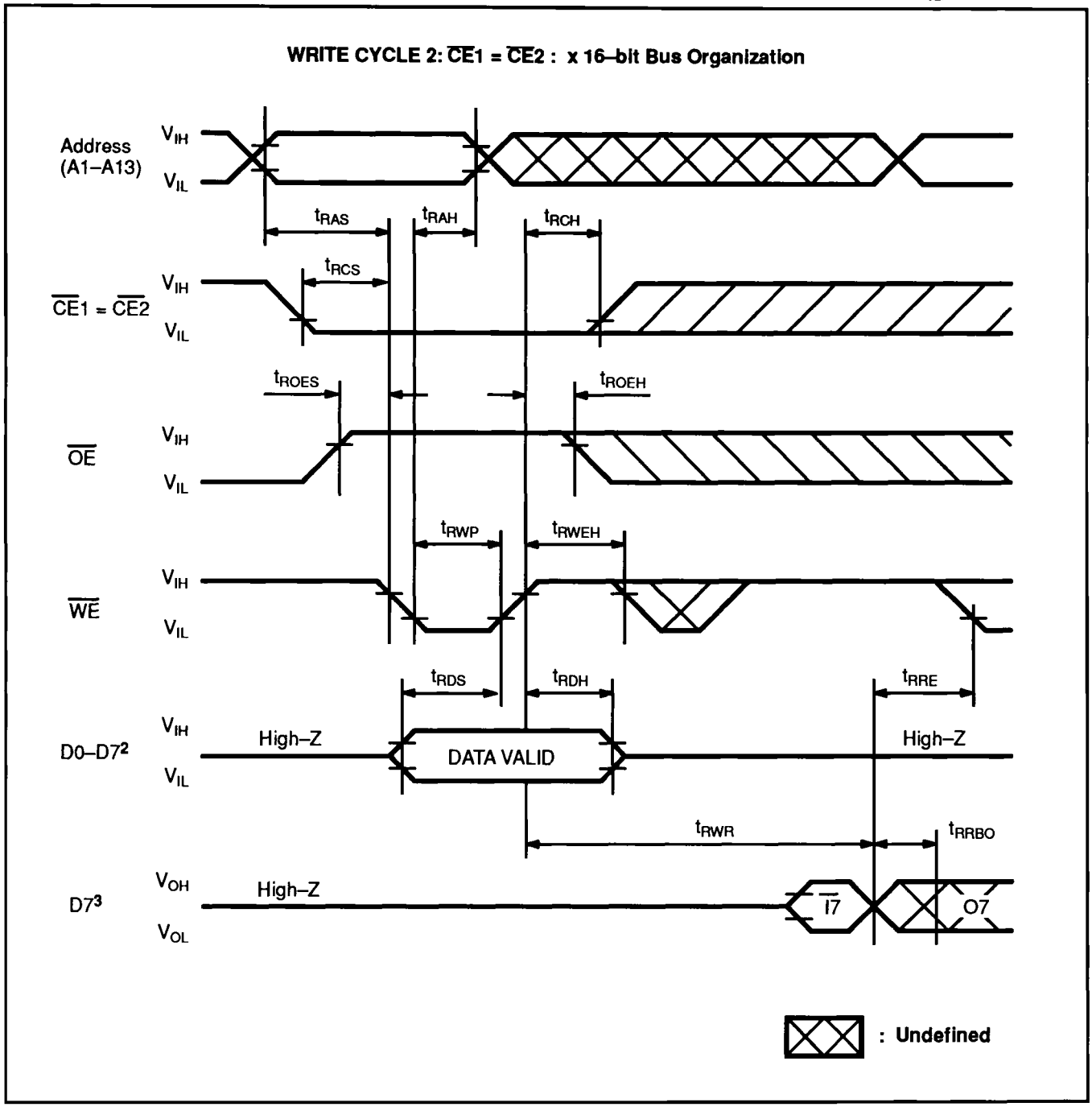


Notes: [1] These timing diagram and conditions are for MB98A51013, MB98A51113, MB98A51213, MB98A51313, and MB98A51413.
[2] Data polling operation.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED, $\overline{REG}$ = V_{IL})[1]



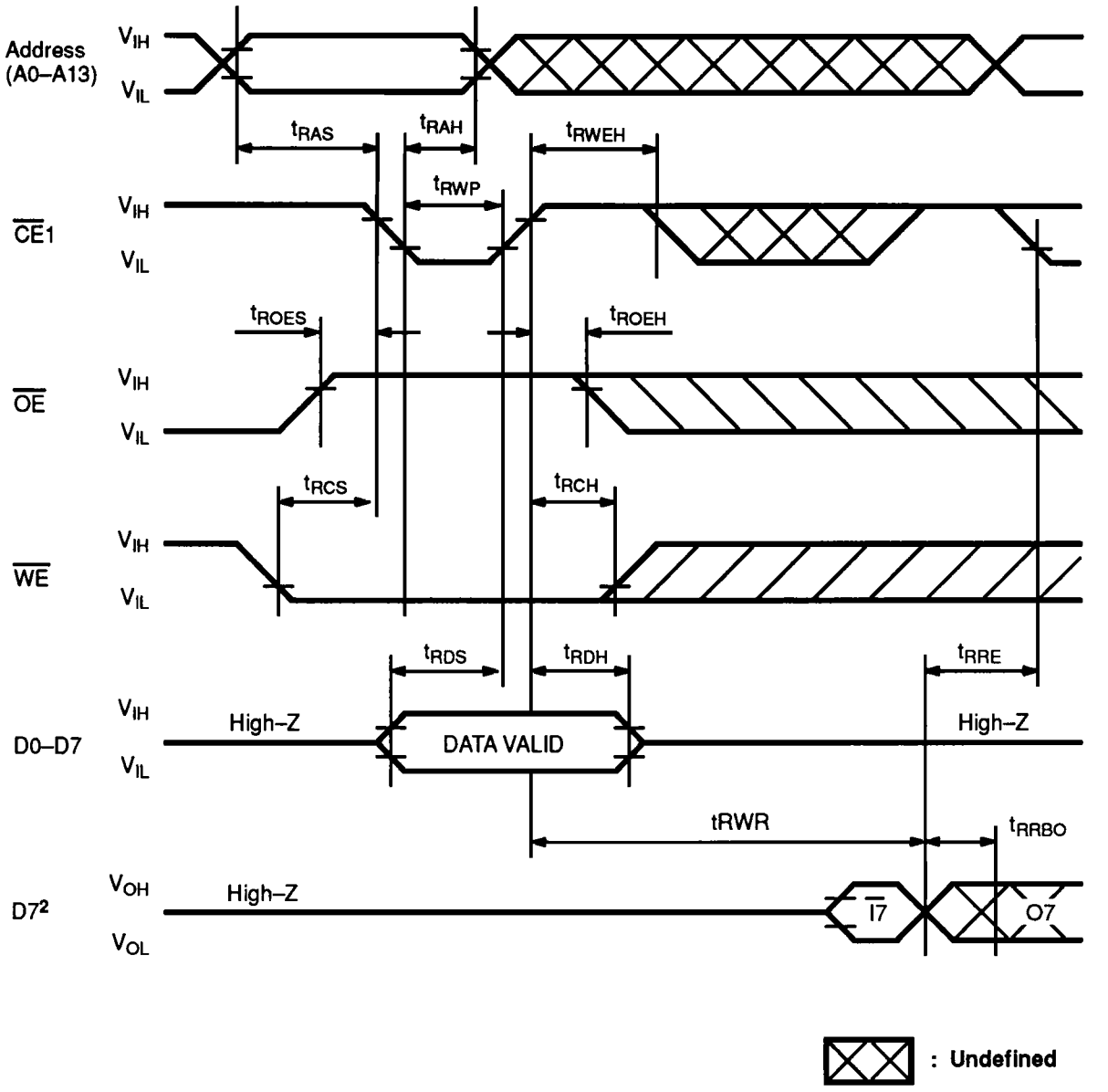
Notes: [1] These timing diagram and conditions are for MB98A51013, MB98A51113, MB98A51213, MB98A51313, and MB98A51413.
[2] Input data from D8 to D15 is invalid.
[3] Data polling operation.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE}$=CONTROLLED, $\overline{REG}$ = V_{IL})[1]

WRITE CYCLE 3: $\overline{CE2}$ = V_{IH} : x 8–bit Bus Organization

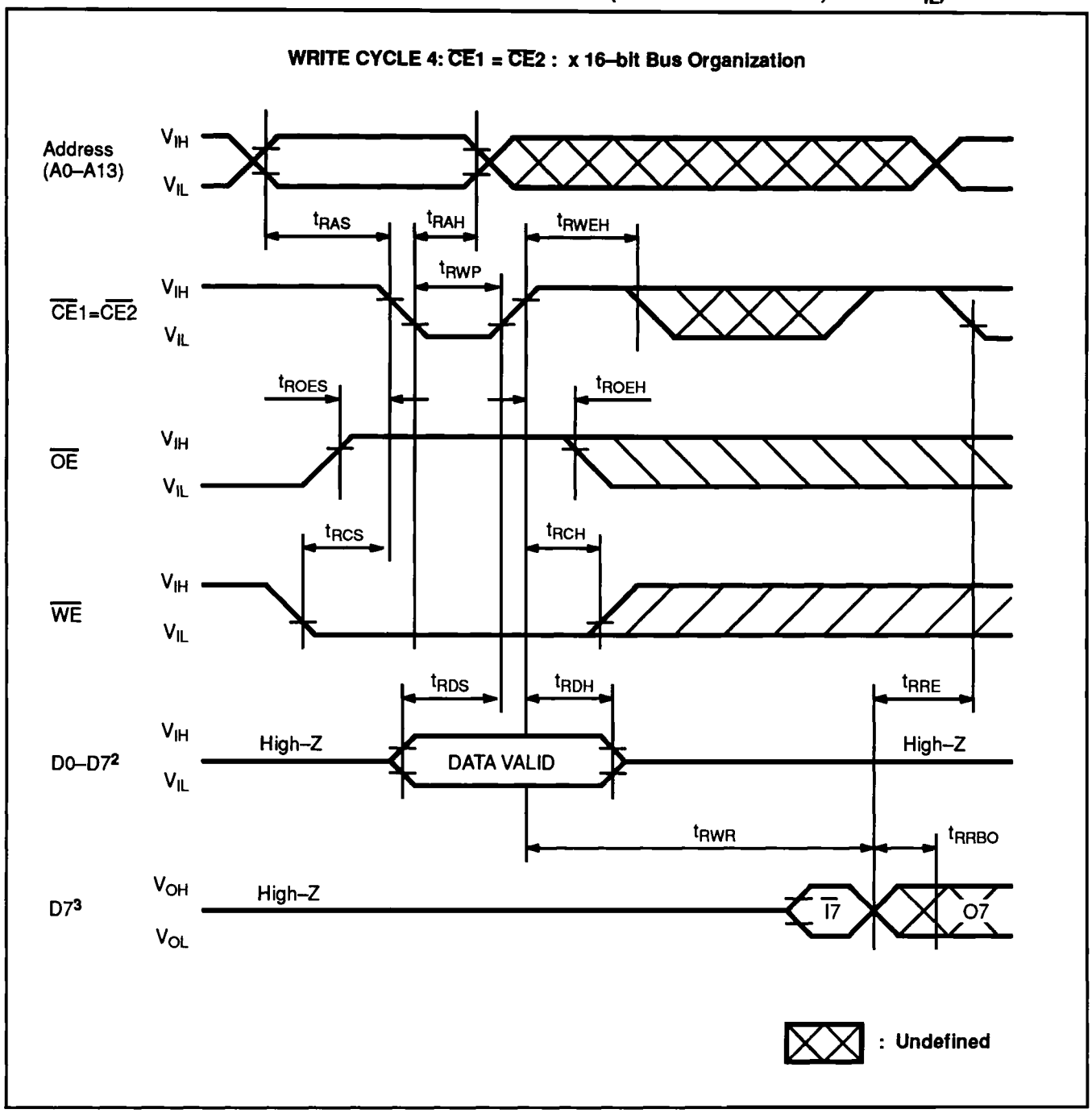


Notes: [1] These timing diagram and conditions are for MB98A51013, MB98A51113, MB98A51213, MB98A51313, and MB98A51413.
[2] Data polling operation.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED, $\overline{REG}$ = V_{IL})[1]



Notes: [1] These timing diagram and conditions are for MB98A51013, MB98A51113, MB98A51213, MB98A51313, and MB98A51413.
[2] Input data from D8 to D15 is invalid.
[3] Data polling operation.

UNIQUE FEATURE FOR MASK ROM CARD

1. SPECIAL MONITORING PINS

$\overline{CD1}$, $\overline{CD2}$: Card Detection Pins

These pins detect the insertion of the card into the system. (See Figure 5.)
When the memory card has been correctly inserted, $\overline{CD1}$ and $\overline{CD2}$ are detected by the system. $\overline{CD1}$, $\overline{CD2}$ are tied to ground on the card side as shown in Figure 5.

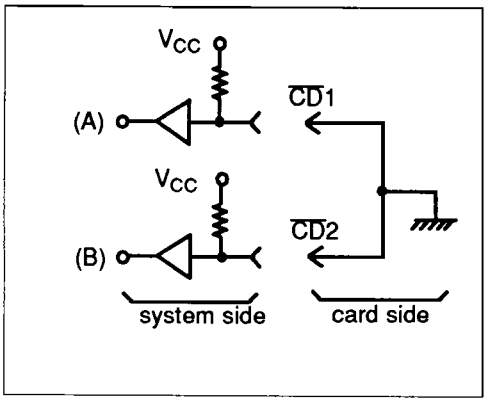
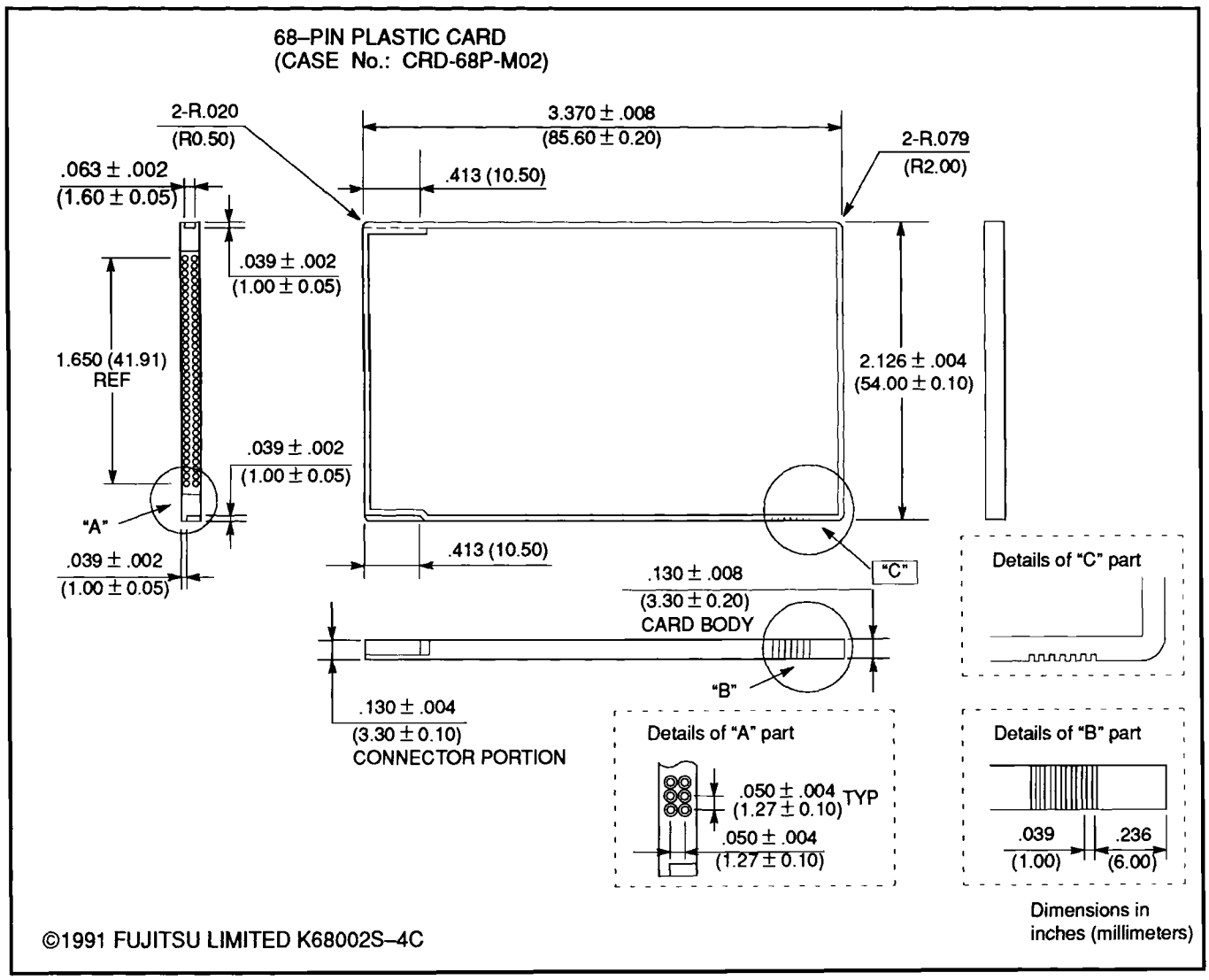


Figure 5. Card Detection Pins

PACKAGE DIMENSIONS



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