DRAM DIE

4 MEG DRAM

1 MEG x 4, 4 MEG x 1

FEATURES

- Single 5.0V power supply
- Industry-standard timing and functions
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are TTL- and CMOS-compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN
- FAST PAGE MODE access cycle

GENERAL PHYSICAL SPECIFICATIONS

- Wafer thickness = 18.5 mils ±0.5 mils
- Backside wafer surface of polished bare silicon
- Typical metalization thickness 9.2K angstroms
- Metalization composition: 99.5% Al and 0.5% Cu over titanium
- Typical topside passivation 8K angstroms undoped oxide with 4K angstroms of nitride over oxide
- Typical pad openings: 4.4 x 4.4 mil
  111 x 111 µm

OPTIONS — ORDER NUMBER

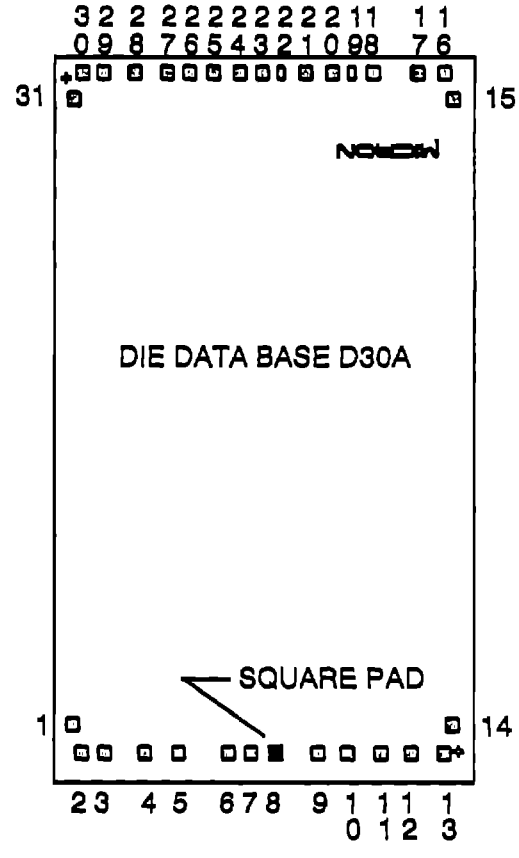
• Speed probing	
No speed probing	None
60ns access	-6*
70ns access	-7*
80ns access	-8
• Form	
Die	D
Wafer (6" wafer)	W
• Testing levels	
Standard probe	C1
Speed probe	C2
Burned-in	C3
Known Good Die	C7

*Not available as C1 level product.

ORDER INFORMATION

• 4 Meg x 1	MT4C1004JD30A
• 1 Meg x 4	MT4C4001JD30A

DIE OUTLINE (Top View)



Die size: 158 x 274 mil
4,013 x 6,960 µm
See Bond Pad Location and Identification Table.

PRODUCT #	DIE DATABASE	FORM	TESTING LEVEL	SPEED

MT4C4001JD30ADC2-6

MICTS054

DIE TESTING PROCEDURES

Micron has established four testing levels for die products. Most Micron products are tested to Standard Probe (C1) level. Selected products are available as Speed Probe (C2) level. Customers especially concerned with reducing the infant mortality rate may choose the Burned-In (C3) level. Known Good Die (C7) level product is available on selected products as market demand dictates. Level C2, C3 and C7 products are designed to provide customers with improved yields over C1.

STANDARD PROBE (C1)

Micron probes wafers at a temperature with limits guardbanded to assure product performance from 0°C to 70°C in Micron's standard package. Since the package environment is not within Micron's control, the user must determine the necessary heat sinking requirements to ensure that the die junction temperature remains within specified limits. A high voltage functional stress test will be performed at probe to assure minimum junction breakdown integrity. V_{BB} (substrate bias voltage) is a forced condition at wafer probe.

Wafer probe consists of various functional and parametric tests of each die. Test patterns, timing, voltage margins, limits and test sequence are determined by individual product yields and reliability data.

Micron retains a wafer map of each wafer as part of the probe records along with a lot summary of wafer yields for each lot probed. Micron reserves the right to change the probe program at any time to improve the reliability, packaged device yield or performance of the product.

SPEED PROBE (C2)

In addition to the testing performed at Standard Probe (C1), Micron also offers Speed Probe (C2). Micron's Hot Chuck Speed Probe assures the speed performance of die products for the fastest speed grades. Although speed probing tests for most data sheet parameters may increase the yield a customer may see over C1-level, C2-level die has not received burn-in and therefore is still subject to infant mortality failures.

BURNED-IN (C3)

Burned-in die incorporates all the testing done in the C2-level die as well as a burn-in step. The addition of the intelligent burn-in operates the parts until they have passed the infant mortality stage.

KNOWN GOOD DIE (C7)

In order to provide the customer with fully warranted die product, Micron has developed a Known Good Die process designed to provide customers with die products of equal quality and reliability to packaged product. Micron's KGD$^{Plus®}$ process allows Micron to fully test and burn-in die product after it has been tested to C1 level.

FUNCTIONAL SPECIFICATIONS

Please refer to the packaged product data sheets found in the applicable Micron data book, for functional and parametric specifications. The specifications are provided for reference only on C1- and C2-level die product. On C2 and C3-level product ^{t}RAC and ^{t}CAC is guaranteed. C7-level product is warranted to the data sheet.

DIE AND WAFER LEVEL CONSIDERATIONS

Only C1- and C2-level products are available in wafer level form. Burned-in die or KGD die are available only in die form. C2-level wafers are shipped with a user's wafer map indicating speed. Users should be aware that there may be multiple speed grades on wafers shipped with a C2 level.

BONDING INSTRUCTIONS

The D30A DRAM die has 31 bond pads. Refer to the bond pad location and identification table for a complete list of bond pads and coordinates.

The D30A DRAM die has an internal substrate bias generator for normal operation, bond pad 25 is used for manufacturing tests only. Normal bonding leaves bond pad 25 open (not bonded) or connected to the isolated substrate which the die is mounted to. Micron recommends using a bond wire on each Vcc and Vss bond pad for improved noise immunity. It is important that the back of the die be kept isolated from any other devices sharing a common package or substrate, since the die substrate is internally driven to a negative voltage.

WAFER SAW

Standard wafer saw cuts the die 100 percent through. Micron holds die dimensions to a maximum tolerance of +0/-1 mil of each cut, as measured from the vertical cut. For clarification purposes, the die size provided is measured from center to center of the die street. A finished die is approximately 1.5 mils smaller on each side due to the sawing operation. As an example: a 158 x 274 die is approximately 156.5 x 272.5 mils after sawing.

PACKAGING

For packaging, Micron utilizes Gel-Pak®. We package all die with the top metalization consistently oriented (refer to Figure 1). External packaging is suitable for electrostatic discharge protection. Each package is individually self-locking or closed with a conductive clip and labeled with the following information:

- Generic device type and data base (Example: 4001JD30A)
- Micron fabrication lot number
- Speed grade of the die (optional)
- Quantity of die in package

STORAGE REQUIREMENTS

Micron die products are packaged in a cleanroom environment for shipping. Upon receipt, the customer should transfer the Gel-Pak to a similar environment for storage. Micron recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

PRODUCT RELIABILITY MONITORS

Reliability of all products is monitored by ongoing QA reliability evaluations. Micron's QA department samples product families on a continuous basis for reliability studies. These studies include high temperature operating life (HTOL) tests for failure in time (FIT) calculations and high temperature steady state (HTSS) tests to monitor electromigration reliability. A summary of these product family evaluations is published on a regular basis.

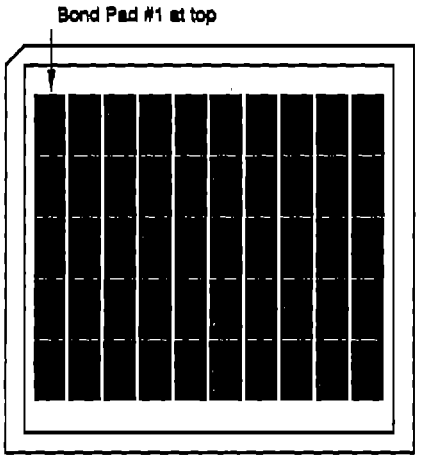
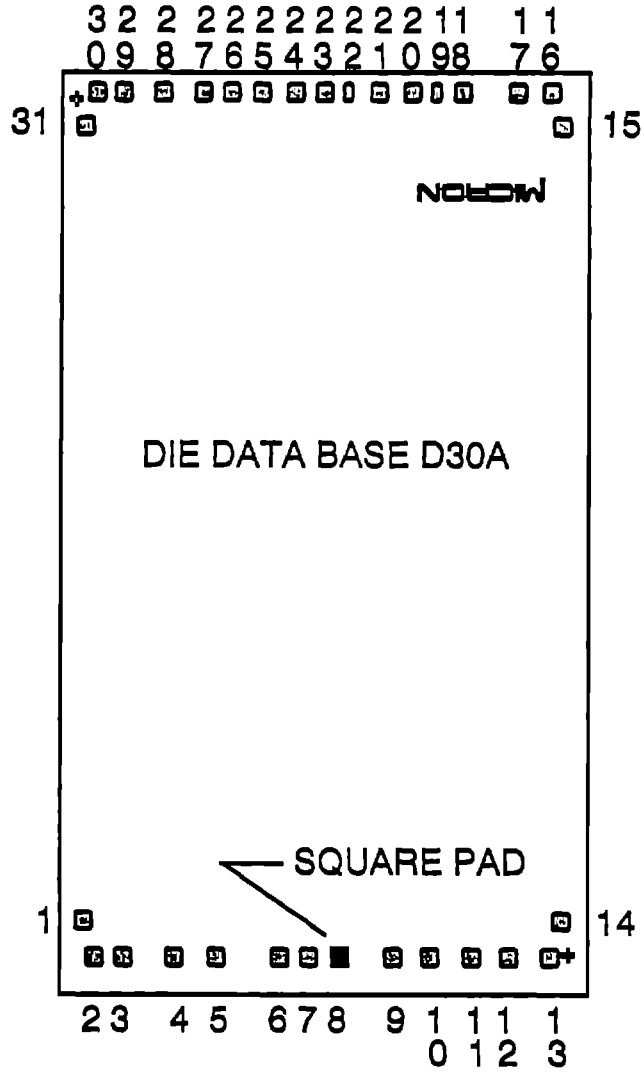


Figure 1
ORIENTATION OF DIE IN GEL-PAK

BOND PAD LOCATION AND IDENTIFICATION TABLE						
			FROM CENTER OF #1			
PAD #	MT4C1004J	MT4C4001J	"X" MILS	"Y" MILS	"X" MICRONS	"Y" MICRONS
1	A9	OE	0.000	0.000	0.0	0.0
2	DNU	DNU	-9.589	-3.547	-243.6	-90.1
3	CAS	CAS	-9.589	-11.553	-243.6	-293.4
4	DNU	DQ3	-9.589	-25.492	-243.6	-647.5
5	DOUT	DQ4	-9.589	-37.337	-243.6	-948.3
6	Vss	Vss	-9.589	-62.177	-243.6	-1579.3
7	Vss	Vss	-9.589	-69.900	-243.6	-1775.5
8	DIN	DNU	-9.554	-77.638	-242.7	-1972.0
9	DNU	DQ1	-9.589	-91.691	-243.6	-2329.0
10	DNU	DQ2	-9.589	-103.802	-243.6	-2636.6
11	WE	WE	-9.589	-118.041	-243.6	-2998.2
12	RAS	RAS	-9.589	-129.026	-243.6	-3277.3
13	DNU	DNU	-9.589	-139.633	-243.6	-3546.7
14	A10	A9	0.473	-143.443	12.0	-3643.5
15	A0	A0	241.840	-143.650	6141.7	-3648.7
16	DNU	DNU	249.976	-137.476	6349.4	-3491.9
17	A1	A1	249.976	-129.602	6349.4	-3291.9
18	A2	A2	249.976	-115.650	6349.4	-2937.5
19	DNU	DNU	249.976	-106.770	6349.4	-2712.0
20	A3	A3	249.976	-100.447	6349.4	-2551.4
21	DNU	Vcc	249.976	-92.568	6349.4	-2351.2
22	DNU	DNU	249.976	-82.345	6349.4	-2091.6
23	Vcc	Vcc	249.976	-76.150	6349.4	-1934.2
24	Vcc	Vcc	249.976	-67.230	6349.4	-1707.6
25	Vss	Vss	249.976	-57.360	6349.4	-1457.0
26	A4	A4	249.976	-49.467	6349.4	-1256.5
27	A5	A5	249.976	-41.590	6349.4	-1056.4
28	A6	A6	249.976	-27.461	6349.4	-697.5
29	A7	A7	249.976	-13.181	6349.4	-334.8
30	DNU	DNU	249.976	-5.308	6349.4	-134.8
31	A8	A8	242.170	0.165	6151.1	4.2

NOTE: DNU stands for "do not use."

DIE OUTLINE (Top View)



Wafer diameter: 150mm
Wafer thickness: 18.5 mil ±0.5 mil
Die size: 158 x 274 mil
(stepping interval)
4,013 x 6960 µm
Bond pad size: 5.1 x 5.1 mil
128 x 128 µm
Passivation Openings (typical): 4.4 x 4.4 mil
111 x 111 µm