

**MCM67Q004**

*Product Preview*

**1M x 4 BiCMOS Self-Timed Synchronous SRAM with TTL I/O**

The Motorola MCM67Q004J and MCM67Q004T are 4,194,304 bit synchronous, high-speed, BiCMOS, TTL Static RAMs organized as 1,048,576 words of 4 bits each. This device is fabricated using Motorola's high performance silicon gate BiCMOS technology. They feature separate TTL input and output buffers and incorporate input and output registers on board with high speed SRAM.

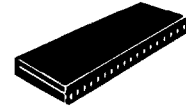
The synchronous design allows for precise cycle control with the use of an external single clock (CK). The Addresses (A0 - A19), Data Inputs (D0 - D3), Data Outputs (Q0 - Q3), Write-Enable ( $\bar{W}$ ), and Chip-Enable ( $\bar{E}$ ), are all registered in on the rising edge of Clock (CK).

Write operations are internally self-timed and initiated by sampling  $\bar{W}$  low at the rising edge of Clock (CK).

- 1M x 4 Bit Fast Access Static Memory Array
- 5 V  $\pm$  10% Power Supply
- Single Clock Operation
- Self-Timed Write Feature
- Input Signal Line Clamp Diode Implementation
- TTL Input and Output Levels
- Address, Data Input, Data Output,  $\bar{E}$ , and  $\bar{W}$  Registers on Chip
- 67 MHz Maximum Clock Cycle Time
- Separate Data Input and Data Output Pins
- 36-Pin, 400 Mil, SOJ and TSOP Packaging



T PACKAGE  
400 MIL TSOP  
CASE 907

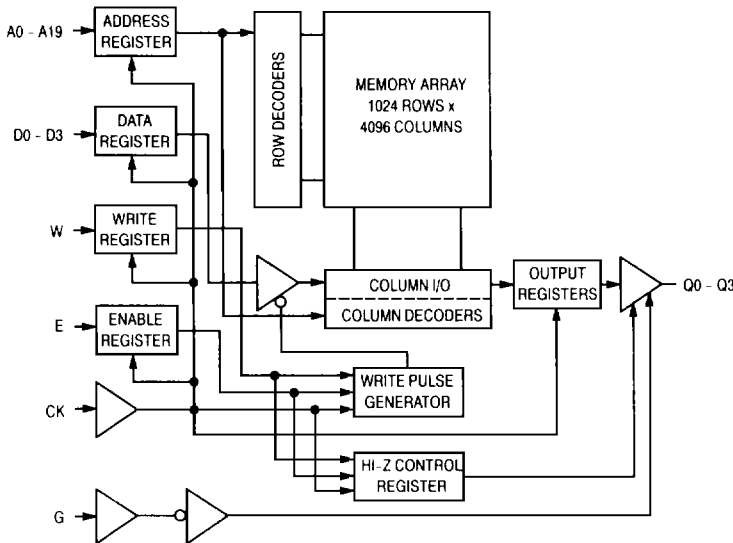


WJ PACKAGE  
400 MIL SOJ  
CASE 893

**PIN ASSIGNMENT**

A0	1	36	A19
A1	2	35	A18
A2	3	34	A17
A3	4	33	A16
A4	5	32	A15
E	6	31	$\bar{G}$
D0	7	30	D3
Q0	8	29	Q3
VCC	9	28	VSS
VSS	10	27	VCC
Q1	11	26	Q2
D1	12	25	D2
$\bar{W}$	13	24	CK
A5	14	23	A14
A6	15	22	A13
A7	16	21	A12
A8	17	20	A11
A9	18	19	A10

**BLOCK DIAGRAM**



**PIN NAMES**

CK	.....	Clock
$\bar{W}$	.....	Write Enable Input
D0 - D3	.....	Data Inputs
E	.....	Chip Enable Bar Input
$\bar{G}$	.....	Output Enable Bar Input
A0 - A19	.....	Address Inputs
Q0 - Q3	.....	Data Outputs
VCC	.....	Power Supply (+ 5 V)
VSS	.....	Power Supply (Ground)

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