

# 4 x 8-bit Multilevel Pipeline Register

# L29C520/521

T-46-09-09

## FEATURES

## DESCRIPTION

- ❑ Four 8-bit Registers
- ❑ Implements Double 2-Stage Pipeline or Single 4-Stage Pipeline Register
- ❑ Hold, Shift, Load Instructions
- ❑ Separate Data In and Data Out Pins
- ❑ High Speed, Low Power CMOS Technology
- ❑ Three-State Outputs
- ❑ Available 100% Screened to MIL-STD-883, Class B
- ❑ Plug Compatible with AMD AM29520 and AM29521
- ❑ Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin CerDIP
  - 24-pin Sidebrazed, Hermetic DIP
  - 24-pin Ceramic Flatpack
  - 28-pin Plastic LCC, J-Lead
  - 28-pin Ceramic LCC (Type C)

The Logic Devices L29C520 and L29C521 are pin-for-pin compatible with the Advanced Micro Devices AM29520 and AM29521, implemented in low power CMOS.

The L29C520 and L29C521 contain four registers which can be configured as two independent, 2-level pipelines or as one 4-level pipeline.

The Instruction pins, I<sub>0</sub> and I<sub>1</sub>, control the loading of the registers. For either device, the registers may be configured as a four-stage delay line, with data loaded into R<sub>1</sub> and shifted sequentially through R<sub>2</sub>, R<sub>3</sub>, and R<sub>4</sub>. Also, for the L29C520, data may be loaded from the inputs into either R<sub>1</sub> or R<sub>3</sub> with only R<sub>2</sub> or R<sub>4</sub> shifting. The L29C521 devices differ from the L29C520 in that R<sub>2</sub> and R<sub>4</sub> remain unchanged during this type of data load, as shown in Tables 1 and 2. Finally, I<sub>0</sub> and I<sub>1</sub> may be set to prevent any register from changing.

The S<sub>0</sub> and S<sub>1</sub> select lines control a 4 to 1 multiplexer which routes the contents of any of the registers to the Y output pins. The independence of

the I and S controls allows simultaneous write and read operations on different registers.

TABLE 1

I <sub>1</sub>	I <sub>0</sub>	L29C520 Instruction
L	L	D→R <sub>1</sub> R <sub>1</sub> →R <sub>2</sub> R <sub>2</sub> →R <sub>3</sub> R <sub>3</sub> →R <sub>4</sub>
L	H	HOLD HOLD D→R <sub>3</sub> R <sub>3</sub> →R <sub>4</sub>
H	L	D→R <sub>1</sub> R <sub>1</sub> →R <sub>2</sub> HOLD HOLD
H	H	ALL REGISTERS ON HOLD

TABLE 2

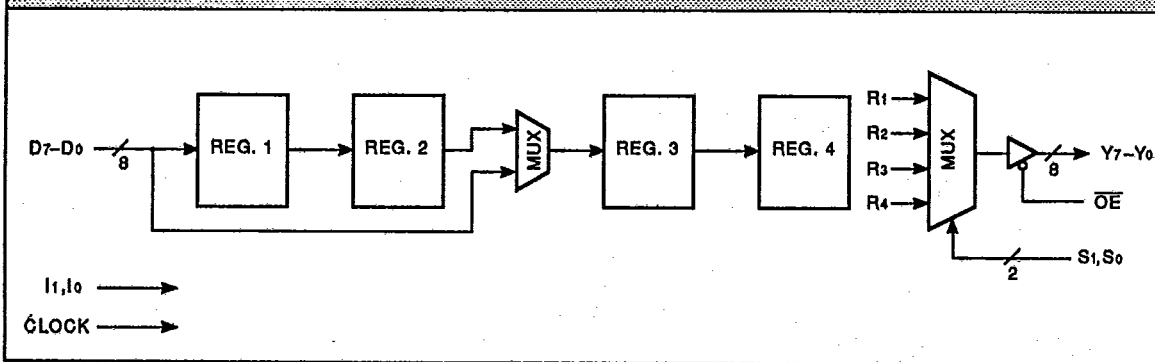
I <sub>1</sub>	I <sub>0</sub>	L29C521 Instruction
L	L	D→R <sub>1</sub> R <sub>1</sub> →R <sub>2</sub> R <sub>2</sub> →R <sub>3</sub> R <sub>3</sub> →R <sub>4</sub>
L	H	HOLD HOLD D→R <sub>3</sub> HOLD
H	L	D→R <sub>1</sub> HOLD HOLD HOLD
H	H	ALL REGISTERS ON HOLD

TABLE 3

S <sub>1</sub>	S <sub>0</sub>	Reg. Selected
L	L	Reg 4
L	H	Reg 3
H	L	Reg 2
H	H	Reg 1

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## L29C520/521 BLOCK DIAGRAM



**4 x 8-bit Multilevel Pipeline Register**

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**MAXIMUM RATINGS** Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature .....	-65°C to +150°C
Operating ambient temperature .....	-55°C to +125°C
Vcc supply voltage with respect to ground .....	-0.5 V to +7.0 V
Input signal with respect to ground .....	-3.0 V to +7.0 V
Signal applied to high impedance output .....	-3.0 V to +7.0 V
Output current into low outputs .....	25 mA
Latchup current .....	> 400 mA

**OPERATING CONDITIONS** To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ Vcc ≤ 5.25 V
Active Operation, Military	-55°C to +125°C	4.50 V ≤ Vcc ≤ 5.50 V

**ELECTRICAL CHARACTERISTICS** Over Operating Conditions

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	IOH = -6.5 mA	3.5			V
VOL	Output Low Voltage	IOL = 20.0 mA			0.5	V
VIH	Input High Voltage		2.0		Vcc	V
VIL	Input Low Voltage	(Note 3)	0.0		0.8	V
IIX	Input Current	Ground ≤ VIN ≤ Vcc			±20	µA
IOLZ	Output Leakage Current	Ground ≤ VOUT ≤ Vcc			±20	µA
IOS	Output Short Current	VOUT = Ground, Vcc = Max (Notes 4, 8)			-250	mA
ICC1	Vcc Current, Dynamic	(Notes 5, 6)		10	15	mA
ICC2	Vcc Current, Quiescent	(Note 7)			1.0	mA



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**SWITCHING CHARACTERISTICS**

**COMMERCIAL OPERATING RANGE (0°C to +70°C) Notes 9, 10 (ns)**

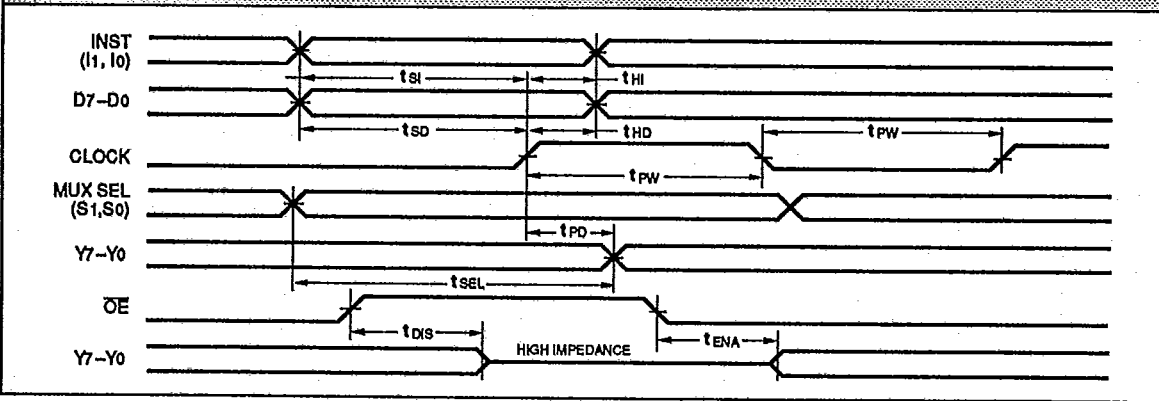
Symbol	Parameter	L29C520/521-			
		25		22	
		Min	Max	Min	Max
t <sub>PD</sub>	CLK to Y7-Y0		25		22
t <sub>SEL</sub>	S1,S0 to Y7-Y0		25		20
t <sub>SD</sub>	D7-D0 to CLK Setup	13		10	
t <sub>HD</sub>	CLK to D7-D0 Hold	3		3	
t <sub>SI</sub>	I1,I0 to CLK Setup	13		10	
t <sub>HI</sub>	CLK to I1,I0 Hold	3		3	
t <sub>DIS</sub>	OE to Output Disable (Note 11)		25		15
t <sub>ENA</sub>	OE to Output Enable (Note 11)		25		21
t <sub>PW</sub>	Clock Pulse Width	10		10	

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**MILITARY OPERATING RANGE (-55°C to +125°C) Notes 9, 10 (ns)**

Symbol	Parameter	L29C520/521-			
		30		24	
		Min	Max	Min	Max
t <sub>PD</sub>	CLK to Y7-Y0		30		24
t <sub>SEL</sub>	S1,S0 to Y7-Y0		30		22
t <sub>SD</sub>	D7-D0 to CLK Setup	15		10	
t <sub>HD</sub>	CLK to D7-D0 Hold	5		3	
t <sub>SI</sub>	I1,I0 to CLK Setup	15		10	
t <sub>HI</sub>	CLK to I1,I0 Hold	5		3	
t <sub>DIS</sub>	OE to Output Disable (Note 11)		20		16
t <sub>ENA</sub>	OE to Output Enable (Note 11)		25		22
t <sub>PW</sub>	Clock Pulse Width	15		10	

**SWITCHING WAVEFORMS**



**NOTES**

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above VCC will be clamped beginning at -0.6 V and VCC + 0.6 V. The device can withstand indefinite operation with inputs in the range of -3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

- N = total number of device outputs
- C = capacitive load per output
- V = supply voltage
- F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of VCC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except  $t_{EN}/t_{DIS}$  test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified IOL and IOH plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1  $\mu$ F ceramic capacitor should be installed between VCC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device VCC and the tester common, and device ground and tester common.

b. Ground and VCC supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and VCC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured  $\pm 200$  mV from steady-state voltage with specified loading.

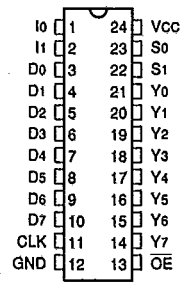
4 x 8-bit Multilevel Pipeline Register

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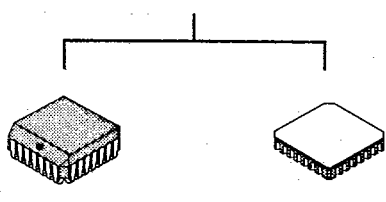
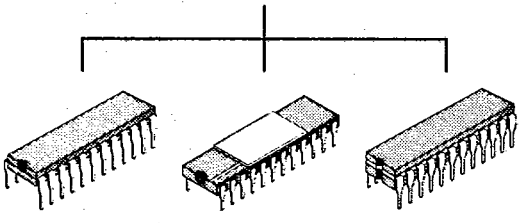
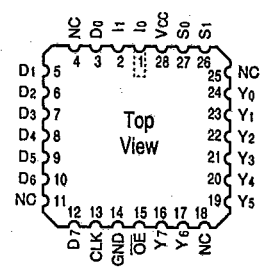
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ORDERING INFORMATION

24-pin  
(0.3" wide)



28-pin



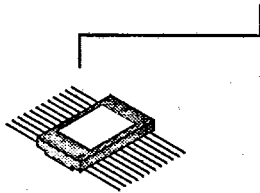
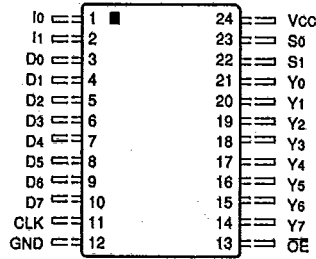
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Speed	Plastic DIP (P2)	Slidebrazed Hermetic DIP (D2)	CarDIP (C1)	Plastic J-Lead Chip Carrier (J4)	Ceramic Leadless Chip Carrier (K1)
<b>0°C to +70°C — COMMERCIAL SCREENING</b>					
25 ns 22 ns	L29C520PC or L29C521PC	L29C520DC or L29C521DC	L29C520CC or L29C521CC	L29C520JC or L29C521JC	L29C520KC or L29C521KC
<b>-55°C to +125°C — COMMERCIAL SCREENING</b>					
30 ns 24 ns		L29C520DM or L29C521DM	L29C520CM or L29C521CM		L29C520KM or L29C521KM
<b>-55°C to +125°C — EXTENDED SCREENING</b>					
30 ns 24 ns		L29C520DME or L29C521DME	L29C520CME or L29C521CME		L29C520KME or L29C521KME
<b>-55°C to +125°C — MIL-STD-883 COMPLIANT</b>					
30 ns 24 ns		L29C520DMB or L29C521DMB	L29C520CMB or L29C521CMB		L29C520KMB or L29C521KMB

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**ORDERING INFORMATION**

24-pin



Speed	Flatpack (F1)		
<b>0°C to +70°C — COMMERCIAL SCREENING</b>			
25 ns 22 ns	L29C520FC or L29C521FC	┌ 25 └ 22	
<b>-55°C to +125°C — COMMERCIAL SCREENING</b>			
30 ns 24 ns	L29C520FM or L29C521FM	┌ 30 └ 24	
<b>-55°C to +125°C — EXTENDED SCREENING</b>			
30 ns 24 ns	L29C520FME or L29C521FME	┌ 30 └ 24	
<b>-55°C to +125°C — MIL-STD-883 COMPLIANT</b>			
30 ns 24 ns	L29C520FMB or L29C521FMB	┌ 30 └ 24	