RC229ATF/1 Low Power Integrated Data/Fax Single Device Modem Family

INTRODUCTION

The Rockwell RC229ATF/1 is a combined 2400 bps data and 9600 bps fax modem family available in a single 100-pin plastic quad flat pack (PQFP). This modem family represents the highest level of integration available in the industry today, and provides the modem OEM with the lowest system cost and smallest form factor.

The RC229ATF/1-55 is a 5.0 volt, low power consumption, lowest cost device intended for desktop applications. The RC229ATF/1-35 is a 5 volt or 3.3 volt, ultra-low power consumption device ideal for low power applications such as portable PCs, pocket modems, PCMCIA cards, and personal digital assistants (PDAs). Table 1 provides a comparison of the basic features of these two devices.

The RC229ATF/1 includes an integrated 74HCT245 transceiver and COM (1-4) Port decoding, which together significantly reduce PCB layout size and complexity.

Data modes, controlled by an industry standard 2400 "AT" command set, can transmit and receive at up to 2400 bps. Fax modes, controlled by a built-in EIA/TIA-578 Class 1 command interface, provide Group 3 transceive functions.

A 60 Character AT command buffer supports full automatic international credit card calling.

Full error correction (V.42 LAPM, MNP2–4) and data compression (V.42 bis, MNP 5) is supported through the Rockwell Protocol Interface (RPI™, patent pending), and host communication software supporting the RPI, a list of which can be obtained from your Rockwell sales representative.

The RC229ATF/1 includes a selectable parallel or serial interface to the host (DTE). When parallel mode is selected, a 16450/16550-compatible interface allows direct connection to a PC-compatible bus without an external UART. The combination of the 16550-compatible interface and 255-byte fax and RPI data buffers provides more reliable performance in a multi-tasking environment.

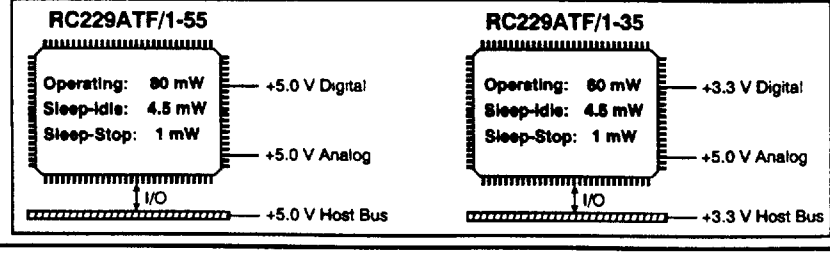
PCMCIA PC Card designs are supported by adding the Rockwell PCMCIA Interface Control Adapter (PICA).

FEATURES

- Data modes
  - CCITT V.22 bis (2400 bps), V.22 (1200 bps), **V.21 (300 bps)**
  - Bell 212A (1200 bps) and 103 (300 bps)
- Group 3 fax modes
  - **V.17 (14400/12000/9600/7200 bps) transmit**
  - **V.29 (9600/7200 bps) transmit and receive**
  - V.27 ter (4800/2400 bps) transmit and receive
  - V.21 Channel 2 (300 bps) transmit and receive
- Enhanced AT commands
- Fax Class 1 commands (EIA/TIA-578)
- **Integrated 16550 UART for operation in multi-tasking operating systems**
- Fax and RPI™ data buffers (in addition to 16-byte 16550 FIFOs): 255 bytes
- **Command buffer: 60 characters**
- **Error Correction (V.42 LAPM, MNP2–4) and Data Compression (V.42 bis, MNP 5)** via RPI™ and host software without additional hardware
- **Fax Error Correction Mode support** (ECM-CCITT T.30 Annex A)
- **High Speed Fax Mode Binary File Transfer support** (BFT-EIA/TIA-614)
- **100-pin plastic quad flat pack (PQFP) package supporting the PCMCIA Type I form factor**
- **Integrated 74HCT245 & COM (1-4) Port decoding**
- Data/fax discrimination and auto answer (+FAA)
- NVRAM interface allows storage of two user configurations and four 36-digit dial strings
- Windows, DOS, and Macintosh software compatible
- Automatic and programmable power down options: Sleep and Stop modes
- Full-duplex data mode test capabilities: analog loop, local digital loop, and remote digital loop
- AT commands for production fax testing and PTT certification
- Extended operating temp. range models available

RPI is a trademark of Rockwell International.

Table 1. RC229ATF/1 Modem Family Comparison



For additional information, see the RC229ATF/1 Designer's Guide (Order No. 879), which provides detailed interface information, and the RC229ATF AT Command Reference Manual (Order No. 888 R1), which provides AT command and S register information.

TECHNICAL SPECIFICATIONS

General

The RC229ATF/1 modem is the full-featured, self-contained data/fax solution shown in Figure 1. No external microcontroller for data or fax control functions is required. Dialing, call progress, and telephone line interface functions are fully supported and controlled through the AT command set.

Data modes perform complete handshake and data rate negotiations. All tone and pattern detection required by the applicable CCITT or Bell standard are supported.

Fax modes support Group 3 fax requirements. Fax data transmission and reception performed by the modem is controlled and monitored through the fax EIA-578 Class 1 command interface. Full HDLC formatting, zero insertion/deletion, and CRC generation/checking is provided.

Both transmit and receive fax data are buffered within the modem. Data transfer to and from the DTE is flow controlled by XON/XOFF.

Configurations and Rates

In data modes with serial interface selected, DTE rate offsets of +1% and −2.5% are accommodated by adding/deleting stop bits as required. In fax modes, the DTE rate is 19200 bps.

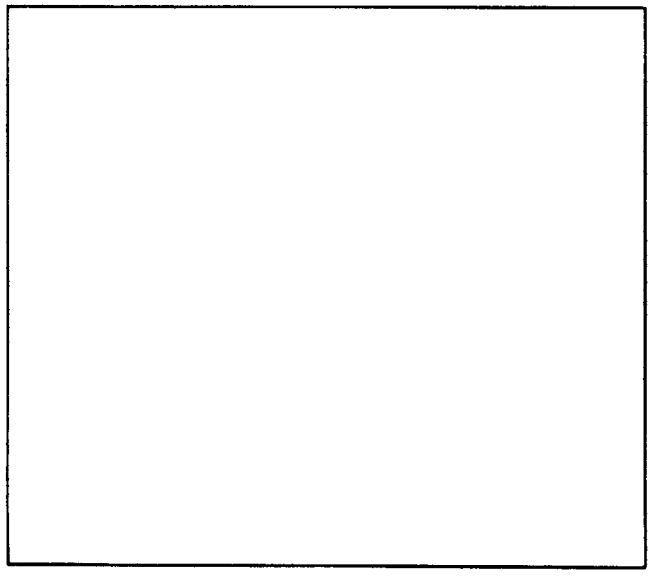


Figure 1. RC229ATF/1 Modem in 100-pin PQFP

Operation

Modem operation is controlled by the AT commands, fax service class 1 commands, and supporting S registers summarized in Tables 1, 2, and 3, respectively. (See the RC229ATF AT Command Reference Manual [Order No. 888 R1] for detailed information.)

Data Modes: Data rate selection is determined by the speed of the originating and answering modems:

Originate Modem Rate (bps)	Connect Speed Based on Answer Modem Rate (bps)		
	300	1200	2400
300	300	300	300
1200	1200	1200	1200
2400	1200	1200	2400

Fax modes: Fax modes are negotiated as defined in T.30, are implemented by AT+F commands, and provide internal data buffering. The AT+FCLASS=0 command causes a transition from fax mode to data mode, and the AT+FCLASS=1 command causes a transition from data mode to fax mode. Most other fax class 1 commands (i.e., AT+F prefixed) are valid only in fax mode. All data commands are valid in fax mode except A/, On, &Tn, and the escape sequence (+++).

Data/Fax Auto Answering

The modem can automatically determine if the incoming call is from a data or fax modem, make the appropriate connection, and inform the DTE of the connection type using the AT+FAA command.

AT Command Format

Each command line must start with the AT prefix and end with a carriage return (CR), and several commands may be included per command line. A command line is $\leq$ 60 characters excluding the CR and AT prefix. A semicolon (;) separator is required between fax commands, while no separator is required between data commands.

AT commands are composed of 10-bit ASCII encoded asynchronous characters. The character format in data mode is 8 data bits with no parity, or 7 data bits with even, odd, or no parity (two stop bits), at a data rate of 19200, 2400, 1200, or 300 bps. The character format in fax mode is 8 data bits with no parity at 19200 bps.

Data Modulation

The data modulation conforms to V.29, V.27 ter, V.22 bis, V.22, V.17, Bell 212A, or Bell 103 depending on the selected configuration. Transmitter and receiver spectrum shaping is provided in accordance with the applicable standard.

Equalization

Automatic adaptive equalization as well as fixed compromised equalization is provided to compensate for line distortions and to minimize the effects of intersymbol interference.

Table 1. "AT" Command Set Summary

Basic Command	Function
AT	Attention Code
A	Answer Command
A/	Repeat Last Command
Bn	Communications Standard Option
C1	Carrier Control Option
D	Dial Command
En	Off-line Character Echo Option
F1	On-line Character Echo Option
Hn	Switch Hook Control Option
In	Identification/Checksum Option
Ln	Speaker Volume Option
Mn	Speaker Control Option
On	On-line Command
P	Pulse Dial
Qn	Result Code Display Option
Sn	Select an S Register
Sn=	Write to an S Register
Sn?	Read an S Register
T	Touch Tone Dial
Vn	Result Code Form Option
Xn	Result Code Set/Call Progress Option
Yn	Long Space Disconnect Option
Zn	Recall Stored Profile Command
+++	Escape Code Sequence
?	Returns Last Addressed S Register
Dial Modifier	**Function**
P	Pulse Dial
R	Originate Call in Answer Mode
S=n	Dial Stored Number (n=0:3)*
T	Touch Tone Dial
W	Wait for Dial Tone
;	Return to Idle State
@	Wait for Quiet Answer Command
!	Flash Hook
,	Pause
0–9, A, B, C,D, #, *	Dial Digits/Characters
& Command	**Function**
&Cn	Data Carrier Detect Option
&Dn	Data Terminal Ready Option
&F	Load Factory Defaults
&Gn	Guard Tone Option
&Jn	Auxiliary Relay Control
&L0	Dial up Line
&M0	Asynchronous Communications Mode
&Pn	Make to Break Ratio Selection
&Q0	Asynchronous Communications Mode
&Sn	Data Set Ready Option
&Tn	Test Command Selection
&V	View Active Configuration and User Profiles
&Wn	Store Active Profile
&X0	Asynchronous Data Transmission
&Yn	Select Stored Profile on Powerup Option
&Zn=x	Store Telephone Number (n=0:3)
% Command	**Function**
%Dn	DTMF Level Attenuation
%Ln	Transmit Level Attenuation
%J	Load Secondary Defaults
%T	DTMF and Calling Tone Diagnostic

Table 2. Fax Command Set Summary

Fax Command	Function
+FCLASS=n	Select Service Class
+F<command>?	Report Active Configuration
+F<command>=?	Report Operating Capabilities
+FAA=n	Data/Fax Auto Answer
+FF	Enhanced Flow Control
+FTS=n	Stop Transmission and Wait
+FRS=n	Receive Silence
+FTM=n	Transmit Data
+FRM=n	Receive Data
+FTH=n	Transmit Data with HDLC Framing
+FRH=n	Receive Data with HDLC Framing
+FRTn	Receive Test Data
+FTTn=m	Transmit Test Data
+Hn	Rockwell Protocol Interface (RPI) Enable

Table 3. S Register Summary

Register	Function
S0*	Ring to Answer On
S1	Ring Count
S2	Escape Code Character
S3	Carriage Return Character
S4	Line Feed Character
S5	Back Space Character
S6	Wait for Dial Tone
S7	Wait Time for Data Carrier
S8	Pause Time for Comma
S9	Carrier Detect Response Time
S10	Lost Carrier to Hang-up Delay
S11	DTMF Dialing Speed
S12	Escape Code Guard Time
S14*	Bit Mapped Options Register
S16	Modem Test Options
S17	Fax Mode Null Byte Timer
S18*	Test Timer
S19	Rockwell Protocol Interface (RPI) Speed
S20	Fax Mode Inactivity Timer
S21*	Bit Mapped Options Register
S22*	Bit Mapped Options Register
S23*	Bit Mapped Options Register
S24	Sleep Mode Inactivity Timer
S25*	Delay to DTR
S26*	RTS to CTS Delay Interval
S27*	Bit Mapped Options Register
S28*	Bit Mapped Options Register

* This S-Register is stored in the modem NVRAM upon receipt of the &W command so that the contents are preserved when modem power is removed.

Scrambler/Descrambler

The modem incorporates a self-synchronizing scrambler/descrambler satisfying the applicable CCITT or Bell requirements.

Transmit Level

The transmit level of –10 dBm ±1 dB (at TIP and RING) is obtained using the circuits shown in Figures 4 and 5.

Transmit Tones

Answer Tone: An answer tone of 2100 Hz (V.22 bis, V.22, or T.30) or 2225 Hz (Bell 212A or 103) is generated.

Guard Tone: An 1800 Hz guard tone can be generated in all data modes.

Calling Tone: A 1100 Hz (0.5 seconds on, 3 seconds off) calling tone (T.30) is generated in the originate fax mode.

Receive Level

The receiver satisfies performance requirements for a received signal from –10 dBm to –43 dBm using the circuit shown in Figure 4. The carrier detect is ON at –43 dBm and OFF at –48 dBm with a minimum of 2 dB hysteresis.

Receiver Tracking

The modem can accommodate carrier frequency offset up to ±7 Hz, and a transmit timing error of ± 0.01% (V.22 bis, V.27 ter, or V.29) or ± 0.02% (V.22 or Bell 212A).

Parallel/Serial Interface Operation

The RC229ATF/1 can be configured to operate with a user selectable 16450 or 16550-compatible parallel interface (hereafter referred to as 16450/550), a V.24 (EIA-232-D) logic-compatible serial interface (RC229ATF/1-55), or an EIA-562 standard serial interface (RC229ATF/1-35). The functional interface signals are shown in Figure 2.

Telephone Line Interface

Telco Interface: Internal differential drivers allow simple connection to the line transformer, requiring only a single line impedance matching resistor.

Relay control: Complete automatic control of the off-hook (OH), talk/data (T/D), and A/A1 relays is provided. Relay drivers allow direct connection to the off-hook and talk/data relays.

DTMF Dialing: Standard DTMF (dual tone multi-frequency) tones (digits 0-9, A, B, C, D, *, and #) or pulses (digits 0-9) can be generated.

Ring Detection: RING signal is detected from valid high-to-low transitions on the RING input line at frequencies of 15.3 Hz to 63 Hz. A RING is valid if the RING ON time is greater than seven cycles of a frequency within this range and is followed by a RING OFF time greater than 500 ms.

NVRAM Interface

A three-line serial interface to an optional user-supplied 1024-bit non-volatile RAM (NVRAM) is provided. The NVRAM can store up to two user-selectable modem configurations as well as four 36-digit dialing strings.

Speaker Interface

A SPKR output is provided with on/off and volume control logic incorporated in the modem, requiring only an external amplifier to drive a loudspeaker.

Low Power Sleep Mode

To conserve power, the RC229ATF/1 has three selectable sleep (power down) modes - Idle, Stop, and Immediate Stop. If enabled by the IDLEN0 and IDLEN1 inputs, the selected sleep mode is entered whenever the modem is inactive. (Please see Table 9.) The sleep mode indicator output, SLEEP, is provided to allow external circuits to be powered down when the modem is in Idle or Stop mode.

The Idle mode allows reduced power consumption with automatic recovery without additional circuitry. If Idle mode is selected, the modem exits Idle mode and returns to full operation whenever a ring signal occurs, the DTE writes to the modem [parallel interface], or TXD is asserted [serial interface].

The Stop mode further reduces power consumption.

Power Requirements and Absolute Maximum Ratings

The power requirements are specified in Table 4, and the absolute maximum ratings are specified in Table 5.

Table 4. Power Requirements

Modem	Mode	Current				Power	
		Typical Current @ T_A = 25°C (mA)		Maximum Current (mA)		Typical Power @T_A = 25°C (mW)	Maximum Power (mW)
RC229ATF/1-55		5.0 VDC[1]		5.25 VDC[1]			
	Normal	16.0		21.0		80.0	110.3
	Sleep	0.9		1.1		4.5	5.8
	Stop[3]	0.2		0.6		1.0	3.2
RC229ATF/1-35		5.0 VDC[2]	3.3 VDC[2]	5.25 VDC[2]	3.6 VDC[2]		
	Normal	6.7	8.1	9.0	14.0	60.0	97.7
	Sleep	0.2	1.0	0.6	1.8	4.5	9.7
	Stop[3]	0.2	0.0	0.6	0.2	1.0	3.9

Test Conditions:

1. RC229ATF/1-55: V_{CC}= 5.0 VDC for typical values and 5.25 VDC for maximum values.
2. RC229ATF/1-35: V_{CC}= 5.0 VDC and 3.3 VDC for typical values, and 5.25 VDC and 3.6 VDC for maximum values.
3. Includes Immediate Sleep-Stop.
4. Values pertain to specified relative humidity of up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
5. A +5VA input voltage ripple of ≤ 0.1 volts peak-to-peak. The amplitude of any frequency in the range 20-150 kHz must be less than 500 microvolts peak.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Limits		Units
		V_{CC} = 5 VDC ± 5%	V_{CC} = 3.3 ± 0.3 VDC	
Supply Voltage	V_{CC}	-0.5 to +6.0	-0.5 to +6.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC} +0.5	-0.5 to V_{CC} +0.5	V
Analog Inputs (Note 2)	V_{IN}	-0.3 to V_{DA} + 0.3	-0.3 to V_{DA} + 0.3	V
Voltage Applied to Outputs in High Z State	V_{HZ}	-0.5 to V_{CC} + 0.5	-0.5 to V_{CC} + 0.5	V
Operating Temperature	T_A			
Commercial:		0 to +70		°C
Industrial:		-40 to +85		°C
Storage Temperature Range	T_{STG}	-55 to +125		°C
DC Input Clamp Current	I_{IK}	±20		mA
DC Output Clamp Current	I_{OK}	±20		mA
Static Discharge Voltage (T_A = 25°C)	V_{ESD}	±2500		V
Latch-up Current (T_A = 25°C)	I_{TRIG}	±400		mA

Notes:

1. Stresses above those listed in this table may cause permanent damage to the product. This is a stress rating only and functional operation of the product at these or other conditions above those indicated in the operation sections of the data sheet is not implied. Exposure to absolute maximum ratings for extended periods may affect product reliability.
2. V_{DA}=5 VDC ± 5% and is the analog power with pin designation +5VA.

HARDWARE INTERFACE

The RC229ATF/1 hardware interface signals are shown for the serial interface in Figure 2a, and for the parallel interface in Figure 2b.

The RC229ATF/1 100-pin PQFP pinout diagrams are given in Figures 3a and 3b for serial and parallel interface implementations, respectively.

RC229ATF/1 100-pin PQFP pin assignments are given in Tables 6a and 6b for serial and parallel interface implementations, respectively.

The RC229ATF/1 digital and analog characteristics are described in Tables 7 and 8, respectively.

The RC229ATF/1 hardware interface signals are described in Table 9.

The parallel interface registers are identified in Table 10.

Schematic designs using the RC229ATF/1-55 implemented with a parallel interface and with a serial interface are shown in Figures 4 and 5, respectively.

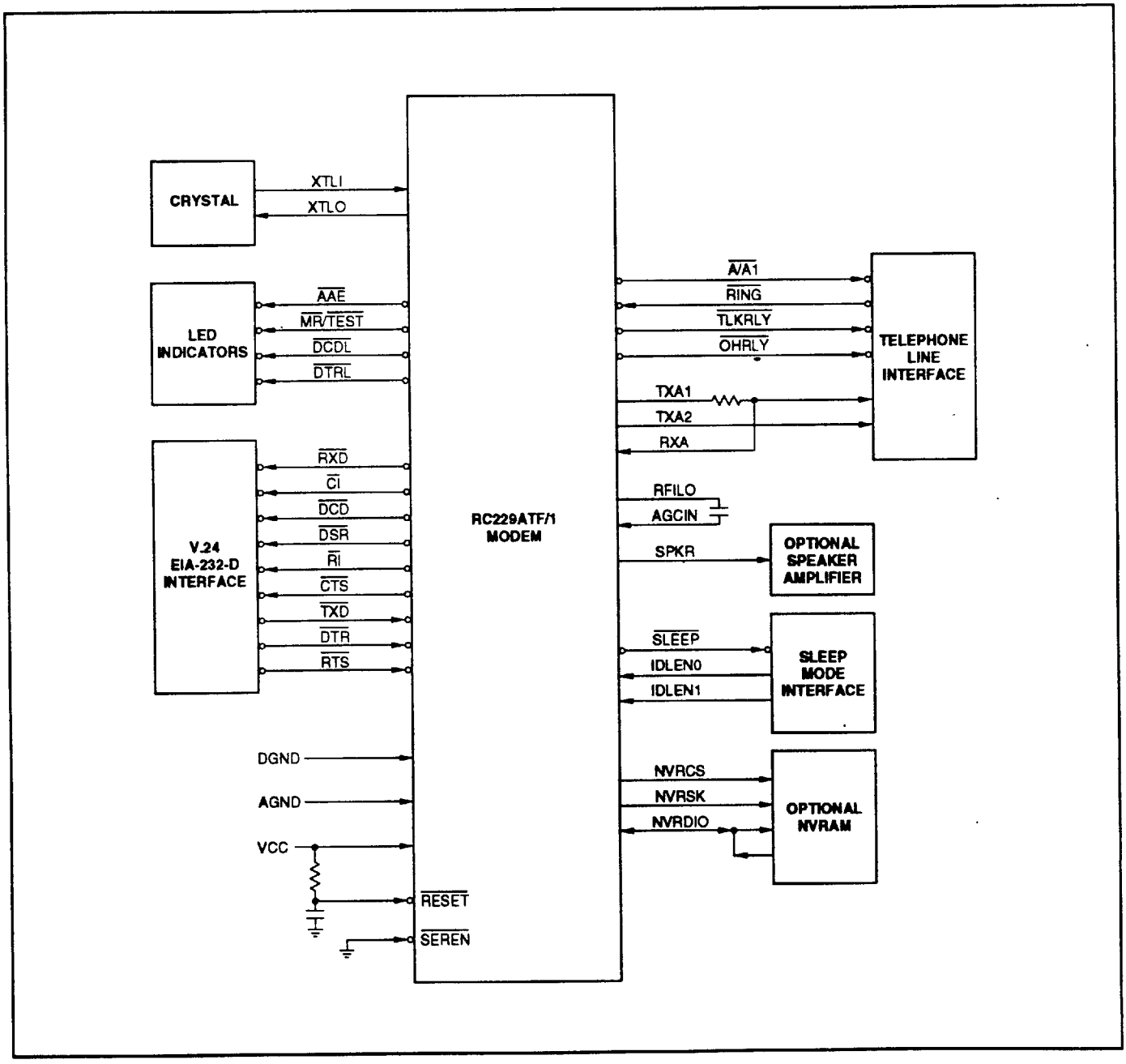


Figure 2a. RC229ATF/1 Hardware Signals - Serial Interface

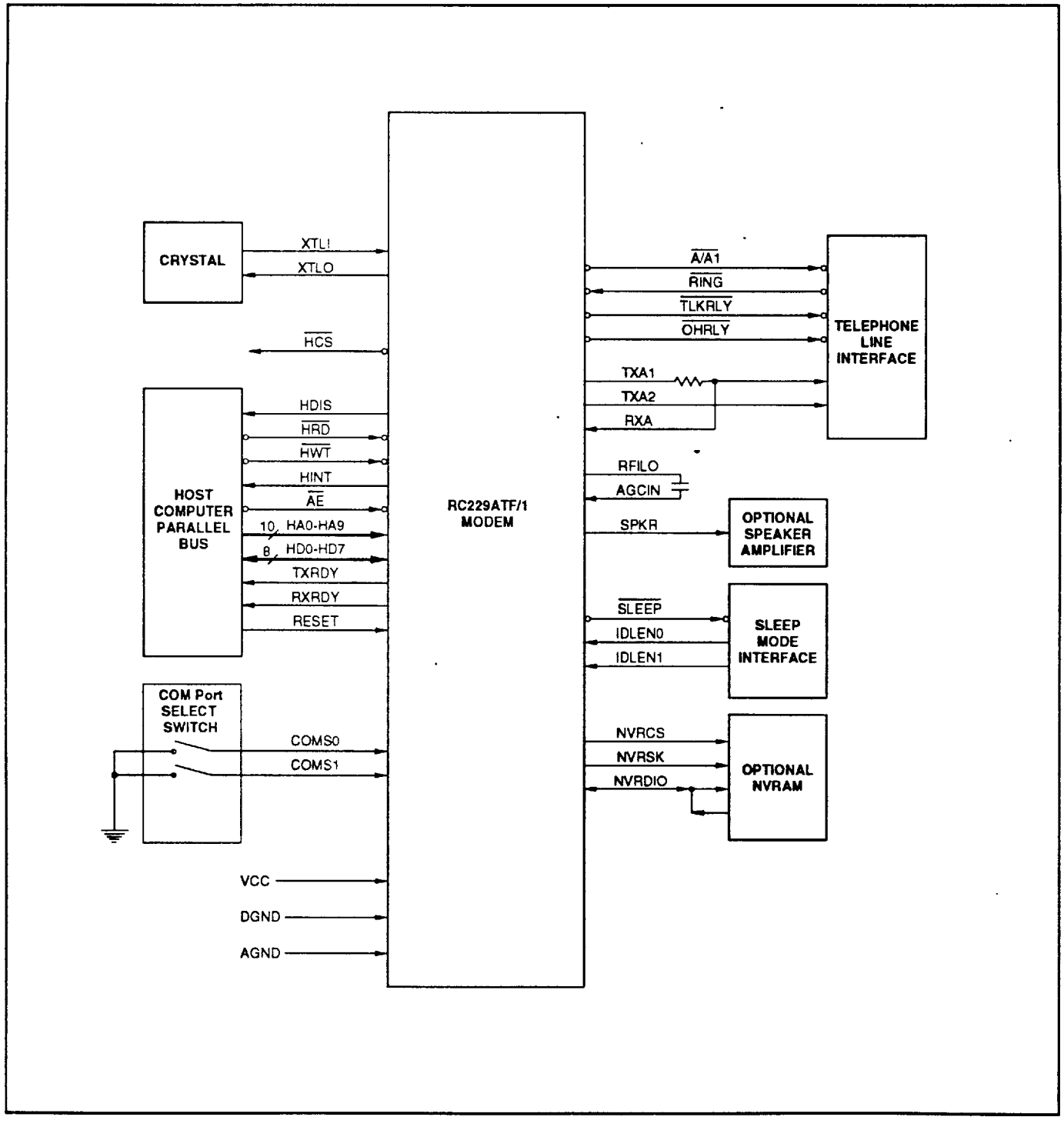


Figure 2b. RC229ATF/1 Hardware Signals - Parallel Interface

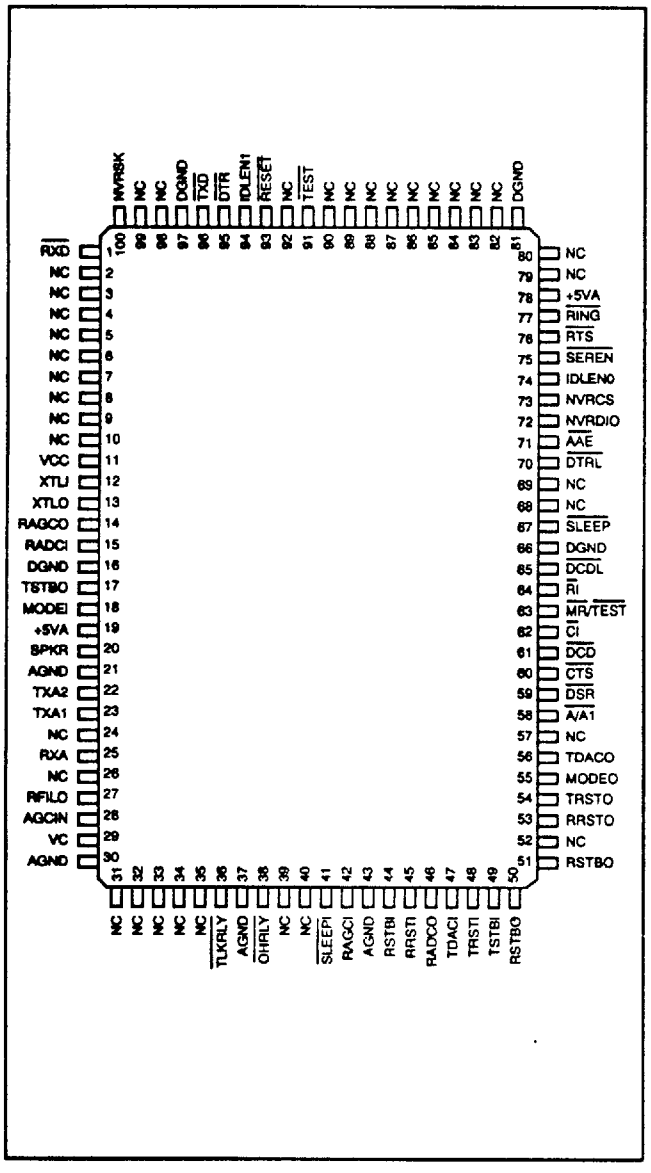


Figure 3a. RC229ATF/1 Pinouts - 100-Pin PQFP - Serial

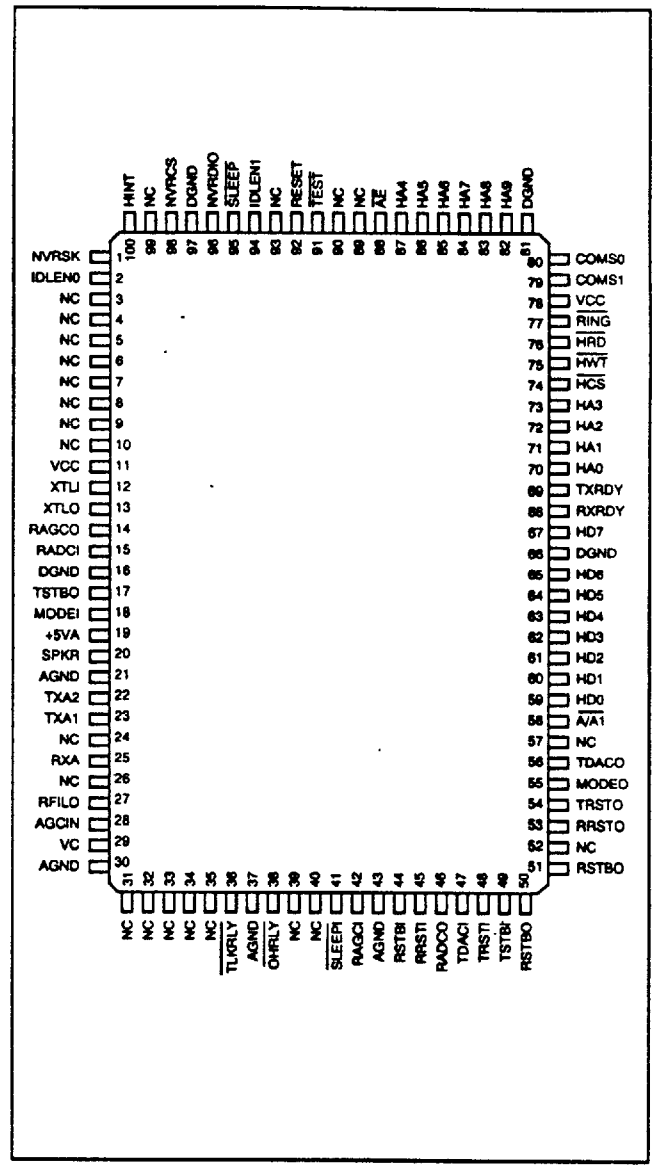


Figure 3b. RC229ATF/1 Pinouts - 100-Pin PQFP - Parallel

Table 6a. RC229ATF/1 PQFP Pin Assignments - Serial

Pin Number	Signal Label	I/O Type	Sleep Mode Signal State[4]
1	RXD	O	High
2	NC	–	–
3	NC	–	–
4	NC	–	–
5	NC	–	–
6	NC	–	–
7	NC	–	–
8	NC	–	–
9	NC	–	–
10	NC	–	–
11	VCC	Note5	Note 5
12	XTLI	I	I
13	XTLO	O	Note 7
14	RAGCO	MI to RAGCI	High
15	RADCI	MI to RADCO	I
16	DGND	DGND	DGND
17	TSTBO	MI to TSTBI	High
18	MODEI	MI to MODEO	I
19	+5VA	VCC	VCC
20	SPKR	O(DF)	Note 8
21	AGND	AGND	AGND
22	TXA2	O(DD)	VC
23	TXA1	O(DD)	VC
24	NC	–	–
25	RXA	I(DA)	I
26	NC	–	–
27	RFILO	–	Note 8
28	AGCIN	–	I
29	VC	–	VC
30	AGND	AGND	AGND
31	NC	–	–
32	NC	–	–
33	NC	–	–
34	NC	–	–
35	NC	–	–
36	TLKRLY	O	High (Inactive)
37	AGND	AGND	AGND
38	OHRLY	O	High (inactive)
39	NC	–	–
40	NC	–	–
41	SLEEPI	I	I
42	RAGCI	MI to RAGCO	I
43	AGND	AGND	AGND
44	RSTBI	MI to RSTBO	I
45	RRSTI	MI to RRSTO	I
46	RADCO	MI to RADCI	Note 9
47	TDACI	MI to TDACO	I
48	TRSTI	MI to TRSTO	I
49	TSTBI	MI to TSTBO	I
50	RSTBO	MI to RSTBI	High
51	RSTBO	MI to RSTBI	High
52	NC	–	–
53	RRSTO	MI to RRSTI	High
54	TRSTO	MI to TRSTI	High
55	MODEO	MI to MODEI	High
56	TDACO	MI to TDACI	High
57	NC	–	–
58	AA1	O	High (inactive)
59	DSR	O	High
60	CTS	O	Low

Table 6a. RC229ATF/1 PQFP Pin Assignments - Serial (Cont'd)

Pin Number	Signal Label	I/O Type	Sleep Mode Signal State[4]
61	DCD	O	High
62	CI	O	High
63	MR/TEST	O	High
64	RI	O	High
65	DCDL	O	High
66	DGND	DGND	DGND
67	SLEEP	O	Low
68	NC	–	–
69	NC	–	–
70	DTRL	O	High
71	AAE	O	High
72	NVRDIO	I/O	High
73	NVRCS	O	Low
74	IDLEN0	I	I
75	SEREN	I	I
76	RTS	I	I
77	RING	I	I
78	VCC	Note 5	Note 5
79	NC	–	–
80	NC	–	–
81	DGND	DGND	DGND
82	NC	–	–
83	NC	–	–
84	NC	–	–
85	NC	–	–
86	NC	–	–
87	NC	–	–
88	NC	–	–
89	NC	–	–
90	NC	–	–
91	TEST	Note 5	Note 5
92	NC	–	–
93	RESET	I	I
94	IDLEN1	I	I
95	DTR	I	I
96	TXD	I	I
97	DGND	DGND	DGND
98	NC	–	–
99	NC	–	–
100	NVRSK	O	High

Notes:

1. MI = Modem Interconnection.
2. NC = No connection (may have internal connection; leave pin disconnected (open)).
3. I/O types are described in Tables 7 (digital signals) and Table 8 (analog signals). I = input and O = output.
4. Indicated signal states apply to both Sleep-Idle mode and Sleep Stop mode, except where specifically noted.
5. Connect to VCC.
6. AGND is analog ground and DGND is digital ground.
7. This signal is oscillating normally in Sleep-Idle mode, and is High in Sleep-Stop mode.
8. Analog signal (0 to +5 VDC).
9. May be High or Low.

Table 6b. RC229ATF/1 PQFP Pin Assignments - Parallel

Pin Number	Signal Label	I/O Type	Sleep Mode Signal State[4]
1	NVRSK	O	High
2	IDLEN0	I	I
3	NC	–	–
4	NC	–	–
5	NC	–	–
6	NC	–	–
7	NC	–	–
8	NC	–	–
9	NC	–	–
10	NC	–	–
11	VCC	Note 5	Note 5
12	XTLI	I	I
13	XTLO	O	Note 7
14	RAGCO	MI to RAGCI	High
15	RADCI	MI to RADCO	I
16	DGND	DGND	DGND
17	TSTBO	MI to TSTBI	High
18	MODEI	MI to MODEO	I
19	+5VA	VCC	VCC
20	SPKR	O(DF)	Note 8
21	AGND	AGND	AGND
22	TXA2	O(DD)	VC
23	TXA1	O(DD)	VC
24	NC	–	–
25	RXA	I(DA)	I
26	NC	–	–
27	RFILO	–	Note 8
28	AGCIN	–	I
29	VC	–	VC
30	AGND	AGND	AGND
31	NC	–	–
32	NC	–	–
33	NC	–	–
34	NC	–	–
35	NC	–	–
36	$\overline{\text{TLKRLY}}$	O	High (inactive)
37	AGND	AGND	AGND
38	$\overline{\text{OHRLY}}$	O	High (inactive)
39	NC	–	–
40	NC	–	–
41	$\overline{\text{SLEEPI}}$	I	I
42	RAGCI	MI to RAGCO	I
43	AGND	AGND	AGND
44	RSTBI	MI to RSTBO	I
45	RRSTI	MI to RRSTO	I
46	RADCO	MI to RADCI	Note 9
47	TDACI	MI to TDACO	I
48	TRSTI	MI to TRSTO	I
49	TSTBI	MI to TSTBO	I
50	RSTBO	MI to RSTBI	High
51	RSTBO	MI to RSTBI	High
52	NC	–	–
53	RRSTO	MI to RRSTI	High
54	TRSTO	MI to TRSTI	High
55	MODEO	MI to MODEI	High
56	TDACO	MI to TDACI	High
57	NC	–	–
58	$\overline{\text{AVA1}}$	O	High (inactive)
59	HD0	I/O	High
60	HD1	I/O	High

Table 6b. RC229ATF/1 PQFP Pin Assign. - Parallel (Cont'd)

Pin Number	Signal Label	I/O Type	Sleep Mode Signal State[4]
61	HD2	I/O	High
62	HD3	I/O	High
63	HD4	I/O	High
64	HD5	I/O	High
65	HD6	I/O	High
66	DGND	DGND	DGND
67	HD7	I/O	High
68	RXRDY	O	Low
69	TXRDY	O	Low
70	HA0	I	I
71	HA1	I	I
72	HA2	I	I
73	HA3	I	I
74	$\overline{\text{HCS}}$	O	High
75	$\overline{\text{HWT}}$	I	I
76	$\overline{\text{HRD}}$	I	I
77	$\overline{\text{RING}}$	I	I
78	VCC	Note 5	Note 5
79	COMS1	I	I
80	COMS0	I	I
81	DGND	DGND	DGND
82	HA9	I	I
83	HA8	I	I
84	HA7	I	I
85	HA6	I	I
86	HA5	I	I
87	HA4	I	I
88	$\overline{\text{AE}}$	I	I
89	NC	–	–
90	NC	–	–
91	$\overline{\text{TEST}}$	Note 5	Note 5
92	RESET	I	I
93	NC	–	–
94	IDLEN1	I	I
95	$\overline{\text{SLEEP}}$	O	Low
96	NVRDIO	I/O	High
97	DGND	DGND	DGND
98	NVRCS	O	Low
99	NC	–	–
100	HINT	O	High

Notes:

1. MI = Modem Interconnection.
2. NC = No connection (may have internal connection; leave pin disconnected (open)).
3. I/O types are described in Tables 7 (digital signals) and Table 8 (analog signals). I = input and O = output.
4. Indicated signal states apply to both Sleep-Idle mode and Sleep Stop mode, except where specifically noted.
5. Connect to VCC.
6. AGND is analog ground and DGND is digital ground.
7. This signal is oscillating normally in Sleep-Idle mode, and is High in Sleep-Stop mode.
8. Analog signal (0 to +5 VDC).
9. May be High or Low.

Table 7a. VCC = 5 V +/-5% Digital I/F Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage	V_{IH}					
TTL		2.0	–	V_{CC} + 0.3	V	
CMOS		0.7 V_{CC}	–	V_{CC} + 0.3	V	
RESET, $\overline{RESET}$, $\overline{TEST}$		0.7 V_{CC}	–	V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}					
TTL		–0.3	–	0.8	V	
CMOS		–0.3	–	0.3 V_{CC}	V	
RESET, $\overline{RESET}$, $\overline{TEST}$		–0.3	–	0.8	V	
Output Voltages						
Output High Voltage	V_{OH}	2.4	–	–	V	I_{LOAD} = -100 µA
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{LOAD} = 1.6 mA
3-State Output Hi-Z Current	I_{OZ}	–	–	±10	µA	V_{IN} = 0 V to V_{CC}
Input Leakage Current	I_I					
$\overline{HWT}$, $\overline{HRD}$, $\overline{RING}$, $\overline{SEREN}$, $\overline{RTS}$		–	–	±2.5	µA	V_{IN} = 0 V to V_{CC}
$\overline{XTLI}$		–	–	±10	µA	V_{IN} = 0 V to V_{CC}
$\overline{RESET}$, $\overline{TEST}$, COMS0, COMS1		15	–	100	µA	V_{IN} = 0 V
		–	–	–2.5	µA	V_{IN} = V_{CC}
$\overline{RESET}$		–15	–	–100	µA	V_{IN} = V_{CC}
		–	–	2.5	µA	V_{IN} = 0 V

Note V_{CC} = 5 V ± 5%, T_A = 0°C to 70°C

Table 7b. VCC = 3.3 V +/- 0.3 V Digital I/F Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage	V_{IH}	2.0	–	V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	–0 3	–	0.8	V	
Output Voltages						
Output High Voltage	V_{OH}	2 4	–	–	V	I_{LOAD} = -100 µA
Output Low Voltage	V_{OL}	–	–	0 4	V	I_{LOAD} = 1.6 mA
3-State Output Hi-Z Current	I_{OZ}	–	–	±8	µA	V_{IN} = 0 V to V_{CC}
Input Leakage Current	I_I					
$\overline{HWT}$, $\overline{HRD}$, $\overline{RING}$, $\overline{SEREN}$, $\overline{RTS}$		–	–	±2 0	µA	V_{IN} = 0 V to V_{CC}
$\overline{XTLI}$		–	–	±8	µA	V_{IN} = 0 V to V_{CC}
$\overline{RESET}$, $\overline{TEST}$, COMS0, COMS1		7	–	50	µA	V_{IN} = 0 V
		–	–	–2.0	µA	V_{IN} = V_{CC}
$\overline{RESET}$		–7	–	–50	µA	V_{IN} = V_{CC}
		–	–	2.0	µA	V_{IN} = 0 V

Note V_{CC} = 3.3 V ± 0.3 V, T_A = 0°C to 70°C

Table 8. Analog Interface Characteristics

Name	Type	Characteristic	
RXA	I (DA)	Input Impedance:	> 50K-ohms
		Voltage Range:	2.5 ± 1.6 V
TXA1, TXA2	O (DD)	Minimum Load:	300 ohms
		Maximum Capacitive Load:	0.01µF
		Output Impedance:	10 ohms
		Output Voltage:	2.5 ± 1.6 V
		D.C. Offset:	< 200 mV[1]
SPKR	O (DF)	Minimum Load:	300 ohms
		Maximum Capacitive Load:	0.01 µF
		Output Impedance:	10 ohms
		Output Voltage:	2.5 ± 1.6 V
		D.C. Offset:	< 20 mV[1]

Note: 1 With reference to VC (2.5 V nominal).

Table 9. Hardware Interface Signal Definitions

Label	I/O Type	Signal Name/Description
		SYSTEM SIGNALS
XTLI XTLO	I O	**Crystal/Clock In and Crystal Out.** The modem must be connected to an external crystal circuit consisting of a crystal and two capacitors and a 100 ohm resistor. Alternatively, XTLI may be driven with a buffered clock; in this case, XTLO should be left open.
$\overline{\text{RESET}}$ RESET	I	**Reset.** The active low $\overline{\text{RESET}}$ input for serial interface, or active high RESET input for parallel interface, resets the internal modem logic. Upon $\overline{\text{RESET}}$ (RESET) transitioning from high to low (low to high), modem operation returns to the state controlled by factory default values and stored values in NVRAM. During modem power turn-on, $\overline{\text{RESET}}$ (RESET) must be held low (high) for at least 5 ms after the VCC and +5VA operating voltage is attained for the modem to stabilize. When the serial interface is selected, $\overline{\text{RESET}}$ can be connected to an external RC network to cause the modem to reset upon power turn on. When the parallel interface is selected, RESET should be connected to the host bus reset line.
$\overline{\text{SEREN}}$	I	**Serial Interface Enable.** When the $\overline{\text{SEREN}}$ input is low, serial interface is selected upon reset. In this case, the serial interface signals should be connected to the V.24 interface (EIA-232-D for the RC229ATF/1-55, and EIA-562 for the RC229ATF/1-35) and LED indicators as shown in Figures 2.
+5VA	PWR	**+ 5V Analog Supply.** +5V ±5% is required.
VCC	PWR	**Digital Power Supply.** +3.3V ± 0.3 V (RC229ATF/1-35) [JEDEC 8-1A (3.3V TTL compatible)] or +5V ±5% (RC229ATF/1-55) is required.
DGND AGND	GND	**Digital and Analog Grounds.**
		SLEEP MODE SIGNALS
IDLEN0 IDLEN1	I I	**Idle Enable 0 and Idle Enable 1.** Encoded inputs enable or disable the sleep modes as given below. IDLEN0 and IDLEN1 must be tied either to ground or to VCC through a 20K-ohm resistor. **IDLEN1 IDLEN0 Mode** H H Sleep mode disabled H L Sleep-Idle mode enabled L H Sleep-Stop mode enabled L L Immediate Sleep-Stop mode enabled If the Idle option is enabled, the modem will enter Sleep-Idle mode after the inactivity duration determined by the S24 register (where the S24 default is 5 seconds). The modem will wake-up upon DTE activity (i.e., $\overline{\text{TXD}}$ or $\overline{\text{DTR}}$ activity in serial mode, or a write to the UART in parallel mode), or ring activity. If the Stop option is selected, the modem will enter Sleep-Stop mode after the inactivity duration determined by the S24 register (where the S24 default is 5 seconds). The modem will wake-up upon DTE activity [i.e., $\overline{\text{DTR}}$ or $\overline{\text{TXD}}$ activity in serial mode (note that the first character is not recognized), or a write to the UART in parallel mode], or ring activity. For PCMCIA applications, Immediate Sleep-Stop mode is entered after Power On Reset (POR). Normal Sleep-Stop mode operation commences after the first wake-up, which follows the same wake-up procedure as Sleep-Stop mode.
$\overline{\text{SLEEP}}$	O	**Sleep Mode.** $\overline{\text{SLEEP}}$ output high indicates the modem is operating in its normal mode. $\overline{\text{SLEEP}}$ low indicates that the modem is in the sleep mode. The $\overline{\text{SLEEP}}$ output can also be used to control power to other devices.
$\overline{\text{SLEEPI}}$	I	**Sleep Mode IA.** $\overline{\text{SLEEP}}$ input low causes the integrated Analog (IA) to enter low power sleep mode.

Table 9. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		NVRAM INTERFACE
NVRCS	O	**NVRAM Chip Select.** NVRCS output high enables the NVRAM.
NVRSK	O	**NVRAM Shift Clock.** The NVRSK output is used to shift data to or from the NVRAM.
NVRDIO	I/O	**NVRAM Data In/NVRAM Data Out.** NVRDIO is a bidirectional signal that carries both the serial input data from the NVRAM and the serial output data to the NVRAM. Depending on the specific NVRAM used, a resistor may be required between the NVRAM DO output pin and the modem NVRDIO bidirectional line. (Refer to the NVRAM data sheet). NVRDIO must be connected to VCC through a 4.7k ohm resistor if NVRAM is not used.
		SPEAKER INTERFACE
SPKR	O(DF)	**Speaker Analog Output.** The SPKR output reflects the output of the receive analog signal. The SPKR output is turned on or off by the Speaker Control Option (Mn command) and the gain is controlled by the Speaker Volume Option (Ln command). When the speaker is turned off, the SPKR output is clamped to the voltage at the VC pin. The SPKR output can drive a load as low as 300 ohms. Typically, the SPKR output is an input to an external LM386 audio power amplifier.
		ASYNCHRONOUS SERIAL INTERFACE (SERIAL INTERFACE ONLY; $\overline{\text{SEREN}}$ = LOW)
$\overline{\text{RXD}}$	O	**Received Data.** The modem presents received serial data to the $\overline{\text{RXD}}$ output pin.
$\overline{\text{TXD}}$	I	**Transmitted Data.** The modem obtains serial data to be transmitted from the $\overline{\text{TXD}}$ input pin.
$\overline{\text{DTR}}$	I	**Data Terminal Ready.** $\overline{\text{DTR}}$ input ON (low) indicates that the DTE is ready to operate. $\overline{\text{DTR}}$ input OFF (high) indicates that the DTE is not ready to operate.
$\overline{\text{CTS}}$	O	**Clear To Send.** In data modes, the $\overline{\text{CTS}}$ output is ON, even in sleep and stop modes. In fax modes, $\overline{\text{CTS}}$ is optionally used for flow control.
$\overline{\text{DSR}}$	O	**Data Set Ready.** The $\overline{\text{DSR}}$ output is controlled by the AT&Sn command.
$\overline{\text{DCD}}$	O	**Data Carrier Detected.** The $\overline{\text{DCD}}$ output is controlled by the AT&C command.
$\overline{\text{CI}}$	O	**Calling Indicator.** $\overline{\text{CI}}$ output ON (low) indicates modem connection at 2400 bps.
$\overline{\text{RI}}$	O	**Ring Indicator.** $\overline{\text{RI}}$ output ON (low) indicates the presence of an ON segment of a ring signal on the telephone line. (The ring signal cycle is typically two seconds ON, four seconds OFF.) The OFF (high) condition of the $\overline{\text{RI}}$ output is maintained during the OFF segment of the ring cycle (between rings) and at all other times when ringing is not being received.
$\overline{\text{RTS}}$	I	**Request to Send.** Reserved.
		SERIAL INDICATOR INTERFACE (SERIAL INTERFACE ONLY; $\overline{\text{SEREN}}$ = LOW)
$\overline{\text{AAE}}$	O	**Auto Answer Enable.** $\overline{\text{AAE}}$ output ON (low) indicates that modem auto answer mode has been enabled with the S0 = command. $\overline{\text{AAE}}$ high indicates auto answer has been disabled. The $\overline{\text{AAE}}$ output also indicates the status of the $\overline{\text{RI}}$ output.
$\overline{\text{MR/TEST}}$	O	**Modem Ready.** $\overline{\text{MR/TEST}}$ output ON (low) indicates that the modem is ready (i.e., modem power is on and a test mode is not selected). In a test mode, the $\overline{\text{MR/TEST}}$ output pulses to indicate a test is in process.
$\overline{\text{DCDL}}$	O	**DCD Indicator.** The $\overline{\text{DCDL}}$ output is controlled by the AT&C command.
$\overline{\text{DTRL}}$	O	**DTR Indicator.** The $\overline{\text{DTRL}}$ output is controlled by the AT&D command.

Table 9. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		PARALLEL HOST INTERFACE (PARALLEL INTERFACE ONLY)
		(See Figure 2b.)
		When the $\overline{HWT}$ input signal is connected to the host bus write line, the parallel interface is selected upon reset. (See Order No. 879, the RC229ATF/1 Designer's Guide, for waveform and timing information.)
		The parallel interface user selectably emulates either a 16450 or 16550 UART. Table 10 identifies the parallel interface registers. Parallel interface operation is equivalent to 16450/550 operation with CS0 and CS1 inputs high, and DISTR and DOSTR inputs low. The corresponding RC229ATF/1 modem and 16450/550 signals are shown below. 16450/550 signals not required for RC229ATF/1 modem family host computer operation are not shown.

16450/550 Signal	RC229ATF/1 Signal
A0 - A2	HA0 - HA2
D0 - D7	HD0 - HD7
MR	$\overline{RESET}$ (Active low)
ADS	$\overline{AE}$
$\overline{DISTR}$	$\overline{HWT}$
$\overline{DOSTR}$	$\overline{HRD}$
INTRPT	HINT
$\overline{DDIS}$	HDIS
OUT2	None (Implemented internally in the RC229ATF/1)
TXRDX	TXRDY
RXRDX	RXRDY

HA0-HA9 (I) — **Host Bus Address Lines 0-9.** During a host read or write operation, HA0-HA2 select an internal register. The state of the divisor latch access bit (DLAB) affects the selection of certain registers. The register addresses are:

DLAB	HA2	HA1	HA0	Register
0	0	0	0	Receiver Buffer Register (Read)
0	0	0	0	Transmitter Holding Register (Write)
0	0	0	1	Interrupt Enable Register
X	0	1	0	Interrupt Identification Register (Read Only)
X	0	1	1	Line Control Register
X	1	0	0	Modem Control Register
X	1	0	1	Line Status Register (Read Only)
X	1	1	0	Modem Status Register (Read Only)
X	1	1	1	Scratch Register
1	0	0	0	Divisor Latch Register (Least Significant Byte)
1	0	0	1	Divisor Latch Register (Most Significant Byte)

HD0-HD7 (I/O) — **Host Bus Data Lines 0-7.** HD0-HD7 are comprised of eight tri-state input/output lines providing bidirectional communication between the host and the modem. Data, control words, and status information are transferred through HD0-HD7. (See Table 10.) No transceiver is required for 74HCT245 compatibility.

$\overline{HCS}$ (O) — **Host Bus Chip Select.** $\overline{HCS}$ output low enables reading from or writing to the modem using the parallel bus.

$\overline{HRD}$ (I) — **Host Bus Read.** $\overline{HRD}$ is an active low read control input. When the modem is selected with $\overline{HCS}$ low, $\overline{HRD}$ low allows status or data words to be read from an addressed register.

$\overline{HWT}$ (I) — **Host Bus Write.** $\overline{HWT}$ is an active low write control input. When the modem is selected with $\overline{HCS}$ low, $\overline{HWT}$ low allows data or control words to be written to an addressed register.

Table 9. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		PARALLEL HOST INTERFACE (PARALLEL INTERFACE ONLY) [Continued]
HINT	O	**Host Bus Interrupt.** HINT is a 16450/550-compatible output indicating interrupt status and is enabled by the OUT2 bit set to a 1 in the Modem Control Register (MCR).
COMS0-1	I	**COM Port Address Inputs 0-1.** These two inputs provide COM port addressing of the internal 16550 interface as shown in the following table:

COMS0	COMS1	Host I/O Address	COM Port Selected
0	0	2E8h	4
0	1	3E8h	3
1	0	2F8h	2
1	1	3F8h	1

RXRDY	O	**Ready to Receive.** RXRDY is a 16550-compatible DMA output that is set when the modem is ready to receive data from the host.
TXRDY	O	**Ready to Transmit.** TXRDY is a 16550-compatible DMA output that is set when the modem is ready to send data to the host.
		TELEPHONE LINE INTERFACE
TXA1 TXA2	O(DF)	**Transmit Analog 1 and 2.** TXA1 and TXA2 are differential outputs. A 600 ohm telephone coupling transformer may be driven directly without the need for external discrete buffer amplifiers. Both TXA1 and TXA2 outputs are turned off when the transmitter is disabled or during local analog loopback.
RXA	I(DA)	**Receive Analog.** RXA is a single-ended receive data input from the telephone line interface.
VC	O	**Centerpoint Voltage.** A +2.5 VDC centerpoint voltage derived from an internal reference voltage. The TXA1 and TXA2 outputs are biased at VC.
$\overline{\text{TLKRLY}}$	O	**Talk/Data Relay Driver.** $\overline{\text{TLKRLY}}$ is an open drain output which can directly drive a relay with greater than 360 Ω coil resistance and having a "must operate " voltage of no greater than 4.0 VDC. A heavier load, such as a electro-mechanical relay, requires the use of an external transistor. An external diode should be provided across the relay coil. The $\overline{\text{TLKRLY}}$ output is clamped off during power-on reset or the sleep mode. The $\overline{\text{TLKRLY}}$ output is activated and deactivated at the same time as the $\overline{\text{OHRLY}}$ output. In a typical application, $\overline{\text{TLKRLY}}$ ON opens the normally closed Talk/Data (T/D) relay and disconnects the handset from the telephone line.
$\overline{\text{OHRLY}}$	O	**Off-Hook Relay Driver.** $\overline{\text{OHRLY}}$ is an open drain output which can directly drive a relay with greater than 360 Ω coil resistance and having a "must operate " voltage of no greater than 4.0 VDC. A heavier load, such as a electro-mechanical relay, requires the use of an external transistor. An external diode should be provided across the relay coil. The $\overline{\text{OHRLY}}$ output is clamped off during power-on reset or the sleep mode. In a typical application, $\overline{\text{OHRLY}}$ ON closes the normally open Off-Hook (OH) relay and connects the modem to the telephone line (off-hook).
$\overline{\text{RING}}$	I	**Ring Detector.** $\overline{\text{RING}}$ is a TTL-compatible input used by the modem to detect a 15.3 Hz to 63 Hz ringing signal. A low-going edge on the $\overline{\text{RING}}$ input also removes the modem from the sleep mode.
$\overline{\text{A/A1}}$	O	**Key Telephone Hold Indicator.** $\overline{\text{A/A1}}$ output low indicates that the telephone line is in use when used on multi-line key telephones.

Table 9. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		MODEM INTERCONNECT
RFILO	MI	**Receive Filter Output.** RFILO is the output of the internal receive bandsplit filter which must be connected to AGCIN through a 0.1 µF, 20%, DC decoupling capacitor. The 1000 pF capacitor to ground provides noise immunity at low signal levels.
AGCIN	MI	**Receive AGC Gain Amplifier Input.** See RFILO.
MODEO (DSP), MODEI (IA)	MI	**Mode Control.** Direct modem interconnect line.
TDACO (DSP), TDACI (IA)	MI	**Transmitter DAC Signal.** Serial digital DAC signal. Direct modem interconnect line.
TSTBO (DSP), TSTBI (IA)	MI	**Transmitter Strobe.** 576 kHz digital transmitter timing reference. Direct modem interconnect line.
TRSTO (DSP), TRSTI (IA)	MI	**Transmitter Reset.** 9.6 kHz, 7.5 kHz, or 7.2 kHz digital transmitter timing reference. Direct modem interconnect line. Direct modem interconnect line.
RADCI (DSP), RADCO (IA)	MI	**Receiver ADC Signal.** Serial digital ADC signal. Direct modem interconnect line.
RAGCO (DSP), RAGCI (IA)	MI	**Receiver AGC Signal.** Serial digital AGC signal. Direct modem interconnect line.
RRSTO (DSP), RRSTI (IA)	MI	**Receiver Reset.** 9.6 kHz, 7.5 kHz, or 7.2 kHz digital receiver timing reference. Direct modem interconnect line.
RSTBO (DSP), RSTBI (IA)	MI	**Receiver Strobe.** 576 kHz digital receiver timing reference. Direct modem interconnect line.

Table 10. Parallel Interface Registers

Register No.	Register Name	Bit No. 7	6	5	4	3	2	1	0
7	Scratch Register (SCR)	Scratch Register							
6	Modem Status Register (MSR)	Data Carrier Detect (DCD)	Ring Indicator (RI)	Data Set Ready (DSR)	Clear to Send (CTS)	Delta Data Carrier Detect (DDCD)	Trailing Edge Ring Indicator (TERI)	Delta Data Set Ready (DDSR)	Delta Clear to Send (DCTS)
5	Line Status Register (LSR)	Error in Receiver FIFO (Note 2)	Transmitter Empty (TEMT)	Transmitter Holding Register (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	Data Ready (DR)
4	Modem Control Register (MCR)	0	0	0	Local Loopback	Out 2	Out 1	Request to Send (RTS)	Data Terminal Ready (DTR)
3	Line Control Register (LCR)	Divisor Latch Access Bit (DLAB)	Set Break	Stick Parity	Even Parity Select (EPS)	Parity Enable (PEN)	Number of Stop Bits (STB)	Word Length Select Bit 1 (WLS1)	Word Length Select Bit 0 (WLS0)
2	FIFO Control Register (FCR) (Write Only)	Receiver Trigger (MSB)	Receiver Trigger (LSB)	–	–	DMA Mode Select	Transmitter FIFO Reset	Receiver FIFO Reset	FIFO Enable
2	Interrupt Identify Register (IIR) (Read Only)	FIFOs Enabled (Note 2)	FIFOs Enabled (Note 2)	0	0	Interrupt ID Bit 2 (Note 2)	Interrupt ID Bit 1	Interrupt ID Bit 0	"0" if Interrupt Pending
1 DLAB = 0	Interrupt Enable Register (IER)	0	0	0	0	Enable Modem Status Interrupt (EDSSI)	Enable Receiver Line Status Interrupt (ELSI)	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Enable Received Data Available Interrupt (ERBFI)
0 DLAB = 0	Transmitter Holding Register (THR)	Transmitter Holding Register (Write Only) (Note 1)							
0 DLAB = 0	Receiver Buffer Register (RBR)	Receiver Buffer Register (Read Only) (Note 1)							
1 DLAB = 1	Divisor Latch (MSB) Register (DLM)	Divisor Latch (MS)							
0 DLAB = 1	Divisor Latch (LSB) Register (DLL)	Divisor Latch (LS)							

Note 1: **Bit 0 is the least significant bit. It is the first bit serially transmitted or received.**
Note 2: **These bits are always 0 in the user-selected 16450-compatible interface mode.**

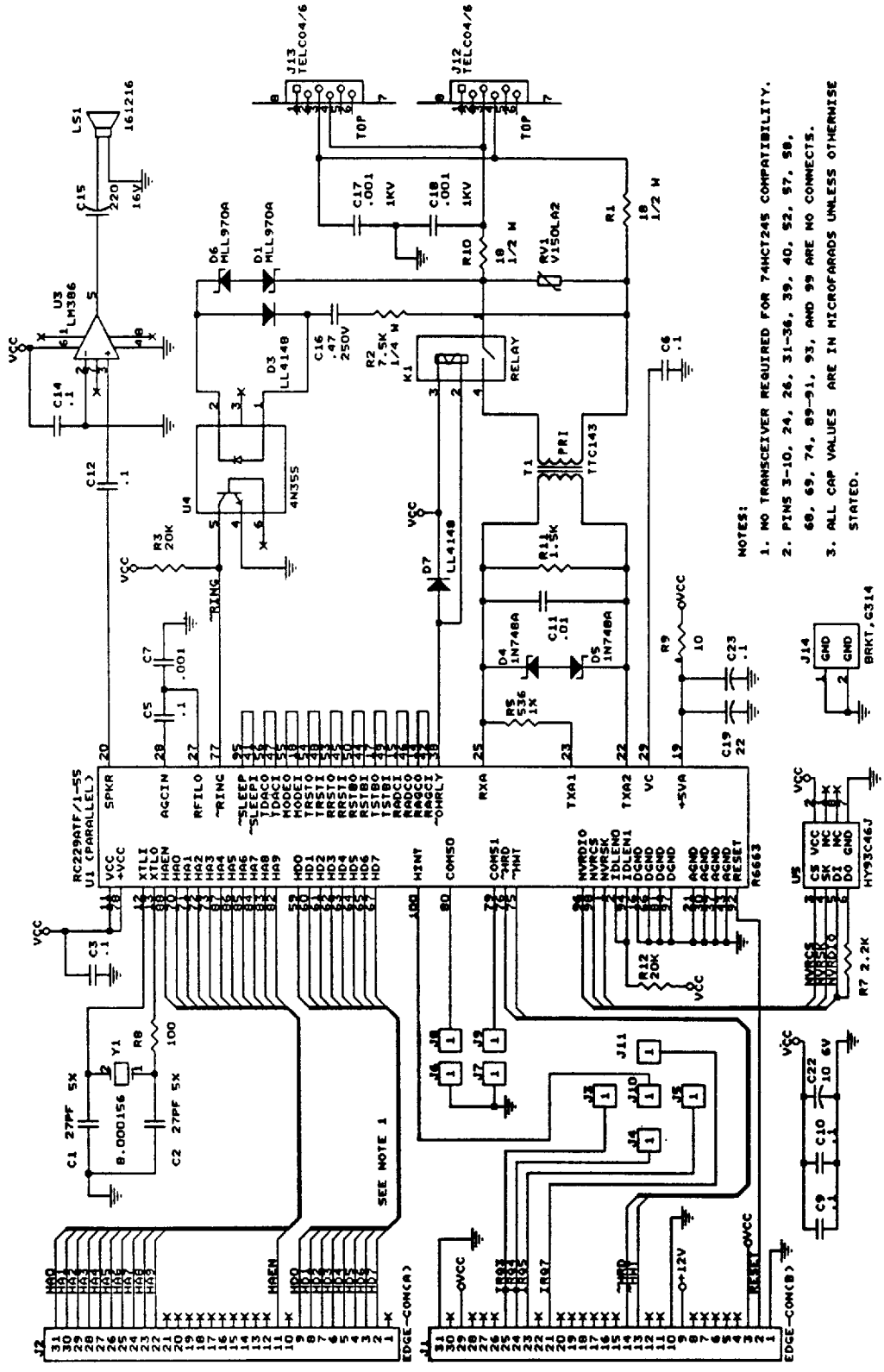


Figure 4. RC229ATF/1-55 Design Schematic - Parallel

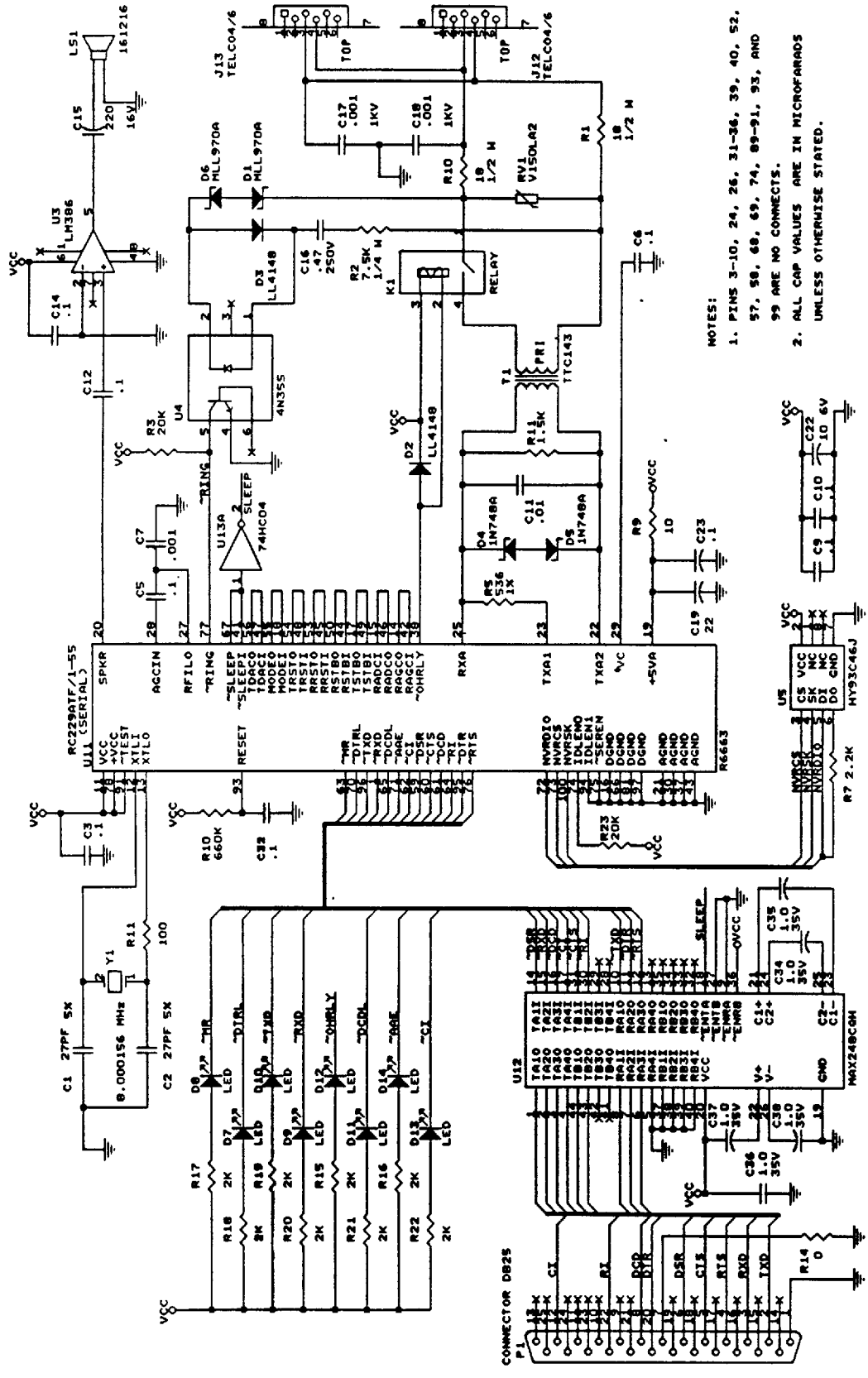


Figure 5. RC229ATF/1-55 Design Schematic - Serial