LXP2175

T1/E1 Elastic Store

General Description

The LXP2175 is one of a family of Level One Primary Rate Interface solutions. It is compatible with LXT30x series transceivers, and LXP2180A/2181A framer/formatters. The LXP2175 is a low-power CMOS elastic-store memory optimized for use in primary rate telecommunications transmission equipment.

Compatible with North American T1 (1.544 MHz) and European E1 (2.048 MHz) primary rate networks, the device serves as a synchronous element between asynchronous data streams. The LXP2175 has several flexible operating modes which eliminate support logic and hardware otherwise required to interconnect parallel or serial TDM backplanes. The LXP2175 is a drop-in replacement for the DS2175.

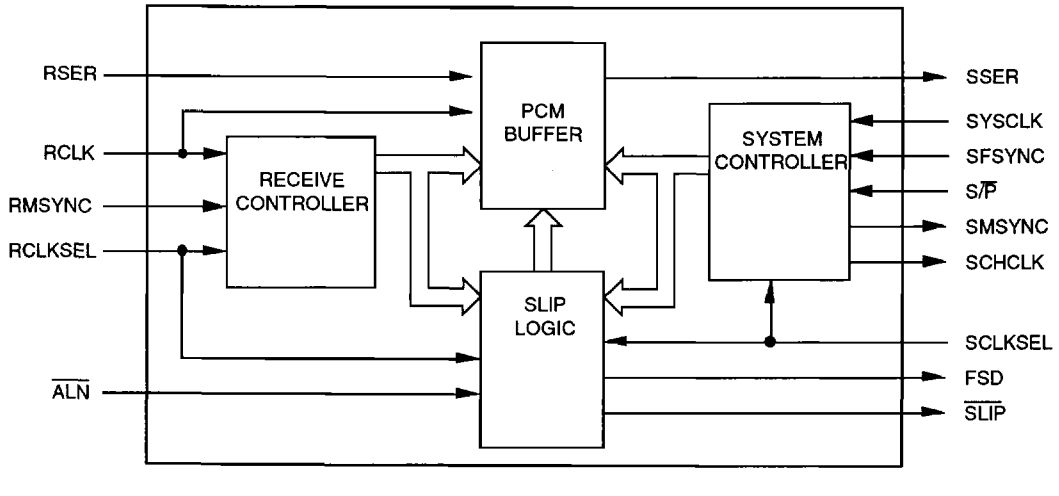
Applications

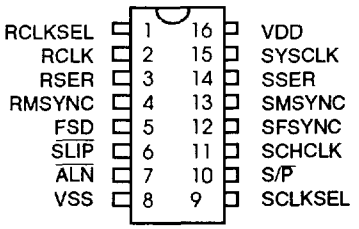
- Digital Trunks
- Drop and Insert Equipment
- Digital Cross-connects (DACS)
- Private Network Equipment
- PABX-to-computer interfaces such as DMI and CPI.

Features

- Drop-in replacement for the DS2175
- Rate buffer for T1/E1 transmissions
- Synchronizes loop-timed and system-timed T1/E1 data streams
- Ideal for 1.544 to 2.048 MHz rate conversion
- Supports parallel and serial backplanes
- Easily monitored two-frame buffer depth
- Comprehensive on-chip slip control logic
- Slips occur only on frame boundaries
- Outputs report slip occurrences and direction
- Align feature allows buffer to be recentered at any time
- Available in 16-pin DIP and SOP
- Compatible with Level One LXP2180A and LXP2181A framer/formatters

Figure 1: Block Diagram





Pin Descriptions

Pin	Sym	I/O	Name	Description
1	RCLKSEL	I	Receive Clock Select	Tie to VSS for 1.544 MHz applications, to VDD for 2.048 MHz.
2	RCLK	I	Receive Clock	Primary 1.544 MHz or 2.048 MHz data clock.
3	RSER	I	Receive Serial Data	Sampled on falling edge of RCLK.
4	RMSYNC	I	Receive Multi-frame Sync	Rising edge establishes receive side frame and multiframe boundaries.
5	FSD	O	Frame Slip Direction	State indicates direction of last slip; latched on slip occurrence.
6	$\overline{\text{SLIP}}$	O	Frame Slip	Active low, open collector output. Held low for 65 SYSCLK cycles when a slip occurs.
7	$\overline{\text{ALN}}$	I	Align	Recenters buffer on next system side frame boundary when forced low.
8	VSS	–	Signal Ground	0.0 volt ground return.
9	SCLKSEL	I	System Clock Select	Tie to VSS for 1.544 MHz applications, to VDD for 2.048 MHz.
10	S/$\overline{\text{P}}$	I	Serial Parallel Select	Tie to VSS for parallel backplane applications, to VDD for serial.
11	SCHCLK	O	System Channel Clock	Transitions high on channel boundaries; useful for serial to parallel conversion of channel data.
12	SFSYNC	I	System Frame Sync	Rising edge establishes system side frame boundaries.
13	SMSYNC	O	System Multi-frame Sync	Slip-compensated multiframe output. Used with RMSYNC to monitor depth of store in real time.
14	SSER	O	System Serial Data	Updated on rising edge of SYSCLK.
15	SYSCLK	I	System Clock	1.544 or 2.048 MHz data clock.
16	VDD	I	Positive Supply	+5 Volt power supply input.

PCM Buffer

The LXP2175 utilizes a two-frame buffer to synchronize incoming PCM data to the system backplane clock. Buffer depth is mode dependent: 2.048 MHz to 2.048 MHz applications use 64 bytes of buffer memory; all other modes are supported by 48 bytes. The buffer samples data at RSER on the falling edge of RCLK. Output data appears at SSER and is updated on the rising edge of SYSCLK. The buffer depth is constantly monitored by on-board contention logic. A "slip" occurs when the buffer is completely emptied or filled. Slips automatically recenter the buffer to a one-frame depth and always occur on frame boundaries.

Data Format

Data is presented to, and output from, the elastic store in a "framed" format. A rising edge at RMSYNC establishes receive side frame boundaries (see Figures 2 and 3). A rising edge at SFSYNC establishes system side multiframe boundaries (see Figures 4 and 5). North American (T1) frames contain 24 data channels of 8 bits each and an F-bit (193 bits total). European (E1) frames contain 32 data channels (256 bits). The frame rate of both systems is 8 KHz. RMSYNC and SFSYNC do not require a pulse at every frame boundary. If desired, they may be pulsed once to establish frame alignment. Internal counters will then maintain the frame alignment and may be reinforced by the next rising edge at RMSYNC and/or SFSYNC.

Slip Correction Capability

The two-frame buffer depth is adequate for T1 and E1 applications where short-term jitter synchronization, rather than correction of significant frequency differences, is required. The LXP2175 provides a balance between total delay (less than 250 ms at its full depth) and slip correction capability.

Buffer Recentering

Many applications require that the buffer be recentered during system power-up and/or initialization. Forcing ALN low recenters the buffer on the next rising edge of SFSYNC. A slip will occur during this recentering if the buffer depth is adjusted. If the depth is presently optimum, no adjustment (slip) occurs.

Slip Reporting

SLIP is held low for 65 SYSCLK cycles when a slip occurs. SLIP is an active-low, open-collector output. FSD indicates slip direction. When low (buffer empty), a frame of data was repeated at SSER during the previous slip. When high (buffer full), a frame of data was deleted. FSD is updated at every slip occurrence.

Buffer Depth Monitoring

SMSYNC is a system side output pulse which indicates system side multiframe boundaries. The distance between rising edges at RMSYNC and SMSYNC indicates the current buffer depth. Slip direction and/or an impending slip condition may be determined by monitoring RMSYNC and SMSYNC real time. SMSYNC is held high for 65 SYSCLK cycles.

Clock Select

Receive and system side clock frequencies are independently selectable by inputs RCLKSEL and SCLKSEL. 1.544 MHz is selected when RCLKSEL (SCLKSEL)=0; and 2.048 MHz is selected when RCLKSEL (SCLKSEL)= 1. In 1.544 MHz (receive) to 1.544 MHz (system) applications, the F-bit is passed through the receive buffer and presented at SSER immediately after a rising edge on SFSYNC. The F-bit is forced to 1 in 2.048 MHz to 1.544 MHz applications. No F-bit position exists in 2.048 MHz system side applications.

Parallel Compatibility

The LXP2175 is compatible with parallel and serial backplanes. In serial applications ($S/\overline{P}$ = 1), channel 1 data appears at SSER after a rising edge at SFSYNC. In parallel applications ($S/\overline{P}$ = 0), the device utilizes a look-ahead circuit. Data is output 8 clocks earlier as shown in Figures 4 and 5, allowing a user to parallel convert data externally, using an HC595 shift register.

Figure 2: Receive Side Timing (RCLK = 1.544 MHz)

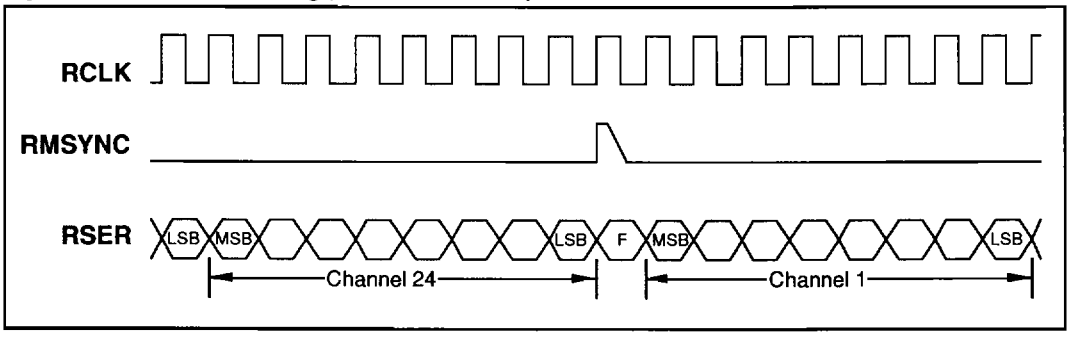
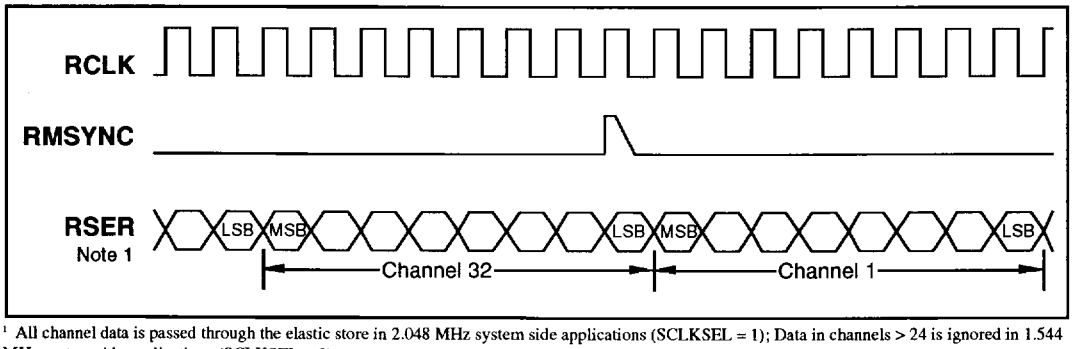
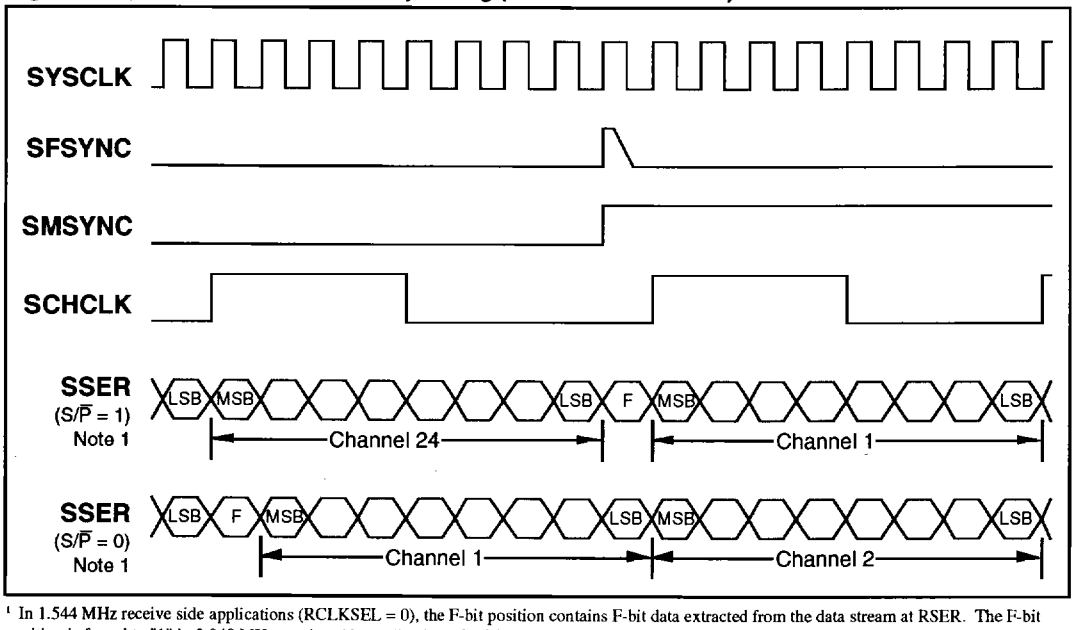


Figure 3: Receive Side Timing (RCLK = 2.048 MHz)



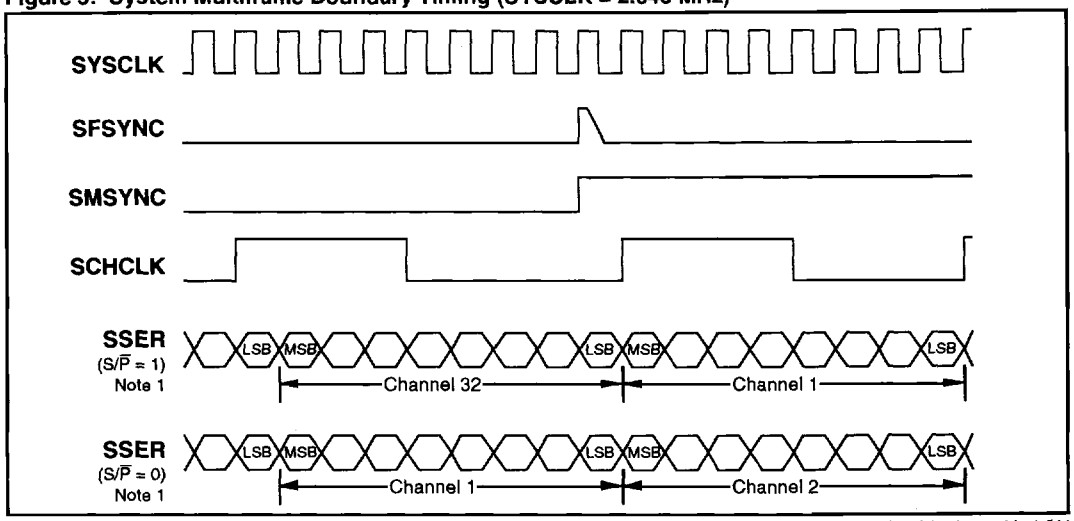
[1] All channel data is passed through the elastic store in 2.048 MHz system side applications (SCLKSEL = 1); Data in channels > 24 is ignored in 1.544 MHz system side applications (SCLKSEL = 0).

Figure 4: System Multiframe Boundary Timing (SYSCLK = 1.544 MHz)



[1] In 1.544 MHz receive side applications (RCLKSEL = 0), the F-bit position contains F-bit data extracted from the data stream at RSER. The F-bit position is forced to "1" in 2.048 MHz receive side applications (RCLKSEL = 1).

Figure 5: System Multiframe Boundary Timing (SYSCLK = 2.048 MHz)



[1] All channel data is passed through the elastic store in 2.048 MHz system side applications (SCLKSEL = 1); Data in channels > 24 is ignored in 1.544 MHz system side applications (SCLKSEL = 0).

Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- Voltage on any pin relative to ground -1.0V to + 7V
- Operating temperature (2175SC and NC) 0 °C (min) to 70 °C (max)
  (2175SE and NE) -40 °C (min) to 85 °C (max)
- Storage temperature -55 °C (min) to 125 °C (max)
- Soldering temperature 260 °C for 10 seconds

Recommended Operating Conditions (Voltages are with respect to ground (VSS) unless otherwise stated)

Parameter	Sym	Min	Typ[1]	Max	Units
Logic 1	V_{IH}	2.0	–	V_{DD} + .3	V
Logic 0	V_{IL}	-0.3	–	+0.8	V
Supply voltage	V_{DD}	4.5	5	5.5	V

DC Electrical Characteristics - Clocked operation over recommended temperature and power supply ranges

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input capacitance	C_{IN}	–	–	5	pF	
Output capacitance	C_{OUT}	–	–	7	pF	
Supply current	I_{DD}	–	6	-	mA	See Notes 2 and 3
Input leakage	I_{IL}	-1.0	–	+1.0	µA	
Output high current	I_{OH}	-1.0	–	–	mA	V_{OH} = 2.4 V, See Note 4
Output low current	I_{OL}	+4.0	–	–	mA	V_{OL} = 0.4 V, See Note 5

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] SYSCLK = RCLK = 1.544 MHz
[3] Outputs Open
[4] All outputs except $\overline{SLIP}$, which is open collector.
[5] All outputs.

A.C. Electrical Characteristics

Parameter	Sym	Min	Max	Units
RCLK Period	t_{RCLK}	200	-	ns
RCLK, SYSCLK Rise and Fall	t_R, t_F	-	20	ns
RCLK Pulse Width	t_{RWH}, t_{RWL}	100	-	ns
SYSCLK Pulse Width	t_{SWH}, t_{SWL}	100	-	ns
SYSCLK Period	t_{SCLK}	200	-	ns
RMSYNC Setup to RCLK Rising	t_{SC}	$-t_{RWH}/2$	$+t_{RWL}/2$	ns
SFSYNC Setup to SYSCLK Rising	t_{SC}	$-t_{SWH}/2$	$+t_{SWL}/2$	ns
RMSYNC, SFSYNC, $\overline{\text{ALN}}$ Pulse Width	t_{PW}	100		ns
RSER Setup to RCLK Falling	t_{SD}	50		ns
RSER Hold from RCLK Falling	t_{HD}	50		ns
Propagation Delay SYSCLK to SSER, or RCLK to RSER	t_{PVD}	-	75	ns
Propagation Delay SYSCLK to SMSYNC High	t_{PSS}	-	75	ns
Propagation Delay SYSCLK or RCLK to $\overline{\text{SLIP}}$ Low, FSD low/high	t_{PS}	-	100	ns
$\overline{\text{ALN}}$ Setup to SFSYNC Rising	t_{SR}	500	-	ns

Figure 6: Receive A.C. Timing Diagram

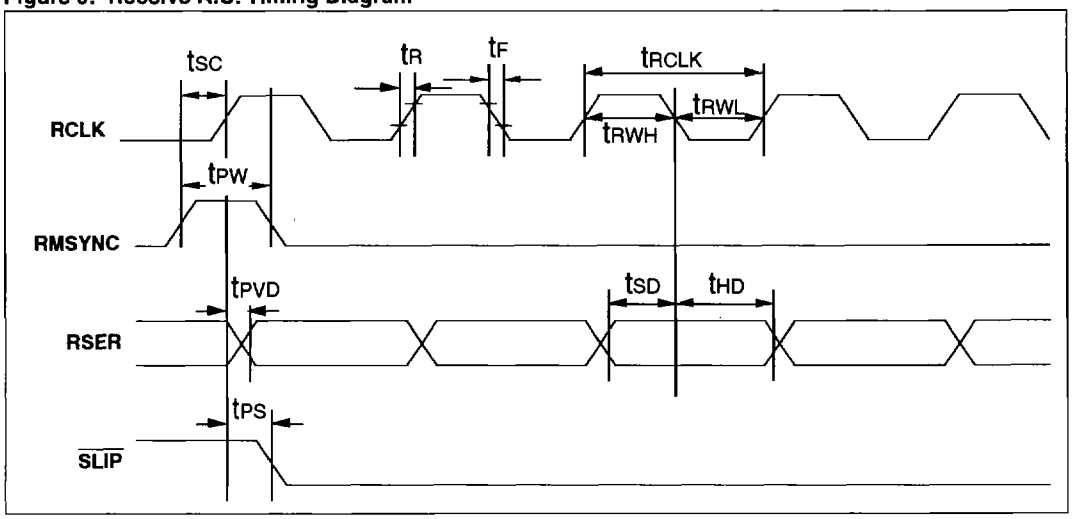


Figure 7: System A.C. Timing Diagram