Monolithic, High Performance 12 Bit D/A Converter Model DAC-681

FEATURES

- 12 Bit Resolution
- 300 nsec. Settling Time
- ±10ppm/°C Max. Tempco
- 5 Output Ranges
- ±¼ LSB Linearity
- 562 Pin Compatibility

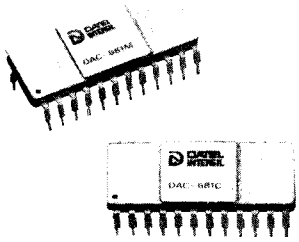
GENERAL DESCRIPTION

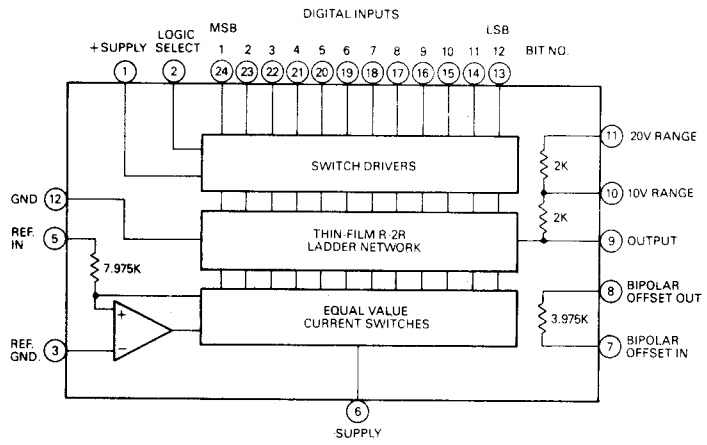
The DAC-681 is a new high performance monolithic 12 bit D/A converter fabricated with advanced bipolar technology. The circuit uses a precision, laser-trimmed thin film R-2R ladder network driven by equal-value switched current sources to achieve ¼ LSB typical linearity, 300 nsec. settling time and ± 10 ppm/°C max. gain tempco.

The DAC-681 operates from TTL or CMOS input logic and provides a 0 to 5 mA or ±2.5 mA output current. The converter contains tracking feedback and bipolar offsetting resistors to provide five output voltage ranges when used with an external operational amplifier: 0 to +5V, 0 to +10V, ±2.5, ±5V, and ±10V. Since these resistors closely track the R-2R ladder with temperature, gain stability of better than 10 ppm/°C is achieved. Differential linearity error is ¼ LSB typical and ½ LSB maximum, with output monotonicity guaranteed over the operating temperature range.

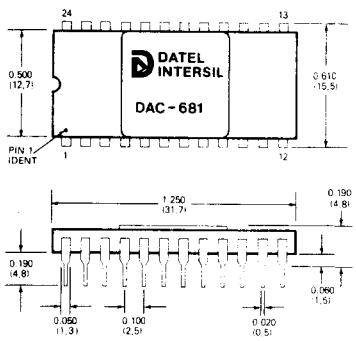
Output settling time for a full scale change to ½ LSB is 300 nsec. typical and 400 nsec. maximum.

The DAC-681 features pin compatibility with 562 type DAC's while offering superior performance to these earlier devices. The package is a 24 pin hermetically sealed ceramic DIP; power requirement is +5V to +15V and −15 VDC. There are two basic models: DAC-681C operates over 0°C to 70°C while DAC-681M operates over −55°C to +125°C.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+ SUPPLY	13	BIT 12 IN (LSB)
2	LOGIC SELECT	14	BIT 11 IN
3	REF. GROUND	15	BIT 10 IN
4	N.C.	16	BIT 9 IN
5	REFERENCE IN	17	BIT 8 IN
6	− SUPPLY	18	BIT 7 IN
7	BIP. OFF. IN	19	BIT 6 IN
8	BIP. OFF. OUT	20	BIT 5 IN
9	OUTPUT	21	BIT 4 IN
10	10V RANGE	22	BIT 3 IN
11	20V RANGE	23	BIT 2 IN
12	GROUND	24	BIT 1 IN (MSB)

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, DAC-681

Typical at 25°C, +5V & −15V Supply, −10V Reference, unless otherwise noted

	DAC-681C	DAC-681M
MAXIMUM RATINGS		
Positive Supply, pin 1	+20V	*
Negative Supply, pin 6	−20V	*
Reference Input, pin 5	±Supply	*
Reference Ground, pin 3	0V	*
Digital Inputs, pins 13-24	−1V to +12V	*
Logic Select Input, pin 2	−1V to +12V	*
Output, pin 9	+Supply, −5V	*
Resistors, pins 7, 8, 10, 11	±Supply	*
INPUTS		
Resolution	12 Bits	*
Coding, unipolar output	Straight Binary	*
Coding, bipolar output	Offset Binary	*
Input Logic Level, bit ON ("1")[1]	+2.0 min. @ 100nA max.	
Input Logic Level, bit OFF ("1")[1]	+0.8V max. @ −100μA max.	
Reference Input Voltage	+10V	*
Reference Input Resistance	8K	*
OUTPUTS		
Output Current, unipolar	0 to −5 mA	*
Output Current, bipolar	±2.5 mA	*
Output Voltage Ranges, unipolar	0 to +5V	*
	0 to +10V	*
Output Voltage Ranges, bipolar	±2.5V	*
	±5V	*
	±10V	*
Output Voltage Compliance	±1V	*
Output Resistance	1K	*
Output Capacitance	20 pF	*
PERFORMANCE		
Linearity Error, max.	±½ LSB	±¼ LSB
Linearity Error Over Temp.,	±1 LSB	±½ LSB
Differential Linearity Error, typ.	±½ LSB	±¼ LSB
Monotonicity	Over Oper. Temp. Range	
Gain Error, max.[2]	±0.25%	*
Unipolar Zero Error, max.[2]	±0.05%	*
Bipolar Offset Error, max.[2]	±0.25%	*
Gain Tempco, max.[3]	±10 ppm/°C	±5 ppm/°C
Zero Tempco, max.[3]	±2 ppm/°C	±2 ppm/°C
Bipolar Offset Tempco, max.[3]	±5 ppm/°C	±5 ppm/°C
Settling Time to ½ LSB[4]	300 nsec. typ., 400 nsec. max.	
Power Supply Sensitivity	±7.5 ppm of FSR/% Supply	
Reference Slew Rate	6 mA/μsec.	*
Reference Bandwidth	10 MHz	*
POWER REQUIREMENT		
Rated Power Supply Voltage	+5 VDC, −15 VDC	
Positive Supply Range[6]	+4.75 VDC to +15 VDC	
Negative Supply Range	−15 VDC ±10%	
Power Supply Quiescent Current, max.	+9 mA, −28 mA	
PHYSICAL-ENVIRONMENTAL		
Operating Temp. Range	0°C to +70°C	−55°C to +125°C
Storage Temp. Range	−65° C to +150°C	*
Package, Hermetically Sealed	24 pin ceramic	*

*Specifications same as first column

NOTES:

1. + Supply must be +5V ±5% for DAC-681C and +5V ±10% for DAC-681M. For operation with CMOS logic see Technical Note 1.
2. Adjustable to zero using external potentiometers. Specified error is for 24.9 ohm trim resistors and external op amp using internal feedback resistor.
3. Using external op amp and internal feedback and offset resistor. Zero Tempco and Bipolar Offset Tempco are in ppm/°C of FSR (Full Scale Range)
4. For full scale change: all bits ON-to-OFF, or all bits OFF-to-ON.
5. See Technical Note 1.

TECHNICAL NOTES

1. For TTL input logic, pin 2 should be connected to pin 12 and the + supply must be +5 VDC (±5% for DAC-681C and ±10% for DAC-681M). For CMOS input logic, connect pin 2 to pin 1 and use any + supply voltage from +4.75V to +12 VDC. CMOS threshold levels are then + Vs × 0.7 for bit ON and +Vs × 0.3 for bit OFF. Logic input current is the same as that specified for TTL.
2. Gain and bipolar offset errors are adjustable to zero by means of two 50 ohm trimming pots. The adjustment range is ±0.3% of FSR for gain and ±0.6% of FSR for bipolar offset. The unipolar zero error is adjustable to zero by means of the offset adjustment of the external output amplifier.
3. The output voltage compliance range of ±1V should not be exceeded or else accuracy will be affected. If a resistor load is driven instead of an op amp summing junction then the maximum resistor value is 200 ohms for unipolar operation and 400 ohms for bipolar operation.
4. Output settling time is specified for current output and is measured with a small current sampling resistor to ground (100 ohms). Voltage output settling time depends on the output operational amplifer used. Datel's AM-500 is recommended for about 500 nsec. settling and AM-452-2 is recommended for about 1.5 μsec. settling. Both should be used with a 3-20 pF variable compensating capacitor across the feedback resistor which should be adjusted for optimum settling time.
5. For best high speed performance, both power supplies should be bypassed with 1 μF electrolytics in parallel with 0.01 μF ceramic capacitors as close as possible to the ± supply pins.
6. The gain and bipolar offset temperature coefficients are specified with the internal feedback and offset resistors used in conjunction with an external operational amplifier. This is because these resistors track the R-2R ladder with temperature and therefore the tempco's do not depend on absolute resistor tempco. The tempco of the external +10V reference must also be included in the total converter tempco, however.
7. Because of the DAC-681 circuit which incorporates equally weighted current sources driving an R-2R ladder network, the turn ON and turn OFF times are virtually symmetrical, resulting in low output glitches compared with other DAC's. The major carry glitch typically has an amplitude of 14% of FSR. The time duration to 90% complete is typically 35 nsec.
8. The DAC-681 wideband output noise with all bits ON is typically 100 μV P-P over 0.1 Hz to 5 MHz.

ORDERING INFORMATION

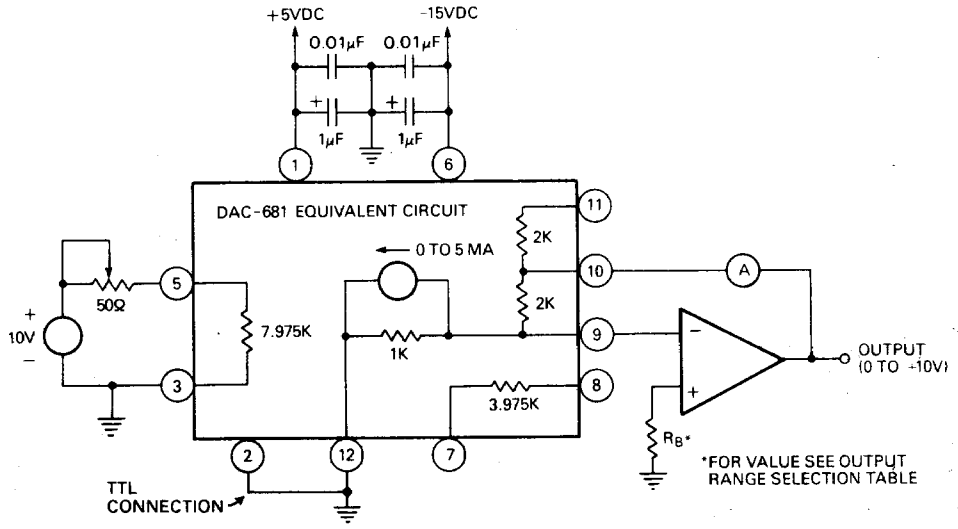
Model	Temp. Range
DAC-681C	0 to 70°C
DAC-681M	−55 to +125°C

Trimming Potentiometer: TP50

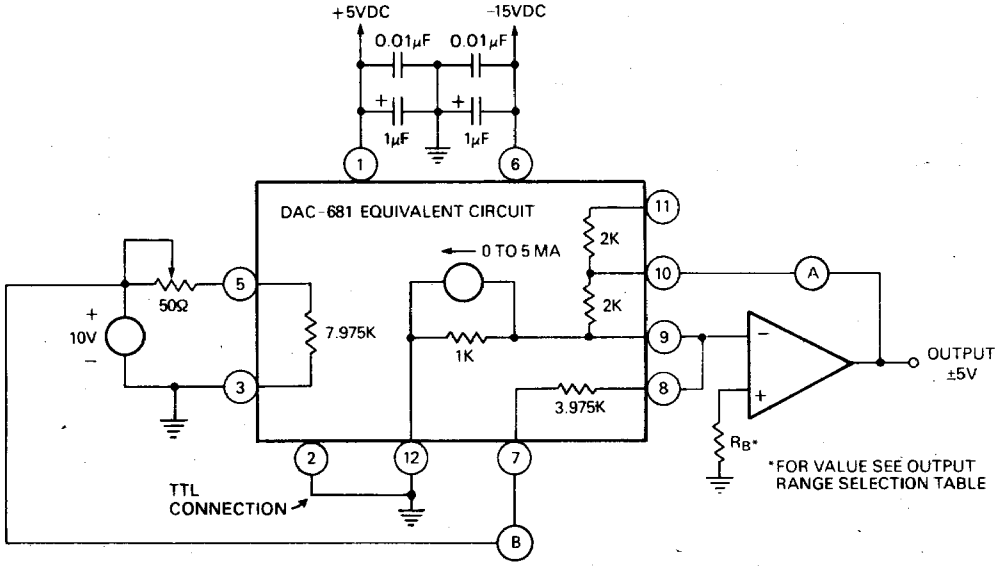
THESE CONVERTERS ARE COVERED BY GSA CONTRACT.

STANDARD CONNECTIONS

UNIPOLAR OPERATION—See Output Range Selection Table



BIPOLAR OPERATION—See Output Range Selection Table



OUTPUT VOLTAGE RANGE SELECTION (See Connection Diagrams Above)

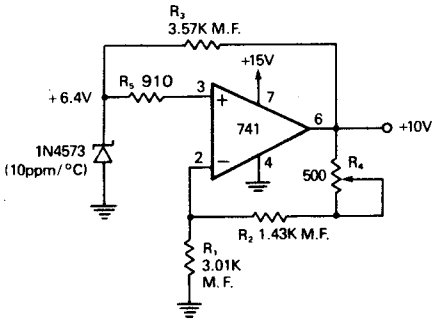
OUTPUT VOLTAGE RANGE	CONNECT THESE PINS TOGETHER				R_B, BIAS COMP. RESISTOR*
0 to +5V	A & 10	9 & 11			510
0 to +10V	A & 10				680
±2.5V	A & 10	9 & 11	8 & 9	7 & B	430
±5V	A & 10	8 & 9	7 & B		560
±10V	A & 11	8 & 9	7 & B		680

*Carbon composition resistor value used from amplifier + input terminal to ground to compensate for offset due to bias current.

CODING TABLE—See Calibration Procedure

INPUT CODE	OUTPUT VOLTAGE RANGE				
	0 TO +5V	0 TO +10V	±2.5V	±5V	±10V
1111 1111 1111	+4.9988V	+9.9976V	+2.4988V	+4.9976V	+9.9951V
1100 0000 0000	+3.7500	+7.5000	+1.2500	+2.5000	+5.0000
1000 0000 0000	+2.5000	+5.0000	0.0000	0.0000	0.0000
0100 0000 0000	+1.2500	+2.5000	−1.2500	−2.5000	−5.0000
0000 0000 0001	+0.0012	+0.0024	−2.4988	−4.9976	−9.9951
0000 0000 0000	0.0000	0.0000	−2.5000	−5.0000	−10.0000

+10V REFERENCE CIRCUIT



Adjust R_4 for +10.000V output. For best stability R_1 & R_2 should track each other closely with temperature. R_4 should be a low tempco trimming pot or else a selected metal film trim resistor.

CALIBRATION PROCEDURE

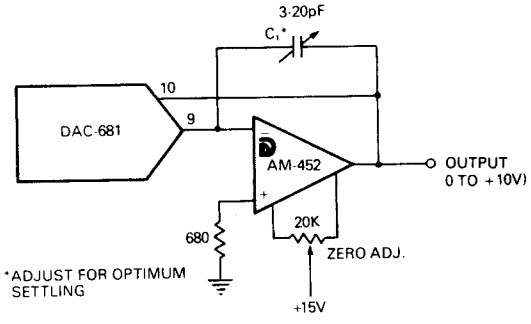
UNIPOLAR OPERATION

1. Set all digital inputs LO. Adjust the output amplifier offset for 0 volts output.
2. Set all digital inputs HI. Adjust Gain trimming pot for an output of +FS-1LSB.
   FS-1LSB = +9.9976V for 0 to +10V range.
   = +4.9988V for 0 to +5V range.

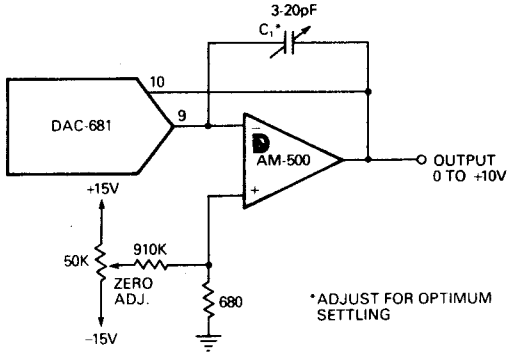
BIPOLAR OPERATION

1. Set all digital inputs LO. Adjust Bipolar Offset trimming pot for one of the following output voltages:
   −2.5V for ±2.5V range
   −5.0V for ±5V range
   −10.0V for ±10V range
2. Set bit 1 (MSB) input HI and all other digital inputs LO. Adjust Gain trimming pot for 0 volts output.

CIRCUIT FOR FAST VOLTAGE OUTPUT (≂1.5 μSEC. SETTLING)



CIRCUIT FOR FAST VOLTAGE OUTPUT (≂0.5 μSEC. SETTLING)



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