DECT SiGe Front End IC

Description

The U7006B is a monolithic SiGe transmit/receive front end IC with power amplifier, internally 50-Ω matched, low-noise amplifier and T/R switch driver. It is especially designed for operation in TDMA systems like DECT. Due to the ramp-control feature and a very low quiescent current an external switch transistor for V_S is not required.

Electrostatic sensitive device.
Observe precautions for handling.

Features

- Single 3-V supply voltage
- High-power-added efficient power amplifier (P_{out} typ. 26.5 dBm)
- Ramp-controlled output power
- Low-noise preamplifier (NF typ. 1.8 dB)
- Biasing for external PIN diode T/R switch
- Current-saving standby mode
- Few external components

Block Diagram

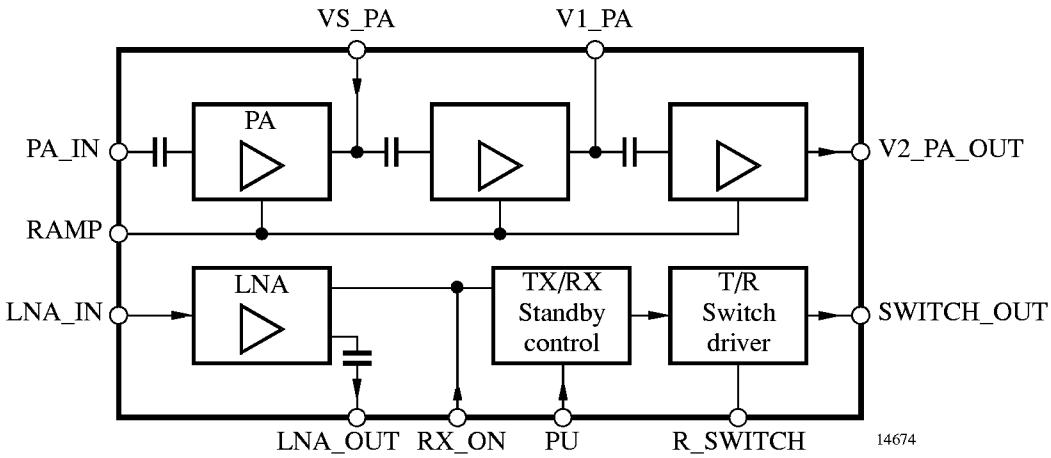


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U7006B-MFB	PSSOP16	
U7006B-MFB-G3	PSSOP16	Taped and reeled

Preliminary Information

Pin Description

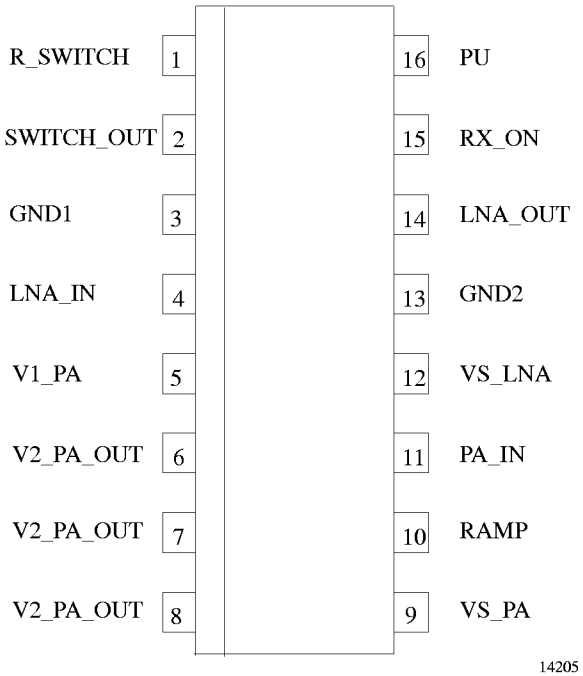


Figure 2. Pinning

Pin	Symbol	Function
1	R_SWITCH	Resistor to GND sets the PIN diode current
2	SWITCH_OUT	Switched current output for PIN diode
3	GND1	Ground
4	LNA_IN	Low-noise amplifier input
5	V1_PA	Inductor to power supply for power amplifier
6 7 8	V2_PA_OUT	Inductor to power supply and matching network for power amplifier output
9	VS_PA	Supply voltage for power amplifier
10	RAMP	Power-ramping control input
11	PA_IN	Power amplifier input
12	VS_LNA	Supply-voltage input for low-noise amplifier
13	GND2	Ground
14	LNA_OUT	Low-noise amplifier output
15	RX_ON	RX active high
16	PU	Power-up active high

Absolute Maximum Ratings

All voltages are referred to GND (Pin 3 and slug)

Parameters		Symbol	Value	Unit
Supply voltage	Pins 6, 10, 13 and 16	V_S	6	V
Junction temperature		T_j	150	°C
Storage temperature		T_{stg}	–40 to +125	°C
Input power PA Pin 11		P_{inPA}	+10	dBm
Input power LNA Pin 4		P_{inLNA}	–5	dBm
ESD protection according to ESD-S5.2-1994			Class M1	

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	19	K/W

Operating Range

All voltages are referred to GND (Pins 3, 13 and slug). Power supply points are VS_LNA, VS_PA, V1_PA, V2_PA_OUT. The following table represents the sum of all supply currents depending on of the TX/RX mode.

Parameters		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pins 5, 6, 7, 8 and 9	V_S	2.7	3.0	4.6	V
Supply voltage	Pin 12	V_S	2.7	3.6	5.5	V
Supply current	TX RX	I_S I_S		350 8		mA mA
Standby current	PU = 0	I_S		10		µA
Ambient temperature		T_{amb}	–25	+25	+70	°C

Electrical Characteristics

Test conditions (unless otherwise specified): V_S = 3.0 V, T_{amb} = 25°C, cw mode

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Power amplifier [1]						
Supply voltage	Pins 5, 6, 7, 8 and 9	V_S	2.7	3.0	4.6	V
Supply current	TX	I_{S_TX}		350		mA
	RX (PA off)	I_{S_RX}			10	µA
Standby current	Standby	$I_{S\_standby}$			10	µA
Frequency range	TX	f	1.88		1.94	GHz
Power gain	TX Pin 11 to Pins 6, 7, 8	Gp		28		dB
Gain-control range	TX	ΔGp		48		dB
Ramping voltage	TX, power gain (max) Pin 10	$V_{RAMP\ max}$		2.1		V
Ramping current		I_{RAMP}		0.5	2.0	mA
Power-added efficiency	TX	PAE		40		%
Saturated output power	TX, referred to Pins 6, 7, 8	P_{sat}		26.5		dBm
Input matching [2]	TX Pin 11	VSWRin		<2.0:1		
Output matching [2]	TX Pins 6, 7, 8	VSWRout		<2.0:1		
Harmonics @P 1dB	TX Pins 6, 7, 8	2 fo		–30		dBc
		3 fo				
Max. input power	Pin 11	P_{inPA}		10		dBm
Stability (no harmonic emission)	TX Pin 6, 7, 8 P_{in} = 2 dBm, V_{RAMP} = 2 V VSWRout <10:1 (all phases)			–60		dBc
T/R–switch driver (current programming by external resistor from R_SWITCH to GND)						
Switch-out current output	Standby Pin 2	$I_{S\_O\_standby}$			2	µA
	RX	$I_{S\_O\_RX}$			2	µA
	TX @ 100 Ω	$I_{S\_O\_100}$		1		mA
	TX @ 1.2 kΩ	$I_{S\_O\_1k2}$		3		mA
	TX @ 33 kΩ	$I_{S\_O\_33k}$		10		mA

Note: 1) Power amplifier shall be unconditional stable, maximum load mismatch and duration: t.b.d.

2) With external matching network (see figure 13)

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Low-noise amplifier [3]						
Supply voltage	All Pin 12	V_S	2.7	3.6	5.5	V
Supply current	RX	I_S		8		mA
Supply current (LNA and control logic)	TX (control logic active) Pin 12	I_S		300		µA
Standby current	Standby Pin 12	I_S		1	10	µA
Frequency range	RX	f	1.88		1.94	GHz
Power gain	RX Pin 4 to Pin 14	Gp	17	19		dB
Noise figure	RX	NF		1.8	2.0	dB
Gain compression	RX, referred to Pin 14	P1dB		–7		dBm
3rd-order input interception point	RX	IIP3		–15		dBm
Input matching	RX	VSWRin		<2:1		
Output matching	RX	VSWRout		<2:1		
Logic input levels (RX_ON, PU)						
High input level	= '1' Pins 5 and 16	V_{iH}	2.4		V_S	V
Low input level	= '0'	V_{iL}	0		0.5	V
High input current	= '1'	I_{iH}		40		µA
Low input current	= '0'	I_{iL}		0		µA

3) Low-noise amplifier shall be unconditional stable

Control Logic

	PU
Power up	1
Standby	0

	RX_ON
RX mode	1
TX mode	0

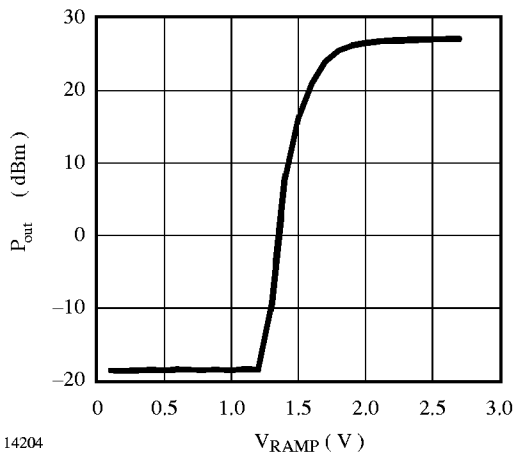


Figure 3. Output power vs. ramp voltage

Input / Output Circuits

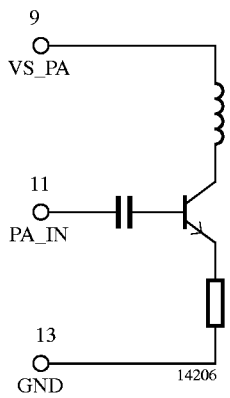


Figure 4.

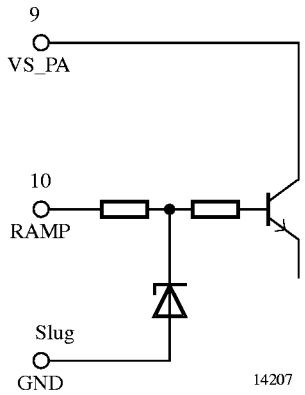


Figure 5.

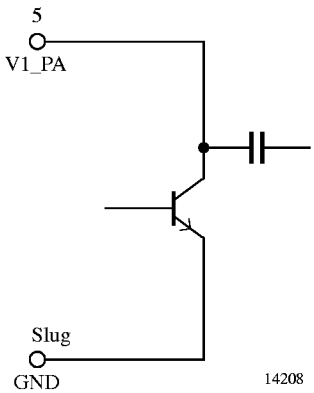


Figure 6.

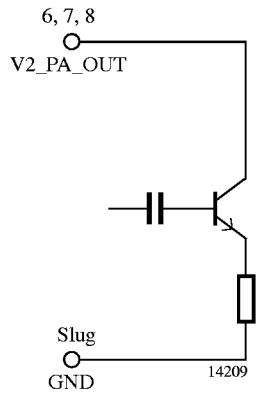


Figure 7.

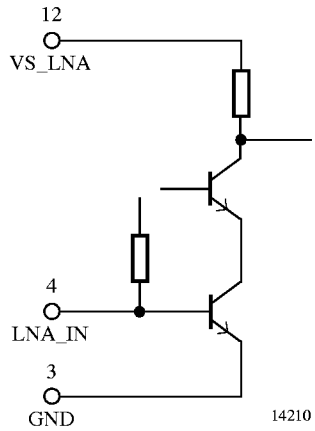


Figure 8.

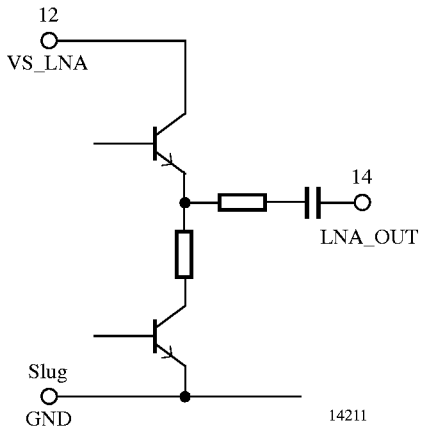


Figure 9.

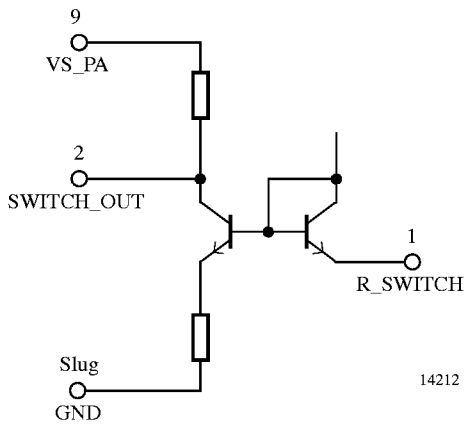


Figure 10.

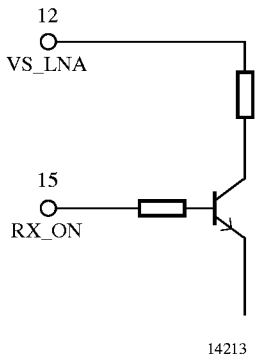


Figure 11.

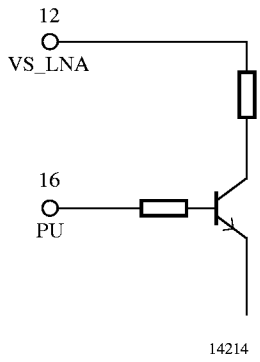


Figure 12.

Typical Application Circuit

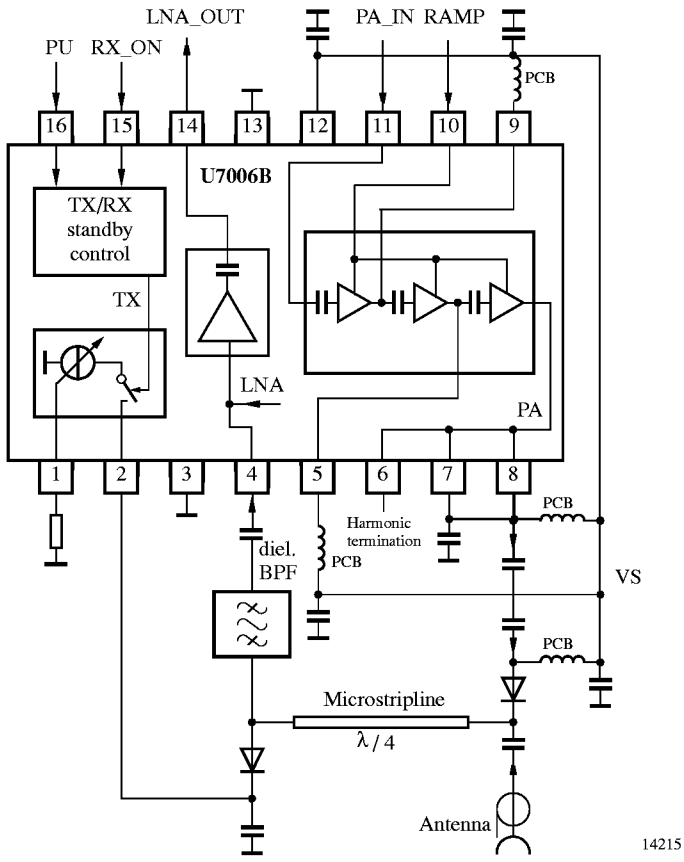


Figure 13. Typical schematic

Application Board

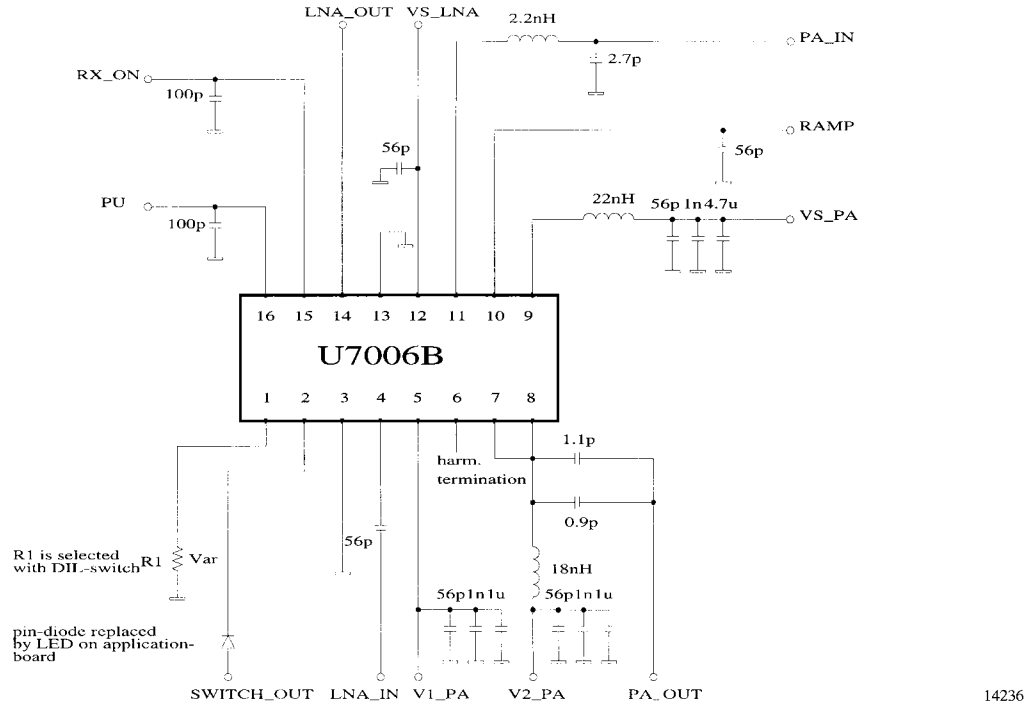


Figure 14. U7006B application board schematic

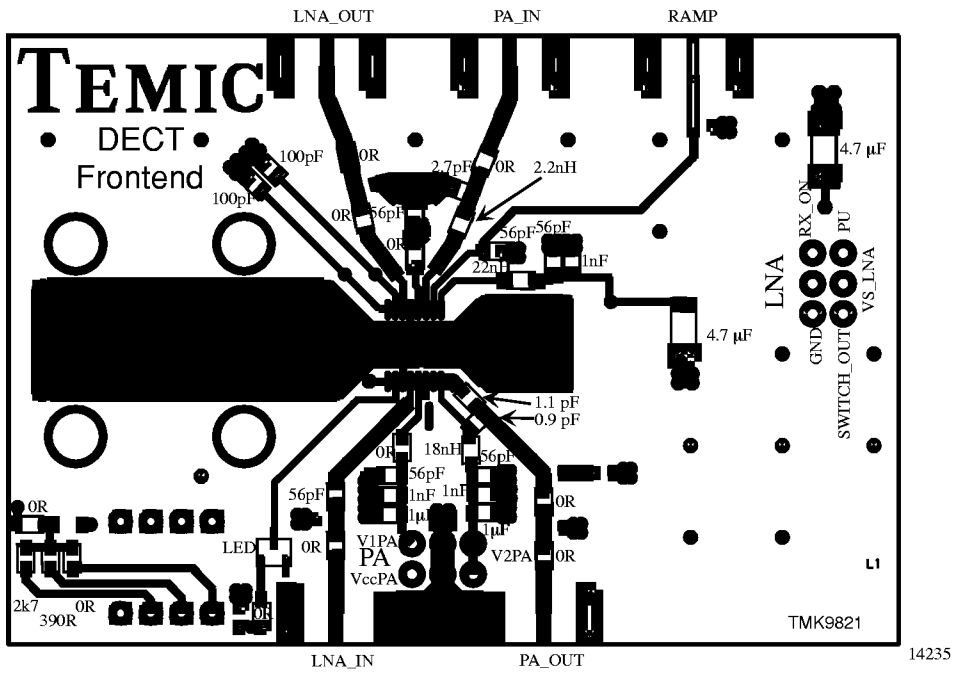
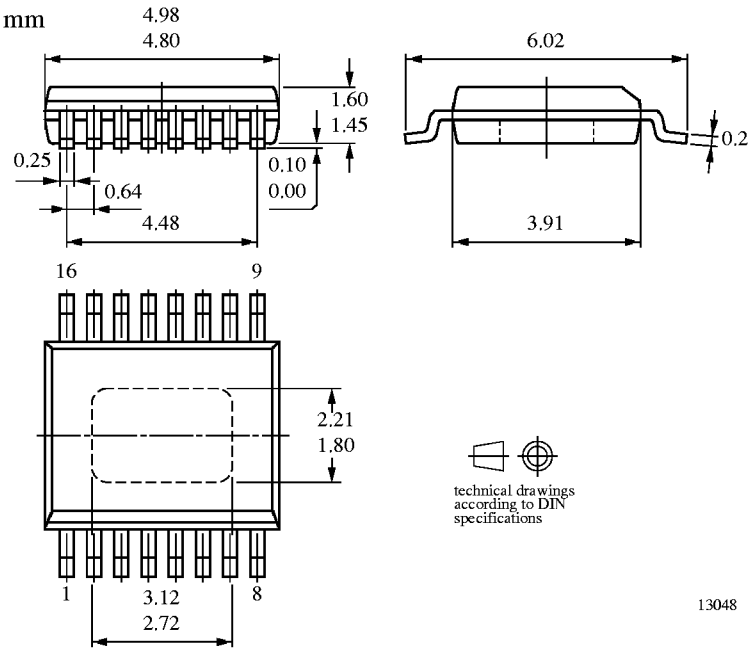


Figure 15. U7006B application board layout

Package Information

Package PSSOP16

Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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