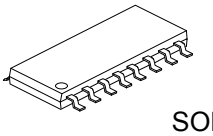
7 CHANNEL SINK TYPE DMOS TRANSISTOR ARRAY



SOP-16

■ DESCRIPTION

The UTC **ULD2003** is DMOS transistor array with 7 circuits. It has a clamp diode for switching inductive loads built-in in each output. Please be careful about thermal conditions during use.

■ FEATURES

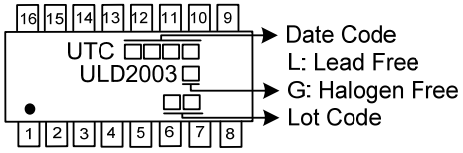
* 7 circuits built-in
* High voltage: V_{OUT} = 50V (MAX)
* High current: I_{OUT} = 500mA/ch (MAX)
* Input voltage(output on): 2.5V (MIN)
* Input voltage(output off): 0.6V (MAX)

■ ORDERING INFORMATION

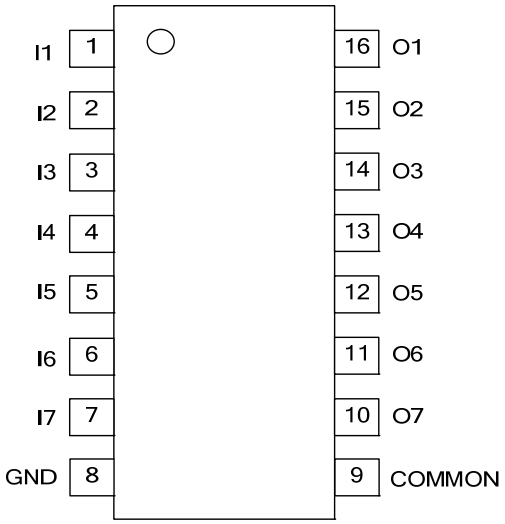
Ordering Number		Package	Packing
Lead Free	Halogen Free		
ULD2003L-S16-R	ULD2003G-S16-R	SOP-16	Tape Reel

ULD2003G-S16-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S16: SOP-16 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



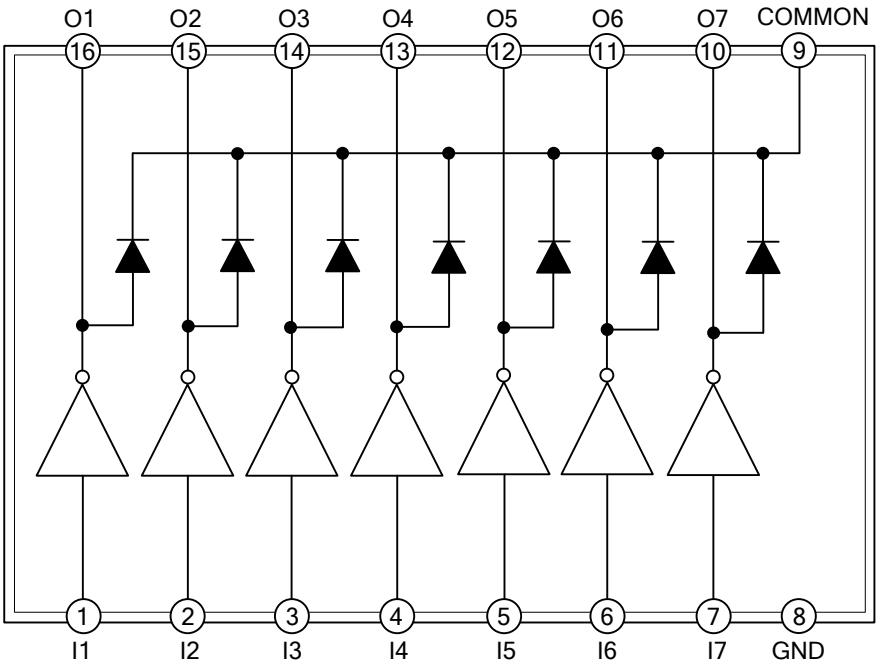
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	I1	1 Channel Input pin
2	I2	2 Channel Input pin
3	I3	3 Channel Input pin
4	I4	4 Channel Input pin
5	I5	5 Channel Input pin
6	I6	6 Channel Input pin
7	I7	7 Channel Input pin
8	GND	GND pin
9	COMMON	Common pin
10	Q7	7 Channel Output pin
11	Q6	6 Channel Output pin
12	Q5	5 Channel Output pin
13	Q4	4 Channel Output pin
14	Q3	3 Channel Output pin
15	Q2	2 Channel Output pin
16	Q1	1 Channel Output pin

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Output Voltage	V_{OUT}	50	V
COMMON Pin Voltage	V_{COM}	-0.5 ~ 50	V
Output Current	I_{OUT}	500	mA/ch
Input Voltage	V_{IN}	-0.5 ~ 30	V
Clamp Diode Reverse Voltage	V_R	50	V
Clamp Diode Forward Current	I_F	500	mA
Power Dissipation (Note 1)	P_D	1.25	W
Operating Temperature	T_{OPR}	-40 ~ +85	°C
Storage Temperature	T_{STG}	-55 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ OPERATING RANGES (T_A=-40~+85°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output Voltage	V_{OUT}					50	V
COMMON Pin Voltage	V_{COM}			0		50	V
Output Current (Note 1)	I_{OUT}	1 Circuits ON, Ta =25°C		0		400	mA/ch
		t_{PW}=25ms 7 Circuits ON T_A=85°C T_J=120°C	Duty = 10%	0		390	mA/ch
			Duty = 50%	0		170	mA/ch
Input Voltage (Output On)	$V_{IN\ (ON)}$	I_{OUT}=100mA or Upper, V_{OUT}=2V		2.5		25	V
Input Voltage (Output Off)	$V_{IN\ (OFF)}$	I_{OUT}=100μA or Less, V_{OUT}=2V		0		0.6	V
Clamp Diode Forward Current	I_F					400	mA

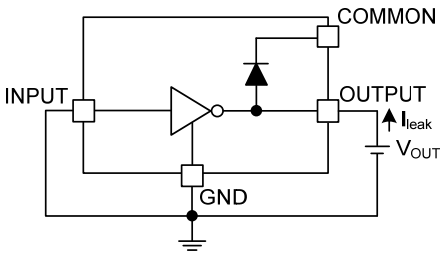
Note: On PCB (JEDEC 2s2p).

■ ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

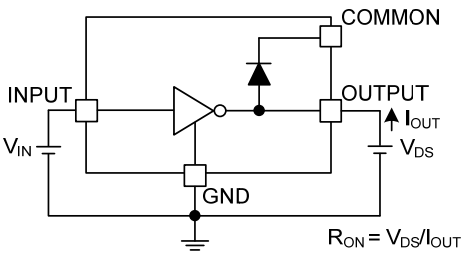
PARAMETER	SYMBOL	Test Circuit	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Leakage Current	I_{leak}	1	V_{OUT}=50V, T_A=85°C, V_{IN}=0V			1.0	μA
Output Voltage (Output ON-Resistance)	V_{DS} (R_{ON})	2	I_{OUT}=350mA, V_{IN}=5.0V		0.7 (2.0)	1.14 (3.25)	V (Ω)
			I_{OUT}=200mA, V_{IN}=5.0V		0.4 (2.0)	0.65 (3.25)	V (Ω)
			I_{OUT}=100mA, V_{IN}=5.0V		0.2 (2.0)	0.325 (3.25)	V (Ω)
Input Current (Output On)	$I_{IN\ (ON)}$	3	V_{IN}=2.5V			0.1	mA
Input Current(Output Off)	$I_{IN\ (OFF)}$	4	V_{IN}=0V, T_A=85°C			1.0	μA
Input Voltage (Output On)	$V_{IN\ (ON)}$	5	I_{OUT}=100mA, V_{OUT}=2V			2.5	V
Clamp Diode Reverse Current	I_R	6	V_R=50V, T_A=85°C			1.0	μA
Clamp Diode Forward Voltage	V_F	7	I_F=350mA			2.0	V
Turn-On Delay	t_{ON}	8	V_{OUT}=50V, R_L=125Ω, C_L=15pF		0.4		μs
Turn-Off Delay	t_{OFF}				0.8		μs

■ TEST CIRCUIT

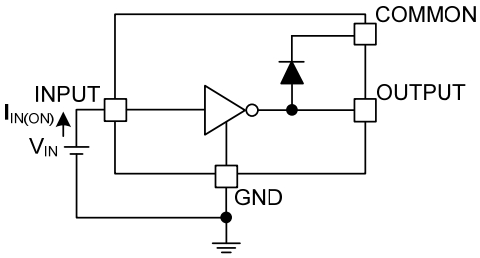
1. I_{leak}



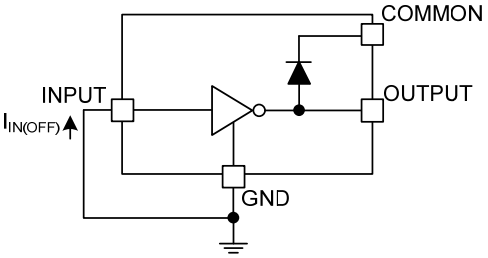
2. V_{DS} (RON)



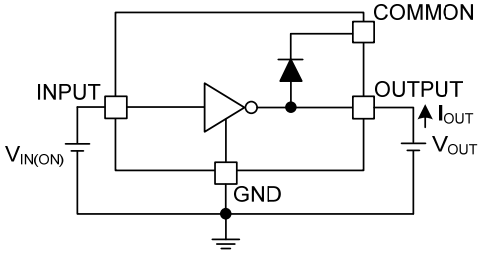
3. $I_{IN\ (ON)}$



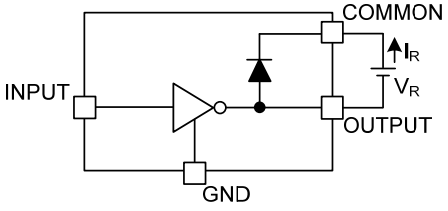
4.$I_{IN(OFF)}$



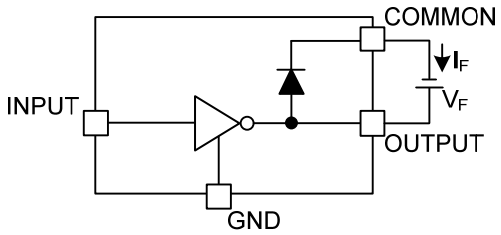
5. $V_{IN\ (ON)}$



6. I_R



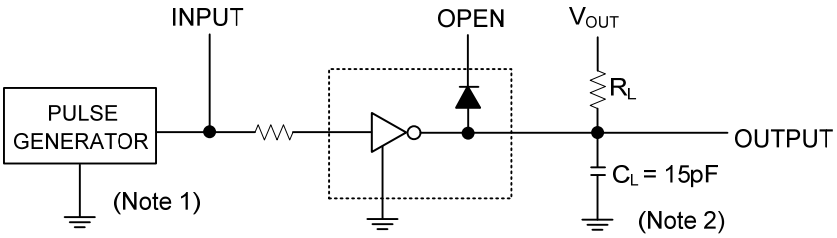
7. V_F

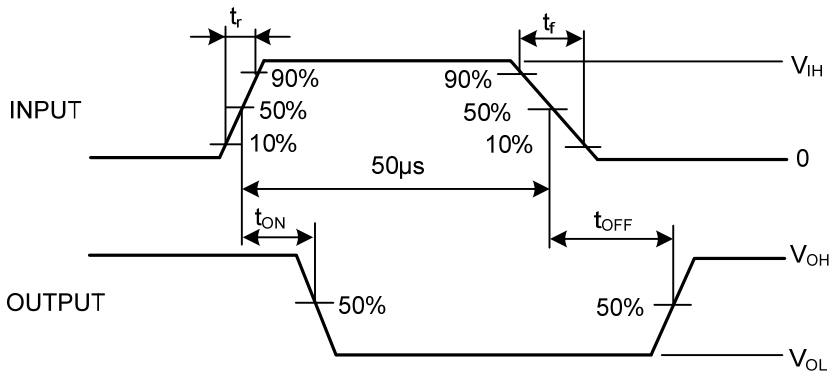


Test circuit may be simplified for explanatory purpose.

■ TEST CIRCUIT (Cont.)

8. t_{ON}, t_{OFF}





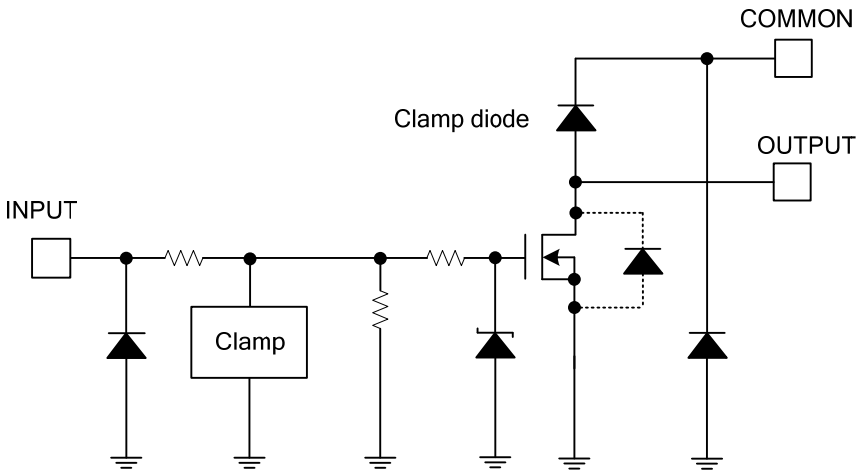
Note 1: Pulse width 50μs, Duty cycle 10%
Output impedance 50Ω, $t_r \leq 5ns$, $t_f \leq 10ns$
Please refer to the following table for the V_{IH} condition.

Product	V_{IH}
ULD2003	5.0V

2. C_L includes the probe and the test board capacitance.

Test circuit and timing chart may be simplified for explanatory purpose.

■ EQUIVALENT CIRCUIT (EACH DRIVER)



Equivalent circuit may be simplified for explanatory purpose.