

## CD4046BC Micropower Phase-Locked Loop

### General Description

The CD4046BC micropower phase-locked loop (PLL) consists of a low power, linear, voltage-controlled oscillator (VCO), a source follower, a zener diode, and two phase comparators. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

Phase comparator I, an exclusive OR gate, provides a digital error signal (phase comp. I Out) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator II is an edge-controlled digital memory network. It provides a digital error signal (phase comp. II Out) and lock-in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input.

The linear voltage-controlled oscillator (VCO) produces an output signal (VCO Out) whose frequency is determined by the voltage at the VCO<sub>IN</sub> input, and the capacitor and resistors connected to pin C1<sub>A</sub>, C1<sub>B</sub>, R1 and R2.

The source follower output of the VCO<sub>IN</sub> (demodulator Out) is used with an external resistor of 10 kΩ or more.

The INHIBIT input, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode is provided for power supply regulation, if necessary.

### Features

- Wide supply voltage range: 3.0V to 18V
- Low dynamic power consumption: 70 μW (typ.) at f<sub>o</sub> = 10 kHz, V<sub>DD</sub> = 5V
- VCO frequency: 1.3 MHz (typ.) at V<sub>DD</sub> = 10V
- Low frequency drift: 0.06%/°C at V<sub>DD</sub> = 10V with temperature
- High VCO linearity: 1% (typ.)

### Applications

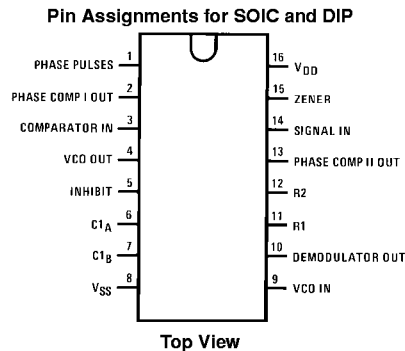
- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discrimination
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Tone decoding
- FSK modulation
- Motor speed control

### Ordering Code:

Order Number	Package Number	Package Description
CD4046BCM	M16A	16-Lead Small Outline integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
CD4046BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram





### Absolute Maximum Ratings (Note 1)

(Note 2)

DC Supply Voltage ( $V_{DD}$ )	-0.5 to +18 $V_{DC}$
Input Voltage ( $V_{IN}$ )	-0.5 to $V_{DD}$ +0.5 $V_{DC}$
Storage Temperature Range ( $T_S$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature ( $T_L$ )	
(Soldering, 10 seconds)	260°C

### Recommended Operating Conditions (Note 2)

DC Supply Voltage ( $V_{DD}$ )	3 to 15 $V_{DC}$
Input Voltage ( $V_{IN}$ )	0 to $V_{DD}$ $V_{DC}$
Operating Temperature Range ( $T_A$ )	-40°C to +85°C

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:**  $V_{SS}$  = 0V unless otherwise specified.

### DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	Pin 5 = $V_{DD}$ , Pin 14 = $V_{DD}$ , Pin 3, 9 = $V_{SS}$ $V_{DD}$ = 5V		20	0.005	20		150	$\mu$ A	
		$V_{DD}$ = 10V		40	0.01	40		300	$\mu$ A	
		$V_{DD}$ = 15V		80	0.015	80		600	$\mu$ A	
		Pin 5 = $V_{DD}$ , Pin 14 = Open, Pin 3, 9 = $V_{SS}$ $V_{DD}$ = 5V		70	5	55		205	$\mu$ A	
	$V_{DD}$ = 10V		530	20	410		710	$\mu$ A		
	$V_{DD}$ = 15V		1500	50	1200		1800	$\mu$ A		
$V_{OL}$	LOW Level Output Voltage	$V_{DD}$ = 5V		0.05	0	0.05		0.05	V	
		$V_{DD}$ = 10V		0.05	0	0.05		0.05	V	
		$V_{DD}$ = 15V		0.05	0	0.05		0.05	V	
$V_{OH}$	HIGH Level Output Voltage	$V_{DD}$ = 5V	4.95		4.95	5		4.95	V	
		$V_{DD}$ = 10V	9.95		9.95	10		9.95	V	
		$V_{DD}$ = 15V	14.95		14.95	15		14.95	V	
$V_{IL}$	LOW Level Input Voltage Comparator and Signal In	$V_{DD}$ = 5V, $V_O$ = 0.5V or 4.5V		1.5	2.25	1.5		1.5	V	
		$V_{DD}$ = 10V, $V_O$ = 1V or 9V		3.0	4.5	3.0		3.0	V	
		$V_{DD}$ = 15V, $V_O$ = 1.5V or 13.5V		4.0	6.25	4.0		4.0	V	
$V_{IH}$	HIGH Level Input Voltage Comparator and Signal In	$V_{DD}$ = 5V, $V_O$ = 0.5V or 4.5V	3.5		3.5	2.75		3.5	V	
		$V_{DD}$ = 10V, $V_O$ = 1V or 9V	7.0		7.0	5.5		7.0	V	
		$V_{DD}$ = 15V, $V_O$ = 1.5V or 13.5V	11.0		11.0	8.25		11.0	V	
$I_{OL}$	LOW Level Output Current <small>(Note 4)</small>	$V_{DD}$ = 5V, $V_O$ = 0.4V	0.52		0.44	0.88		0.36	mA	
		$V_{DD}$ = 10V, $V_O$ = 0.5V	1.3		1.1	2.25		0.9	mA	
		$V_{DD}$ = 15V, $V_O$ = 1.5V	3.6		3.0	8.8		2.4	mA	
$I_{OH}$	HIGH Level Output Current <small>(Note 4)</small>	$V_{DD}$ = 5V, $V_O$ = 4.6V	-0.52		-0.44	-0.88		-0.36	mA	
		$V_{DD}$ = 10V, $V_O$ = 9.5V	-1.3		-1.1	-2.25		-0.9	mA	
		$V_{DD}$ = 15V, $V_O$ = 13.5V	-3.6		-3.0	-8.8		-2.4	mA	
$I_{IN}$	Input Current	All Inputs Except Signal Input $V_{DD}$ = 15V, $V_{IN}$ = 0V		-0.3	$10^{-5}$	-0.3		-1.0	$\mu$ A	
		$V_{DD}$ = 15V, $V_{IN}$ = 15V		0.3	$10^{-5}$	0.3		1.0	$\mu$ A	
$C_{IN}$	Input Capacitance	Any Input <small>(Note 3)</small>					7.5		pF	
$P_T$	Total Power Dissipation	$f_o$ = 10 kHz, $R1$ = 1 M $\Omega$ , $R2$ = $\infty$ , $C \times X_{OIN} = C_{MAX}/2$ $V_{DD}$ = 5V				0.07			mW	
		$V_{DD}$ = 10V				0.6			mW	
		$V_{DD}$ = 15V				2.4			mW	

**Note 3:** Capacitance is guaranteed by periodic testing.

**Note 4:**  $I_{OH}$  and  $I_{OL}$  are tested one output at a time.

AC Electrical Characteristics (Note 5)							
T <sub>A</sub> = 25°C, C <sub>L</sub> = 50 pF							
Symbol	Parameter	Conditions	Min	Typ	Max	Units	
<b>VCO SECTION</b>							
I <sub>DD</sub>	Operating Current	f <sub>o</sub> = 10 kHz, R1 = 1 MΩ, R2 = ∞, ζXO <sub>IN</sub> = ζ <sub>ΔΔ</sub> /2 V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		20 90 200		μA μA μA	
f <sub>MAX</sub>	Maximum Operating Frequency	C1 = 50 pF, R1 = 10 kΩ, R2 = ∞, ζXO <sub>IN</sub> = ζ <sub>ΔΔ</sub> V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V	0.4 0.6 1.0	0.8 1.2 1.6		MHz MHz MHz	
		Linearity	VCO <sub>IN</sub> = 2.5V ±0.3V, R1 ≥ 10 kΩ, V <sub>DD</sub> = 5V VCO <sub>IN</sub> = 5V ±2.5V, R1 ≥ 400 kΩ, V <sub>DD</sub> = 10V VCO <sub>IN</sub> = 7.5V ±5V, R1 ≥ 1 MΩ, V <sub>DD</sub> = 15V		1 1 1		% % %
			Temperature-Frequency Stability No Frequency Offset, f <sub>MIN</sub> = 0	%/°C ∝ 1/φ, ζ <sub>ΔΔ</sub> R2 = ∞ V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		0.12–0.24 0.04–0.08 0.015–0.03	
	Frequency Offset, f <sub>MIN</sub> ≠ 0	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		0.06–0.12 0.05–0.1 0.03–0.06		%/°C %/°C %/°C	
	VCO <sub>IN</sub>	Input Resistance	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		10 <sup>6</sup> 10 <sup>6</sup> 10 <sup>6</sup>		MΩ MΩ MΩ
VCO	Output Duty Cycle	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		50 50 50		% % %	
t <sub>THL</sub>	VCO Output Transition Time	V <sub>DD</sub> = 5V		90	200	ns	
t <sub>THL</sub>		V <sub>DD</sub> = 10V		50	100	ns	
		V <sub>DD</sub> = 15V		45	80	ns	
<b>PHASE COMPARATORS SECTION</b>							
R <sub>IN</sub>	Input Resistance Signal Input	V <sub>DD</sub> = 5V	1	3		MΩ	
		V <sub>DD</sub> = 10V	0.2	0.7		MΩ	
		V <sub>DD</sub> = 15V	0.1	0.3		MΩ	
	Comparator Input	V <sub>DD</sub> = 5V			10 <sup>6</sup>		MΩ
		V <sub>DD</sub> = 10V			10 <sup>6</sup>		MΩ
V <sub>DD</sub> = 15V				10 <sup>6</sup>		MΩ	
AC-Coupled Signal Input Voltage Sensitivity	C <sub>SERIES</sub> = 1000 pF f = 50 kHz V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V			200	400	mV	
				400	800	mV	
				700	1400	mV	

## AC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DEMODULATOR OUTPUT</b>						
VCO <sub>IN</sub> - V <sub>DEM</sub>	Offset Voltage	RS ≥ 10 kΩ, V <sub>DD</sub> = 5V		1.50	2.2	V
		RS ≥ 10 kΩ, V <sub>DD</sub> = 10V		1.50	2.2	V
		RS ≥ 50 kΩ, V <sub>DD</sub> = 15V		1.50	2.2	V
	Linearity	RS ≥ 50 kΩ				
		VCO <sub>IN</sub> = 2.5V ±0.3V, V <sub>DD</sub> = 5V		0.1		%
		VCO <sub>IN</sub> = 5V ±2.5V, V <sub>DD</sub> = 10V		0.6		%
		VCO <sub>IN</sub> = 7.5V ±5V, V <sub>DD</sub> = 15V		0.8		%
<b>ZENER DIODE</b>						
V <sub>Z</sub>	Zener Diode Voltage	I <sub>Z</sub> = 50 μA	6.3	7.0	7.7	V
R <sub>Z</sub>	Zener Dynamic Resistance	I <sub>Z</sub> = 1 mA		100		Ω

Note 5: AC Parameters are guaranteed by DC correlated testing.

### Phase Comparator State Diagrams

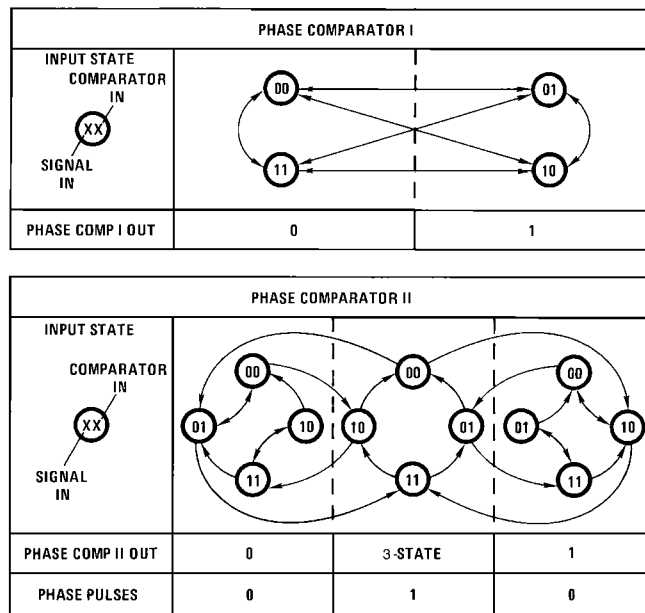


FIGURE 2.

Typical Waveforms

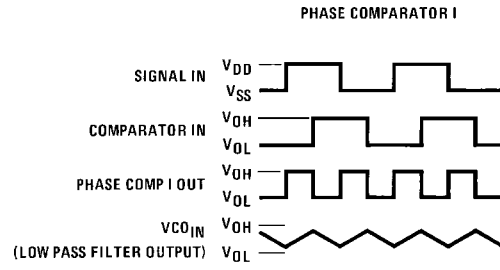


FIGURE 3. Typical Waveform Employing Phase Comparator I in Locked Condition

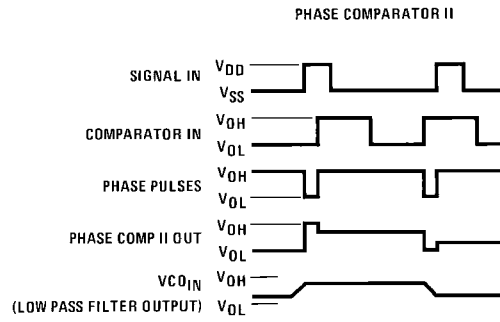


FIGURE 4. Typical Waveform Employing Phase Comparator II in Locked Condition

Typical Performance Characteristics

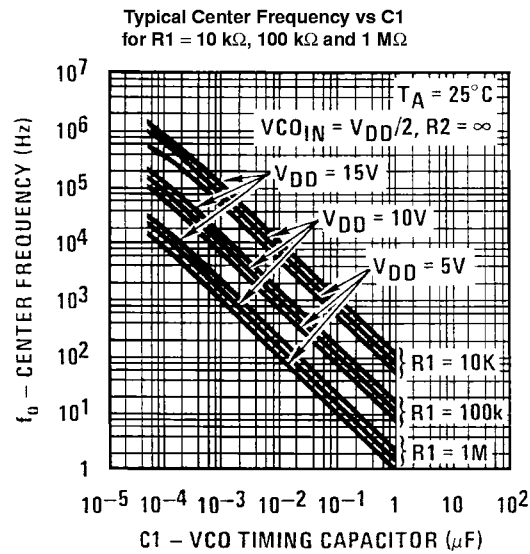


FIGURE 5.

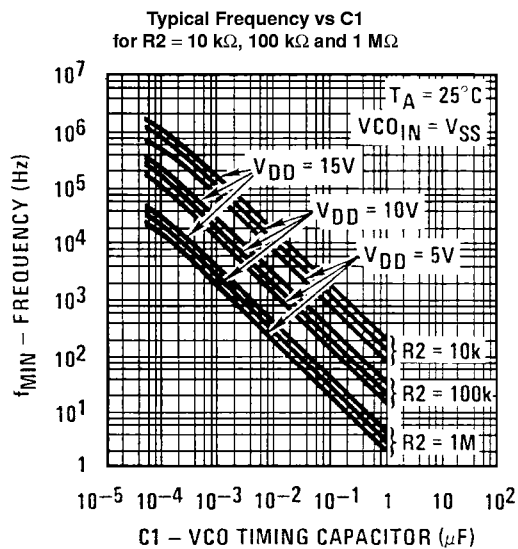


FIGURE 6.

Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I,  $P_D (Total) = P_D (f_0) + P_D (f_{MIN}) + P_D (R_S)$ ; Phase Comparator II,  $P_D (Total) = P_D (f_{MIN})$ .

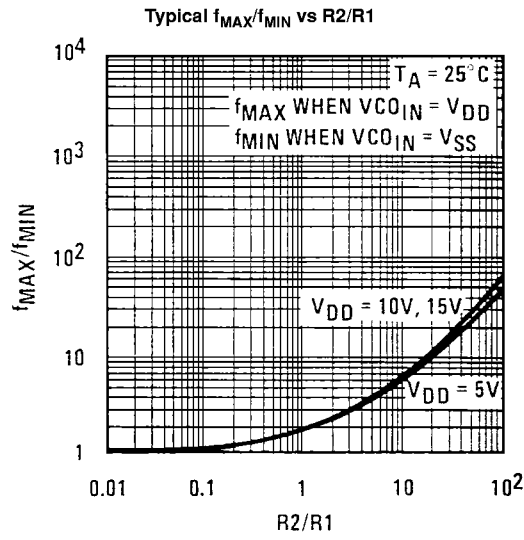


FIGURE 7.

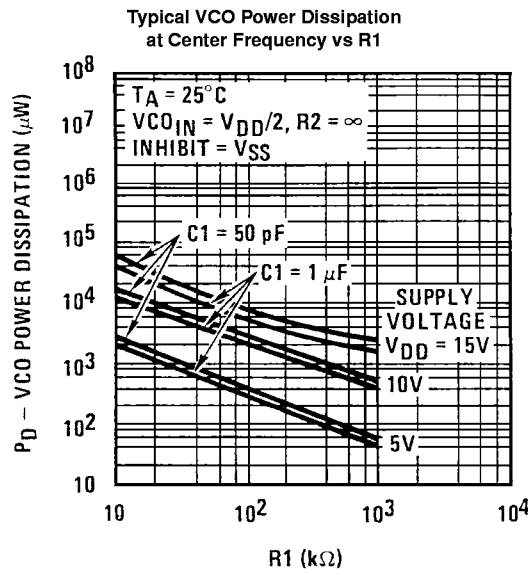


FIGURE 8.

Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I,  $P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S)$ ; Phase Comparator II,  $P_D (Total) = P_D (f_{MIN})$ .

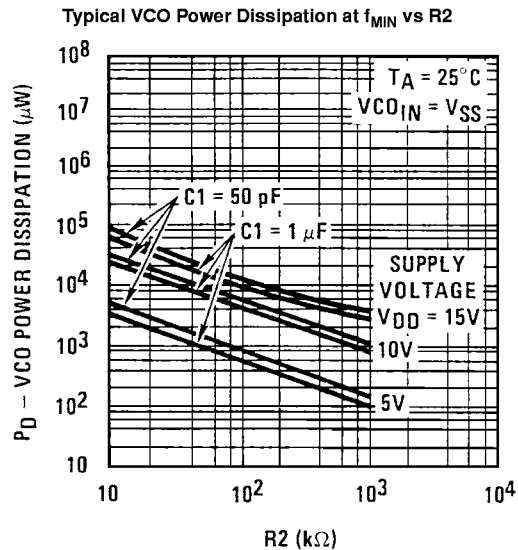


FIGURE 9.

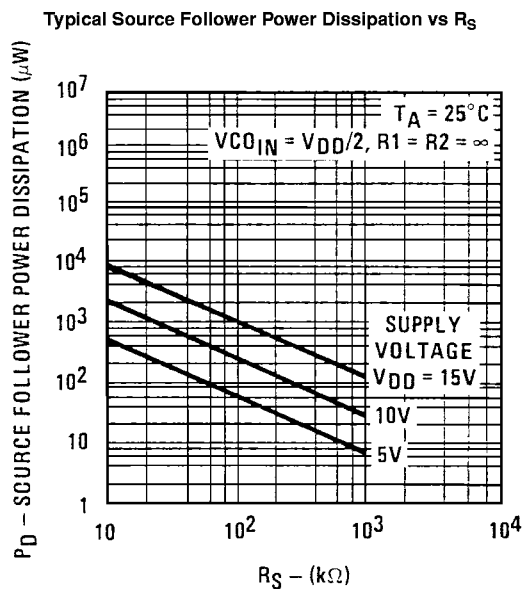


FIGURE 10.

Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I,  $P_D(\text{Total}) = P_D(f_b) + P_D(f_{MIN}) + P_D(R_S)$ ; Phase Comparator II,  $P_D(\text{Total}) = P_D(f_{MIN})$ .

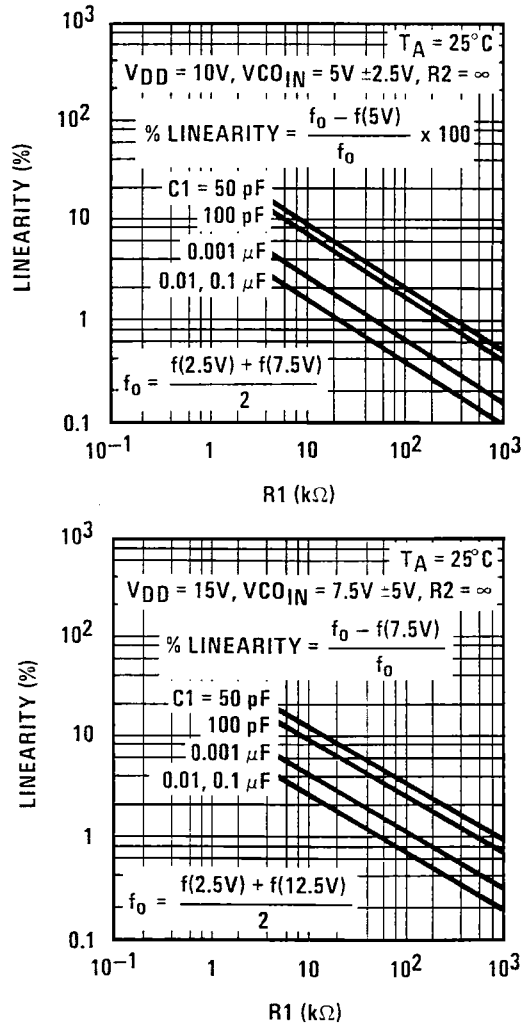


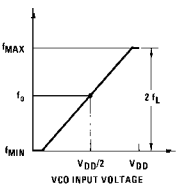
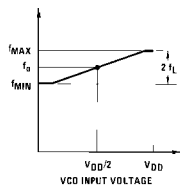
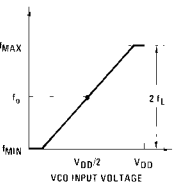
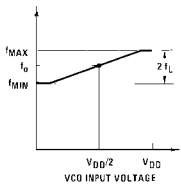
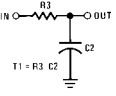
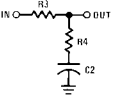
FIGURE 11. Typical VCO Linearity vs R1 and C1

Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I,  $P_D(\text{Total}) = P_D(f_0) + P_D(f_{MIN}) + P_D(R_S)$ ; Phase Comparator II,  $P_D(\text{Total}) = P_D(f_{MIN})$ .

## Design Information

This information is a guide for approximating the value of external components for the CD4046B in a phase-locked-loop system. The selected external components must be within the following ranges: R1, R2 ≥ 10 kΩ, R<sub>S</sub> ≥ 10 kΩ, C1 ≥ 50 pF.

In addition to the given design information, refer to Figure 5, Figure 6, Figure 7 for R1, R2 and C1 component selections.

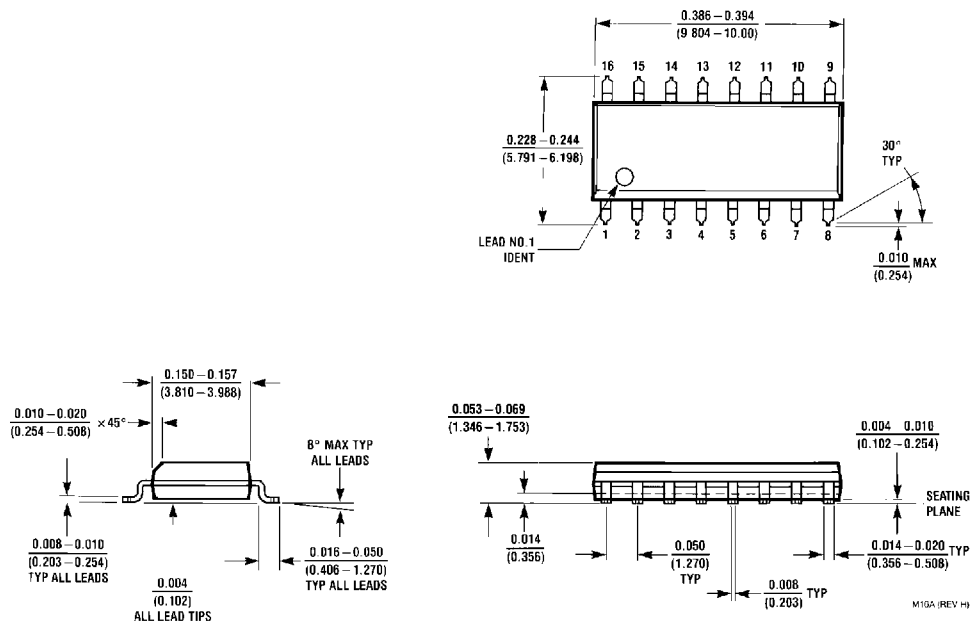
Characteristics	Using Phase Comparator I		Using Phase Comparator II	
	VCO Without Offset R2 = ∞	VCO With Offset	VCO Without Offset R2 = ∞	VCO With Offset
VCO Frequency				
For No Signal Input	VCO in PLL system will adjust to center frequency, f <sub>0</sub>		VCO in PLL system will adjust to lowest operating frequency, f <sub>min</sub>	
Frequency Lock Range, 2 f <sub>L</sub>	2 f <sub>L</sub> = full VCO frequency range 2 f <sub>L</sub> = f <sub>max</sub> - f <sub>min</sub>			
Frequency Capture Range, 2 f <sub>C</sub>		$2 f_C \approx \frac{1}{\pi} \sqrt{\frac{2 \pi f_L}{\tau 1}}$		
Loop Filter Component Selection		For 2 f <sub>C</sub> , see Ref.	f <sub>C</sub> = f <sub>L</sub>	
Phase Angle Between Single and Comparator	90° at center frequency (f <sub>0</sub> ), approximating 0° and 180° at ends of lock range (2 f <sub>L</sub> )		Always 0° in lock	
Locks on Harmonics of Center Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	

Characteristics	Using Phase Comparator I		Using Phase Comparator II	
	VCO Without Offset R2 = ∞	VCO With Offset	VCO Without Offset R2 = ∞	VCO With Offset
VCO Component Selection	<p>Given: <math>f_o</math>. Use <math>f_o</math> with Figure 5 to determine R1 and C1.</p>	<p>Given: <math>f_o</math> and <math>f_L</math>. Calculate <math>f_{min}</math> from the equation <math>f_{min} = f_o - f_L</math>.</p> <p>Use <math>f_{min}</math> with Figure 6 to determine R2 and C1.</p> <p>Calculate <math>\frac{f_{max}}{f_{min}}</math> from the equation <math>\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}</math>.</p> <p>Use <math>\frac{f_{max}}{f_{min}}</math> with Figure 7 to determine ratio R2/R1 to obtain R1.</p>	<p>Given: <math>f_{max}</math>. Calculate <math>f_o</math> from the equation <math>f_o = \frac{f_{max}}{2}</math>.</p> <p>Use <math>f_o</math> with Figure 5 to determine R1 and C1.</p>	<p>Given: <math>f_{min}</math> and <math>f_{max}</math>. Use <math>f_{min}</math> with Figure 6 to determine R2 and C1.</p> <p>Calculate <math>\frac{f_{max}}{f_{min}}</math></p> <p>Use <math>\frac{f_{max}}{f_{min}}</math> with Figure 7 to determine ratio R2/R1 to obtain R1.</p>

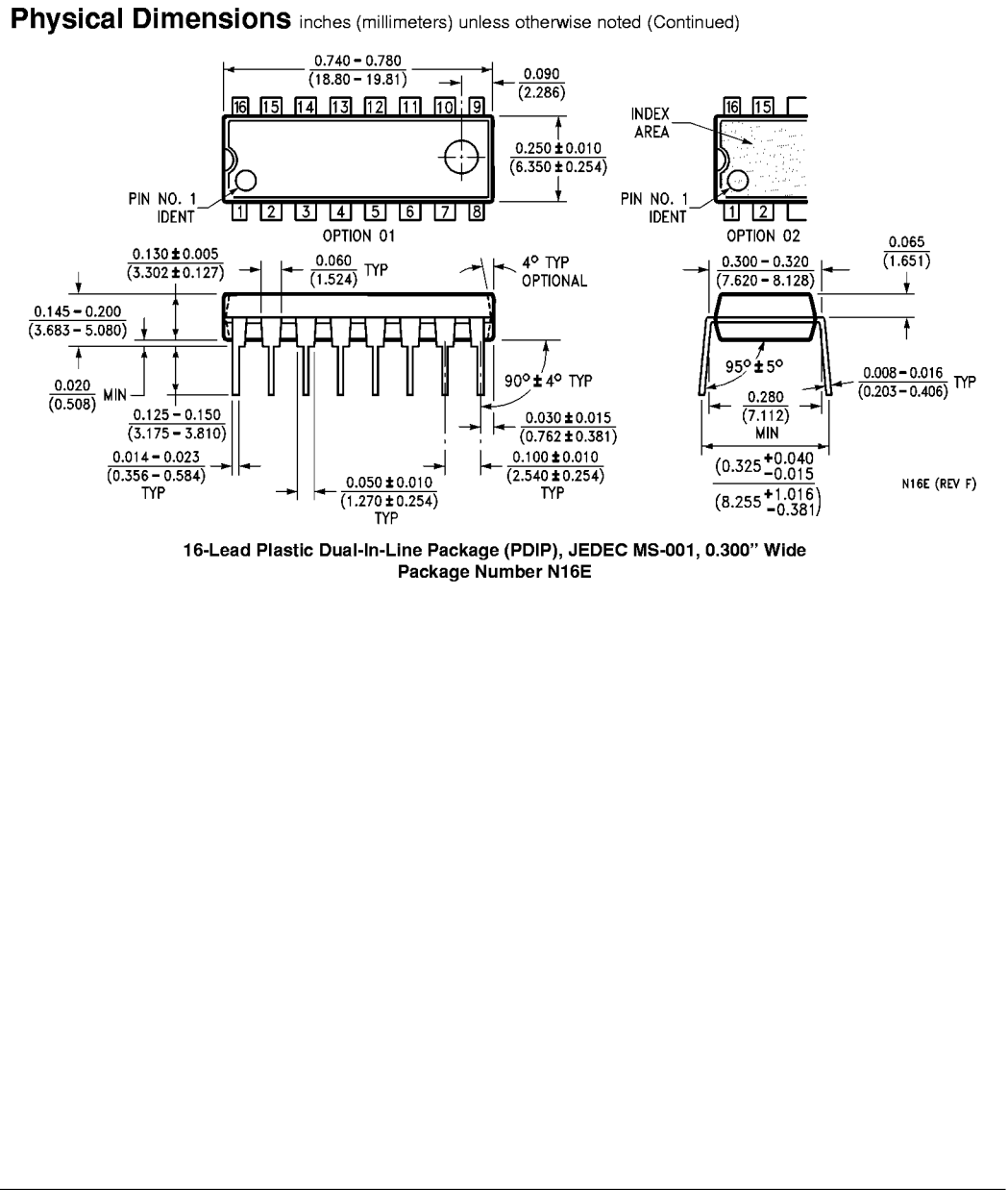
**References**

G.S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.  
 Floyd Gardner, "Phaselock Techniques", John Wiley & Sons, 1966.

**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body  
Package Number M16A**



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