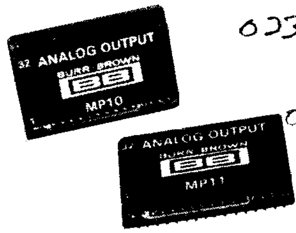
BURR-BROWN®

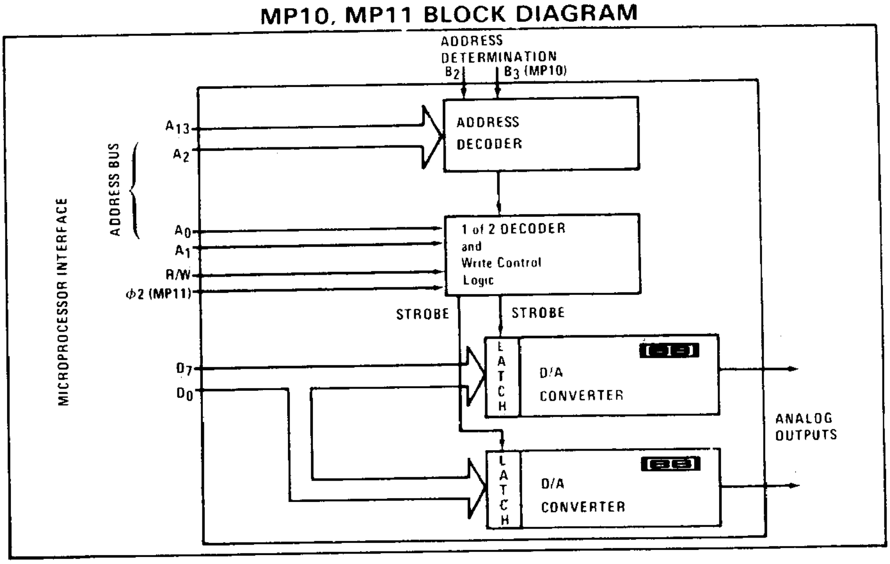


MP10
MP11

MP10/11

Microprocessor-Interfaced
8-BIT ANALOG OUTPUT SYSTEM

MP10, MP11 BLOCK DIAGRAM



FEATURES

- USE AS ANALOG INPUT AND OUTPUT
- EASY TO USE
  - Completely compatible with most microprocessors
  - No external logic required
  - Timing compatible
  - Memory-mapped
- SAVES DEVELOPMENT MONEY AND TIME
- COMPLETELY SELF-CONTAINED
- COMPATIBLE WITH:
  - 8080 (Intel)
  - 9080A (AMD)
  - Z-80 (Zilog)
  - 6800 (Motorola)
  - 8008 (Intel)
  - F-8 (Fairchild)
  - SC/MP (National)
  - 650X (MOS Technology)

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DESCRIPTION

These microprocessor peripherals provide an analog interface compatible with most microprocessors. The MP10 and MP11 are electrically and functionally microprocessor-compatible in static or dynamic situations.

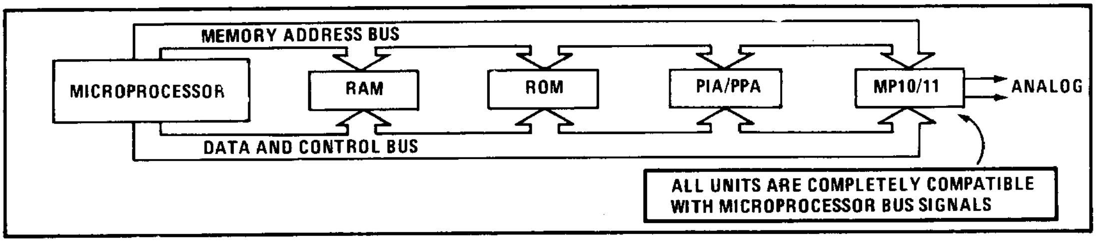
These units are complete analog systems packaged in 32-pin triple-wide dual-in-line packages. They contain two 8-bit D/A converters which are internally trimmed for gain and offset so that no external trimming is required. All necessary interface, timing and address decoding logic is also included.

The MP10 is designed to be used with 8080A and 8008 type microprocessors. It can be used with SC/MP if pull-up resistors are added to the address bus, with the F-8 Dynamic or Static memory interface chip if the RAM WRITE signal is a minimum of 430nsec and with the Z-80 if t_w (ϕH) = t_w (ϕL) = 500nsec. The MP11 is designed to be used with 6800 and 650X type microprocessors.

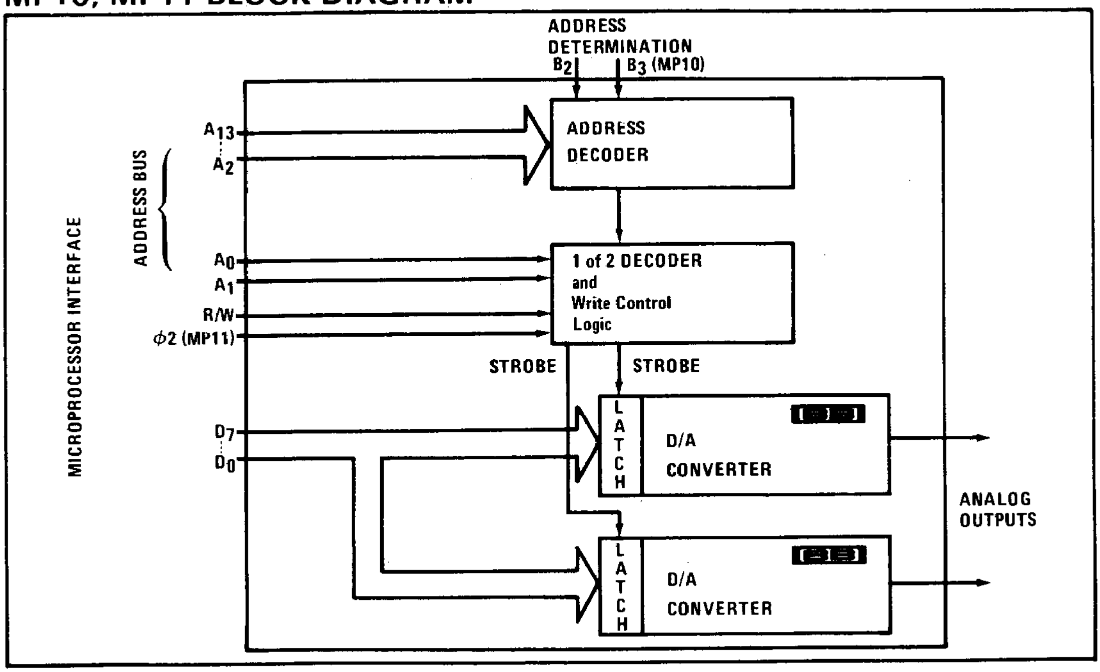
The address lines A_2 through A_{13}, B_2 and B_3 of the MP10 are CMOS compatible so that they can be directly connected to the address bus of an 8080 or 8008. All other input lines require standard TTL voltages. The address lines A_2 through A_{13} and B_2 of the MP11 are LSTTL compatible so they can be directly connected to the address bus of a 6800 or 650X. All other input lines require standard TTL voltages but are high impedance and require only microamp drive currents.

THEORY OF OPERATION

When programming these peripherals, the user treats them as memory. Because the D/A converter input is an 8 bit word, one 8 bit memory location is required for each channel. Since these units are treated as memory, a single instruction is all that's needed to write to an output channel. For instance, when the MP10 is used with an 8080, a single instruction, SHLD, can be used to output data to both D/A converter channels from the H and L register pair. Likewise, when the MP11 is used with the 6800 or 650X, a single STX instruction can be used to output data to both D/A converter channels from the index register. The MP10 and the MP11 require an initialization as would any programmable peripheral.



MP10, MP11 BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

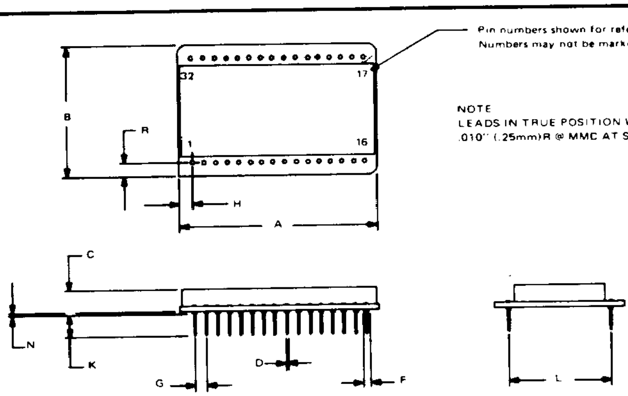
(Typical at 25°C and rated supplies unless otherwise noted.)

	MP10/MP11
ANALOG OUTPUT	
Number of analog outputs	2
Output voltage range	±10V
Output impedance	1Ω
Output settling time	25μsec
TRANSFER CHARACTERISTICS	
Resolution	8 bit binary (complementary binary)
One LSB	78.1mV
Throughput accuracy (max)	±0.4% FSR[1,2]
Throughput accuracy (typical)	±0.25% FSR
Temperature coefficient of accuracy	±0.008% FSR/°C

	MP10/MP11
DIGITAL INPUT/OUTPUT	
All signals compatible with the microprocessor bus	
An analog output channel selected by:	A0
Input data bits read by:	D0 - D7
POWER REQUIREMENTS	
	+5VDC ±5% at 90 mA
	+15V ±3% at 30 mA
	-15V ±3% at 30 mA
TEMPERATURE RANGE	
Operating temperature range	0°C to 70°C
Storage temperature range	-55°C to +85°C

1. FSR is Full Scale Range = 20V.
2. Accuracy components are: Linearity Error = ±0.2% FSR; Gain Error = ±0.1% FSR, Offset Error = ±0.1% FSR.

MECHANICAL SPECIFICATIONS



Pin numbers shown for reference only. Numbers may not be marked on package.

NOTE
LEADS IN TRUE POSITION WITHIN .010" (.25mm)R @ MMC AT SEATING PLANE.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30

MATERIAL: Ceramic
WEIGHT: 14 grams (0.5 oz)
PINS: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
MATING CONNECTOR: 2302MC (Set of two, 16-pin strips)

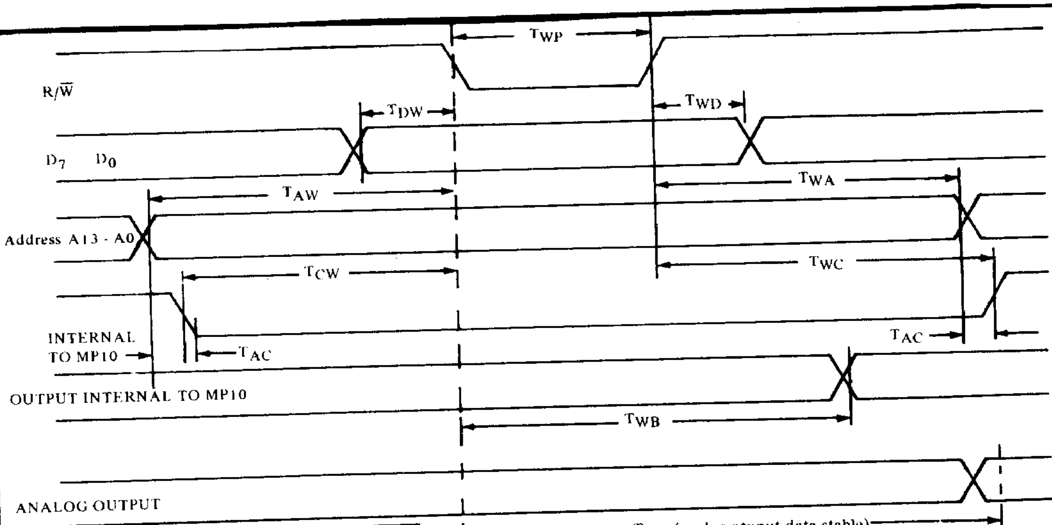
PIN CONNECTIONS

MP10

8080 Pin Connections	Pin	Signal	Signal	Pin	8080 Pin Connections
1	1	A10	A11	32	40
2	2	Common	A13	31	38
3	3	D4	A12	30	37
4	4	D5	A 9	29	35
5	5	D6	A 8	28	34
6	6	D7	A 7	27	33
7	7	D3	A 6	26	32
8	8	D2	A 5	25	31
9	9	D1	A 4	24	30
10	10	D0	A 3	23	29
12	11	Reset	A 2	22	27
18	12	R/$\overline{W}$	B 2	21	—
26	13	A1	B 3	20	—
25	14	A0	+5V	19	20
—	15	+15VDC	Out 1	18	—
—	16	-15VDC	Out 2	17	—

MP11

6800 Pin Connections	Pin	Signal	Signal	Pin	6800 Pin Connections
—	1	Output 1	-15VDC	32	—
—	2	Output 2	+15VDC	31	—
8	3	+5VDC	R/$\overline{W}$	30	34
37	4	Enable	$\overline{Reset}$	29	40
9	5	A0	D0	28	33
10	6	A1	D1	27	32
11	7	A2	D2	26	31
12	8	A3	D3	25	30
13	9	A4	D4	24	29
14	10	A5	D5	23	28
15	11	A6	D6	22	27
16	12	A7	D7	21	26
17	13	A8	Common	20	21
18	14	A9	B2	19	—
19	15	A10	A13	18	23
20	16	A11	A12	17	22



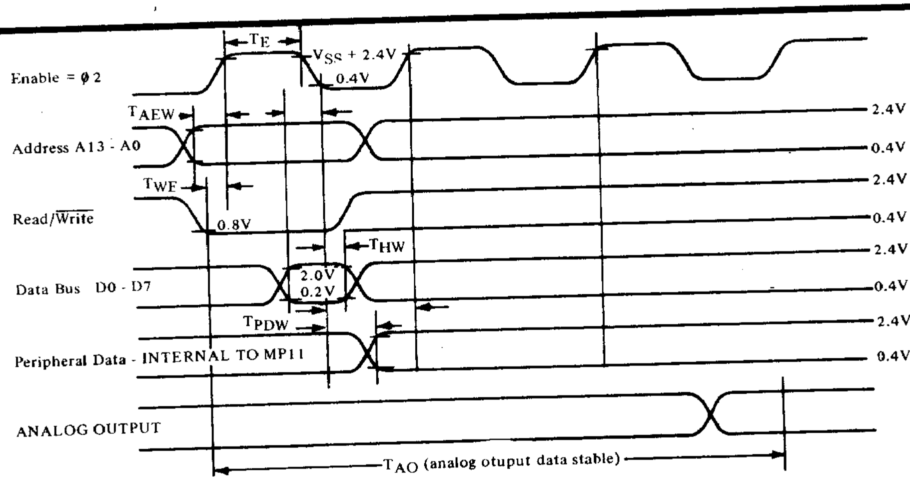
Symbol	Min	Max	Units
T_{WP}	430	—	ns
T_{DW}	100	—	ns
T_{WD}	65	—	ns
T_{AW}	620	—	ns
T_{WA}	35	—	ns
T_{WD}	30	—	ns
T_{WC}	35	—	ns
T_{WB}	—	635	ns
T_{AO}	16	25	µs
T_{AC}	—	600	ns

FOR THE 8080 ITSELF

$T_{AW} = 2tcy - t_{D3} - t_{R42} - 140ns$

$T_{AW} = 670ns$ Min

FIGURE 1. MP10 Timing Diagram.



Symbol	Min	Max	Unit
T_E	0.450	25	µs
T_{AEW}	180	—	ns
T_{DSU}	300	—	ns
T_{WE}	130	—	ns
T_{HW}	10	—	ns
T_{PDW}	—	1.0	µs
T_{AO}	17	25	µs

FIGURE 2. MP11 Timing Diagram.

PROGRAMMING

These units are easily programmed since all are treated as memory locations. They use any memory reference instruction that can write data from internal registers or the accumulator. A single instruction can be used to write data to one or both channels. When the MP10 is used with an 8080, a single SHLD instruction referenced to the lower of the two addresses will automatically transfer the data in the H register to DAC1 and the data in the L register to DAC2. An STA instruction will transfer the data in the accumulator to either DAC. When the MP11 is used with a 6800, a single STX instruction referenced to the lower of the two addresses will automatically transfer the eight upper bits of the index register to DAC1 and the eight lower bits to DAC2. An STAA instruction will transfer the contents of the accumulator to either DAC. Of course, if direct addressing is not desired, MOV instructions may be used to transfer data from internal registers to a specific DAC memory location. As with any programmable peripheral, the MP10 and MP11 must be initialized.

MP10 INITIALIZATION

The RESET input controls the status of the control register of the MP10. An active high on this line will reset the control register to all "zeros".

The MP10 will require initialization every time RESET is activated. If RESET is connected to ground, the MP10 must be initialized only once before output of the data.

MP10 INITIALIZATION SEQUENCE:

1. Load initialization address
2. Load initialization data

MP10 INITIALIZATION ADDRESS:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X	X	1	1	1	1	1	1	1	1	1	1	a	a	1	1

(A_3, A_2: User Defined)

X = don't care, not connected to MP10
1 = True

MP10 INITIALIZATION DATA

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1	0	0	0	0	0	0	0	$= 80_{16}$

For 8080 the sequence may look as follows:

LXI H, ADDR; ADDR = Initialization address
Loads H & L registers with initialization address

MVI M, DATA; DATA = 80
Loads initialization data (80_{16}) to initialization address

The initialization sequence assigns internal registers to function as input registers for the D/A converters. Now data can be written into the MP10. This is accomplished by outputting the correct MP10 address:

	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
OUTPUT 1	1	1	1	1	1	1	1	1	1	1	a	a	0	0
OUTPUT 2	1	1	1	1	1	1	1	1	1	1	a	a	0	1

(A_3, A_2: User Defined)

The B_2 and B_3 inputs determine the address to which the MP10 will respond. The four memory locations which are possible are outlined below:

B_2	B_3	A_2	A_3
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

At the time that the address appears on the address bus, data will appear on the data bus and a R/W pulse will be generated by the microprocessor. After 25μsec, the analog voltage will be stable at the selected output. Timing requirements shown in Figure 1 must be satisfied in order for the MP10 to be initialized and operate correctly. These timing requirements are completely compatible with the 8080.

MP11 INITIALIZATION

The RESET input controls the status of the control and peripheral registers of the MP11. The initialization sequence will differ if RESET is connected to a master reset line of a microprocessor or if it is hard-wired to V_{cc}. The MP11 will require initialization every time the RESET line is activated low. If the RESET line is hard wired to V_{cc}, the MP11 must be initialized only once before output of the data is attempted.

MP11 ADDRESS STRUCTURE

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X	X	1	1	1	1	1	1	1	1	1	1	0	a	Y	Y

A_{15}, A_{14} - don't care, not connected to MP11
A_2 - Address is user selectable
A_0, A_1 - Addresses control the initialization sequence

MP10/11

Initialization sequence when $\overline{RESET}$ is hard wired to V_{cc}:

1. Load accumulator with "zeros"
2. Store accumulator at memory locations:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
X	X	1	1	1	1	1	1	1	1	1	1	0	a	1	0	Address of Control register A

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
X	X	1	1	1	1	1	1	1	1	1	1	0	a	1	1	Address of Control register B

3. Load accumulator with "ones"
4. Store accumulator at memory locations:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
X	X	1	1	1	1	1	1	1	1	1	1	0	a	0	0	Address of Peripheral register A
X	X	1	1	1	1	1	1	1	1	1	1	0	a	0	1	Address of Peripheral register B
X	X	1	1	1	1	1	1	1	1	1	1	0	a	1	0	Address of Control register A
X	X	1	1	1	1	1	1	1	1	1	1	0	a	1	1	Address of Control register B

For the 6800 this sequence can be written as follows:

	LDAA	"zeros"	Loads Zeros in accumulator
	STAA	Address of control register A	Stores zero's in C.R.A.
	STAA	Address of control register B	Stores zero's in C.R. B
	LDAA	"ones"	Loads one's in accumulator
	STAA	Address of peripheral register A	Stores one's in P.R.A
	STAA	Address of peripheral register B	Stores one's in P.R.B.
	STAA	Address of control register A	Stores one's in C.R.A
	STAA	Address of control register B	Stores one's in C.R.B
Or as:	LDX	# $0000	Loads zero's in index register
	STX	$ Address control register A	Stores zero's in C.R. A and B
	LDX	# $1111	Loads one's in index register
	STX	$ Address peripheral register A	Stores one's in P.R. A and B
	STX	$ Address control register A	Stores one's in C.R. A and B

Initialization sequence when $\overline{RESET}$ line is connected to master reset (control registers A and B are always set to zero after master reset and only ones need to be stored in the registers):

LDAA	"ones"
STAA	Address Peripheral register A
STAA	Address Peripheral register B
STAA	Address Control register A
STAA	Address Control register B

or as:

LDXX	# $1111
STX	$ Address Peripheral register A
STX	$ Address Control register A

Now data can be written into MP11. This is accomplished by outputting the correct MP11 address:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
X	X	1	1	1	1	1	1	1	1	1	1	0	a	0	0	OUTPUT 1
X	X	1	1	1	1	1	1	1	1	1	1	0	a	0	1	OUTPUT 2

At the time that the address appears on the address bus, data will appear on the data bus, and if the R W and Enable pulses are correctly timed, 25μsec from the true address the analog voltage will be stable at the selected output.

Timing requirements shown in Figure 1 must be satisfied for the MP11 to be initialized and operate correctly. All timing requirements are completely compatible with 6800 microprocessors. User definable address line A_2 used in conjunction with the B_2 input allows the user to place the MP11 in two different memory locations or use two different MP11's in order to expand the analog system to four outputs. When B_2 is wired to logical 1, the MP11 responds to an A_2 address of 0 and when B_2 is wired to a logical 0, the MP11 responds to an A_2 address of 1.

TEST PROGRAMS

The test circuit and test programs following allow the user to test the operation of the MP10 or MP11. The test may be conducted by setting up the MP10/MP11 as shown in Figure 3. The microprocessor system should have a teletype/CRT terminal interface. The programs will step through several output voltage levels for each DAC output (see Figure 4). Notice how the software is different for the two test programs to illustrate two software approaches.

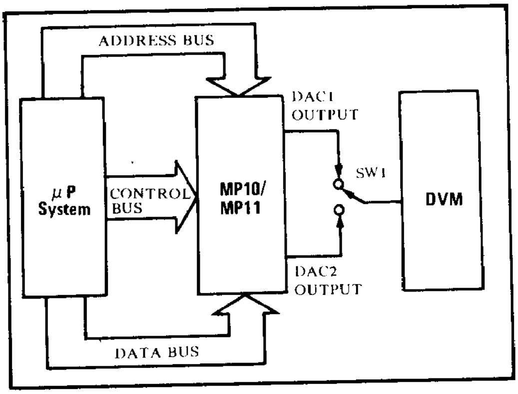


FIGURE 3. Test Circuit for MP10/MP11.

MP10 Test Program

```
              Initialize MP10
         LXI H ADDR X      Address of the first
                           byte of data.
LOOP 1  ┌►MOV A, M         Load ACC with first byte
        │                  of data.
        │ STA ADDR2        Output to MP10 DAC1
        │ INX H            Increment ADDR1
        │ CALL CI   )      Call Input routine
        │ CPI       }      Wait for any character
        │ 8D        )      except carriage return
        └─JNZ LOOP1
          LXI ADDR X
LOOP 2  ┌►MOV A, M
        │ STA ADDR3        Output to MP10 DAC2
        │ INX H            Increment ADDR1
        │ CALL CI   )
        │ CPI       }      Wait for any character
        │ 8D        )      except carriage return
        └─JNZ LOOP2
          RET
```

The MP10 test program will output five different voltages from DAC1 and then from DAC2 (see Figure 4). DAC1 will initially output -10V. To step through the other values for DAC1 enter any character other than carriage return (CR). To transfer control to DAC2, enter CR. DAC2 will output -10V. To step through the other values for DAC2 enter any character except CR. To exit the test program, enter CR.

Store the following codes in memory beginning with location ADDR X:

```
ADDR X     ← FF
ADDR X + 1 ← BF
ADDR X + 2 ← 7F
ADDR X + 3 ← 3F
ADDR X + 4 ← 00
```

ADDR 2 is the address of output 1, ADDR 3 is the address of output 2:

MP11 Test Program

```
                              Initialize MP11
     LDX   # $ FFFF;          Load index register
     STX   ADDR 1;            Store FF in each DAC
     JSR   INP
     LDX   # $ BFBF;          Load index register
     STX   ADDR 1;            Store BF in each DAC
     JSR   INP
     LDX   # $ 7F7F;          Load index register
     STX   ADDR 1;            Store 7F in each DAC
     JSR   INP
     LDX   # $ 3F3F;          Load index register
     STX   ADDR 1;            Store 3F in each DAC
     JSR   INP
     LDX   # $ 0000;          Load index register
     STX   ADDR 1;            Store 00 in each DAC
     JSR   INP
INP  LDAA    ADDR X           Load Status )  Wait for
                              of ACIA     }  TTY
     Bit A   #01                          )  input
     BEQ     INP
     LDA A   ADDR X + 1       Load Data   )
                              From ACIA   )
     CMP     A                            )  Jump back
     8D                                   }  to test
     BNE     Back                         )  program or
     JMP     Return                       )  return to
BACK RTS                                     main program
```

The MP11 test program will output -10V from both DAC1 and DAC2 then wait for an input from the TTY. Any character except CR will advance both DAC's of the MP11 to the next value as defined in Figure 4. CR terminates test program by jumping to RETURN.

ADDR 1 is the address of output 1, ADDR X is the address of the ACIA.

Step	Ideal Output	Actual Output Limits
1	-10V	-9.922V to -10.078V
2	-5.0V	-4.922 to -5.078
3	0.000V	-0.078 to +0.078
4	+5.0V	+4.972 to +5.078
5	+9.922V	+9.844 to +10.000

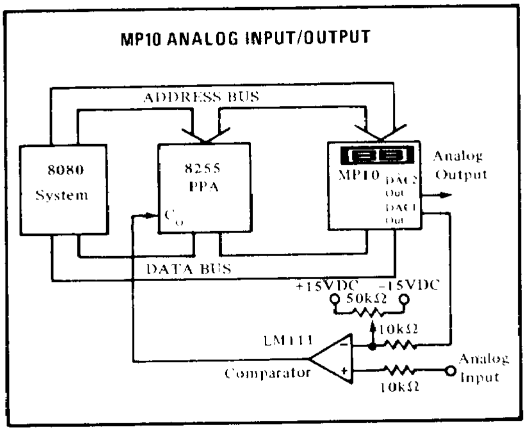
FIGURE 4. Output Voltages for Test Programs.

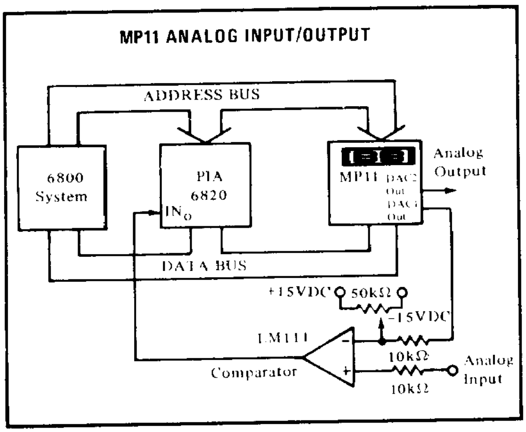
APPLICATIONS

ANALOG INPUT AND ANALOG OUTPUT

Although the MP10 and MP11 are analog output peripherals, they can be easily adapted to provide both analog inputs and outputs.

With the addition of a few external components, these units can each provide one analog input and one analog output for your system as shown below.

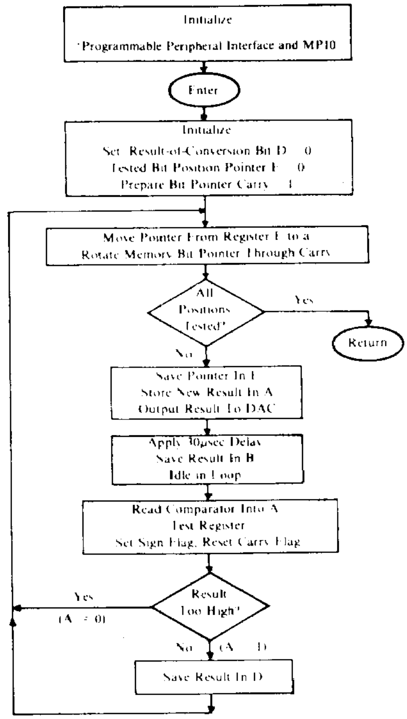




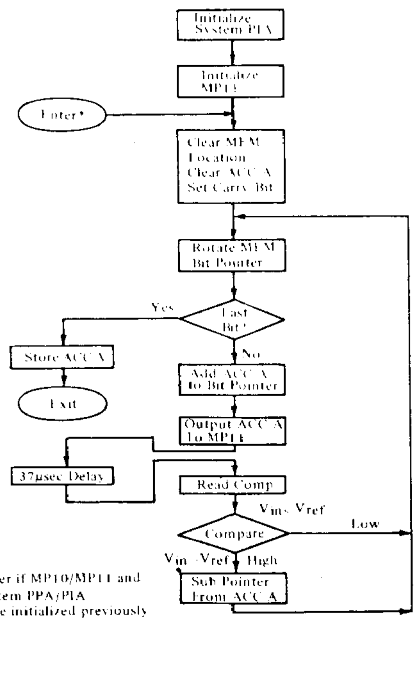
These systems use the microcomputer system to perform the logic of a successive approximation A/D converter, using one channel of the MP10 or MP11 to provide the D/A converter reference function required. In a successive approximation converter, the analog input is compared to known outputs of a D/A converter. First, the microcomputer turns the MSB on, waits for the settling time of the MP10 or MP11, and the switching time of the comparator, then reads the status. If the comparator indicates that the MSB voltage is smaller than the analog input, the MSB input to the MP10/MP11 stays "on" and the next most significant bit is turned on. If the comparator indicates that the MSB value is larger than the analog input, the microcomputer will turn the MSB "off" and turn "on" the next most significant bit. In this way all 8 bits of the D/A converter are tested. When the conversion is complete, the input of the D/A converter will be a digital representation of the analog input. This value will also be stored in the microprocessor's accumulator (complementary binary).

The A/D conversion will require approximately 900 microseconds when performed in this manner. Burr-Brown will shortly have available a detailed application note describing this process including all software required.

FLOWCHART USING 8080 and MP10



FLOWCHART USING 6800 and MP11



* Enter if MP10/MP11 and system PPA/PIA were initialized previously