6. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameters	Symbol	Product names	Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}	μPD77C25		–0.5 to +7.0	V
		μPD77P25			
	V_{PP}	μPD77P25		–0.5 to +13.5	
Input Voltage	V_I	μPD77C25		–0.5 to V_{DD} +0.5	V
		μPD77P25			
	V_{RST}	μPD77P25	RST Pin	–0.5 to +13.0	
Output Voltage	V_O	μPD77C25		–0.5 to V_{DD} +0.5	V
		μPD77P25			
Operating Ambient Temperature	T_A	μPD77C25		–40 to +80	°C
		μPD77P25	Normal operation	–10 to +70	
			PROM mode	+20 to +30	
Storage Temperature	T_{stg}	μPD77C25		–65 to +150	°C
		μPD77P25			

Caution Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

RECOMMENDED OPERATING CONDITIONS

Parameters	Symbol	Product names	Conditions	MIN.	TYP.	MAX.	Unit
Power Supply Voltage	V_{DD}	μPD77C25	Normal operation	4.5	5.0	5.5	V
		μPD77P25					
		μPD77P25	Programming	5.75	6.0	6.25	
	V_{PP}	μPD77P25	Reading and normal operation	4.5	5.0	5.5	
			Programming	12.2	12.5	12.8	
Low Level Input Voltage	V_{IL}	μPD77C25		–0.3		+0.8	V
		μPD77P25					
High Level Input Voltage	V_{IH}	μPD77C25		2.2		V_{DD} +0.3	V
		μPD77P25					
Low Level Clock Input Voltage	V_{ILC}	μPD77C25		–0.3		+0.5	V
		μPD77P25					
High Level Clock Input Voltage	V_{IHC}	μPD77C25		3.5		V_{DD} +0.3	V
		μPD77P25					
Input Voltage for Setting PROM mode	V_{RST}	μPD77P25	Reading and writing	11.5	12.0	12.5	V
Operating Ambient Temperature	T_A	μPD77C25		–40	+25	+85	°C
		μPD77P25	Normal operation	–10		+70	
			PROM mode	+20		+30	

DC CHARACTERISTICS [NORMAL OPERATION] (μPD77C25: T_A = –40 to +85 °C, μPD77P25: T_A = –10 to +70 °C, V_{DD} = 4.5 V to 5.5 V)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Low-level Output Voltage	V_{OL}	I_{OL} = 2.0 mA			0.45	V
High-level Output Voltage	V_{OH}	I_{OH} = –400 μA	0.7 V_{DD}			V
Low-level Input Leak Current	I_{LIL}	V_{IN} = 0 V			–10	μA
High-level Input Leak Current	I_{LIH}	V_{IN} = V_{DD}			10	μA
Low-level Output Leak Current	I_{LOL}	V_{OUT} = 0.47 V			–10	μA
High-level Output Leak Current	I_{LOH}	V_{OUT} = V_{DD}			10	μA
Supply Current (μPD77C25)	I_{DD}	f_{CLK} = 8.192 MHz		25	50	mA
		f_{CLK} = 8.192 MHz, RST = "1"		15	25	mA
Supply Current (μPD77P25)	I_{DD}	f_{CLK} = 8.192 MHz		35	60	mA
		f_{CLK} = 8.192 MHz, RST = "1"		20	35	mA
	I_{PP}				1	mA

DC CHARACTERISTICS [PROM MODE] (T_A = +20 to +30 °C, V_{DD} = 5.75 V to 6.25 V)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Leak Current	I_{RST}	V_{RST} = 12.0 ± 0.5 V			30	μA
Supply Current	I_{DD}				60	mA
	I_{PP}				30	mA

CAPACITANCE (T_A = 25 °C, V_{DD} = 0 V)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLK, SCK Input Capacitance	C_0	f_C = 1 MHz			20	pF
Input Capacitance	C_{IN}				20	pF
Output Capacitance	C_{OUT}				20	pF

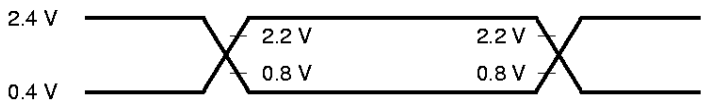
CLOCK TIMING REQUIREMENTS

Clock Timing (μPD77C25: T_A = –40 to +85 °C, μPD77P25: T_A = –10 to +70 °C, V_{DD} = 5 V ±10 %)

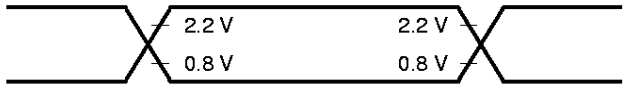
Parameters	Symbol	Product names	Conditions	MIN.	TYP.	MAX.	Unit
CLK Cycle Time	t_{CYC}	μPD77C25	Measuring at 2.0 V	120	122	2000	ns
		μPD77P25					
CLK Pulse Width	t_{CC}	μPD77C25	Measuring at 2.0 V	55			ns
		μPD77P25		60			
CLK Rise Time	t_{CR}	μPD77C25	Measuring at 1.0, 3.0 V			10	ns
		μPD77P25					
CLK Fall Time	t_{CF}	μPD77C25	Measuring at 1.0, 3.0 V			10	ns
		μPD77P25					
SCK Cycle Time	t_{CYS}	μPD77C25		240	244		ns
		μPD77P25					
SCK High Pulse Width	t_{SSH}	μPD77C25		100			ns
		μPD77P25					
SCK Low Pulse Width	t_{SSL}	μPD77C25		100			ns
		μPD77P25					
SCK Rise Time	t_{SR}	μPD77C25				20	ns
		μPD77P25					
SCK Fall Time	t_{SF}	μPD77C25				20	ns
		μPD77P25					

VOLTAGE REFERENCE LEVELS

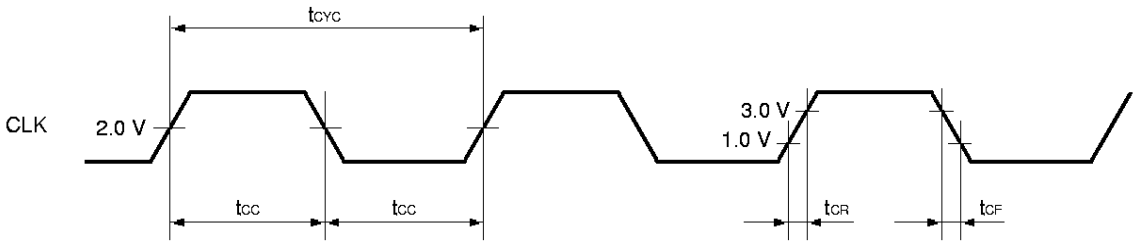
Input

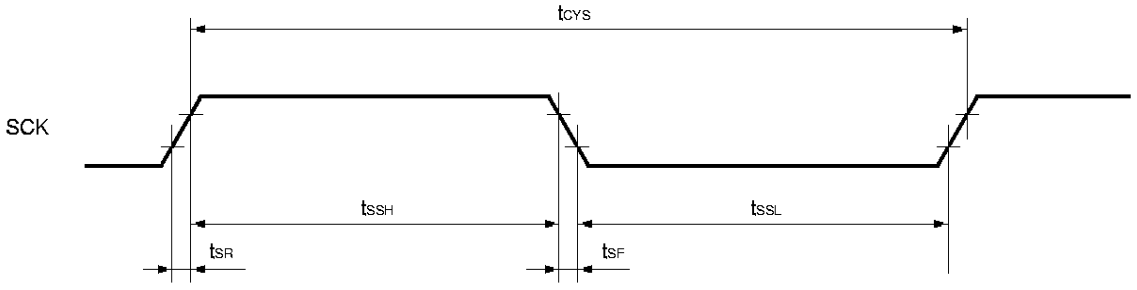


Output



TIMING CHART





HOST INTERFACE TIMING

Timing Requirement (μPD77C25: T_A = –40 to +85 °C, μPD77P25: T_A = –10 to +70 °C, V_{DD} = 5 V ±10 %)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
A0, $\overline{CS}$, $\overline{DACK}$ Setup Time for $\overline{RD}$	t_{SAR}		0			ns
A0, $\overline{CS}$, $\overline{DACK}$ Hold Time for $\overline{RD}$	t_{HRA}		0			ns
$\overline{RD}$ Pulse Width	t_{WRD}		120			ns
A0, $\overline{CS}$, $\overline{DACK}$ Setup Time for $\overline{WR}$	t_{SAW}		0			ns
A0, $\overline{CS}$, $\overline{DACK}$ Hold Time for $\overline{WR}$	t_{HWA}		0			ns
$\overline{WR}$ Pulse Width	t_{WWR}		120			ns
Data Setup Time for $\overline{WR}$	t_{SDW}		100			ns
Data Hold Time for $\overline{WR}$	t_{HWD}		0			ns
$\overline{RD}$, $\overline{WR}$ Recovery Time	t_{RV}		100			ns
$\overline{DACK}$ Hold Time for DRQ	t_{HRQA}		0.5t_{CYC}			ns
$\overline{RD}$, $\overline{WR}$ Setup Time for CLK	t_{SRWC}	**Note**	50			ns
$\overline{RD}$, $\overline{WR}$ Hold Time for CLK	t_{HCRW}	**Note**	50			ns

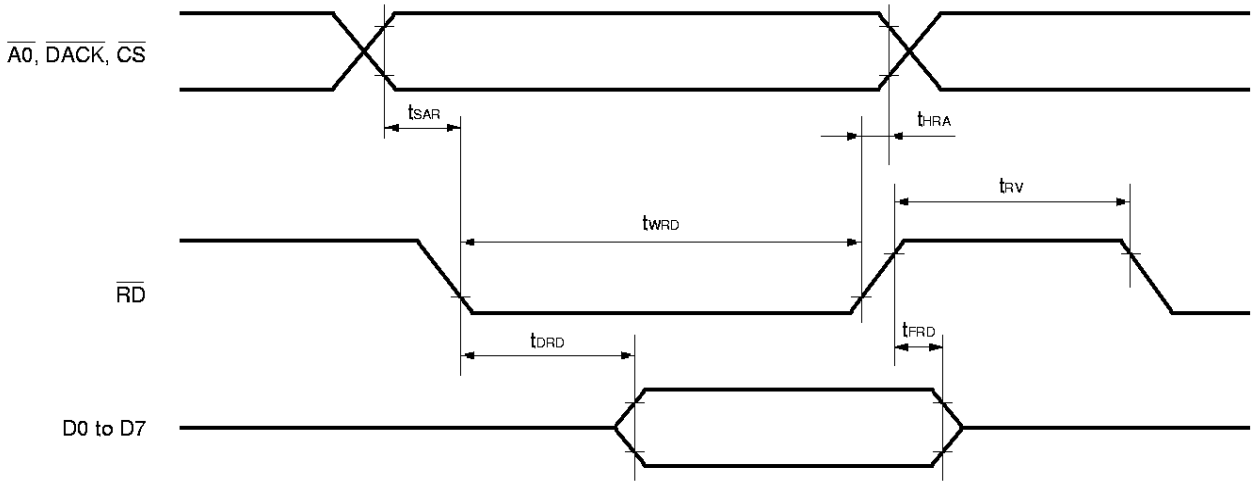
Note Setup and hold requirement for asynchronous signal only guarantee recognition at next CLK.

Switching Characteristics (μPD77C25: T_A = –40 to +85 °C, μPD77P25: T_A = –10 to +70 °C, V_{DD} = 5 V ± 10 %, C_L = 100 pF)

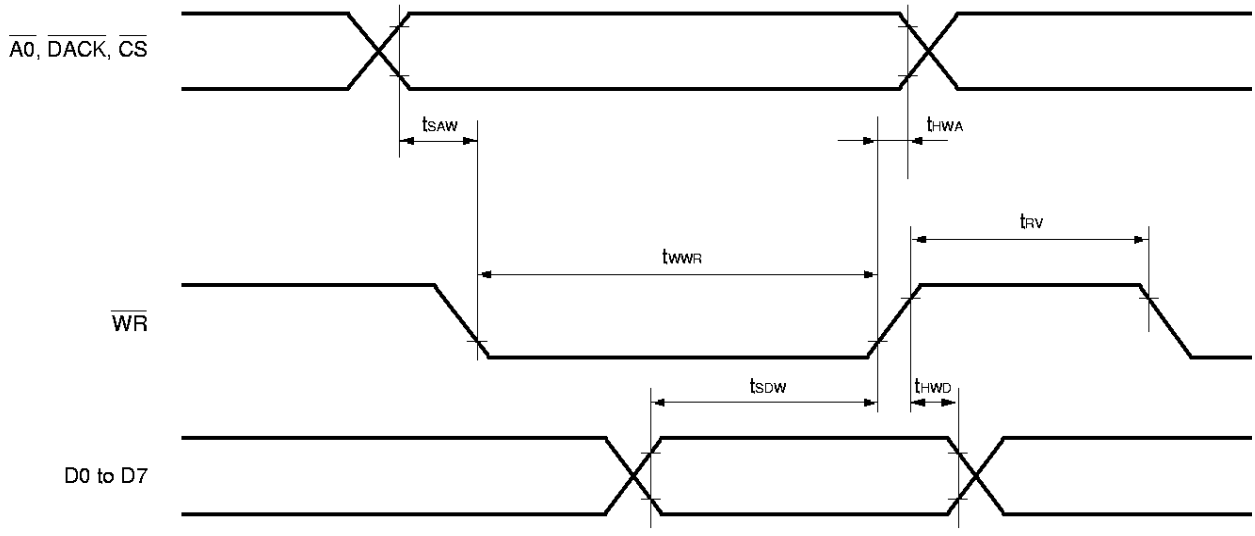
Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{RD}$ ↓ → Data Delay Time	t_{DRD}				100	ns
$\overline{RD}$ ↑ → Data Float Time	t_{FRD}		10		65	ns
CLK ↑ → DRQ Delay Time	t_{DCRQ}				80	ns
$\overline{DACK}$ ↓ → DRQ Delay Time	t_{DARQ}				110	ns
CLK ↑ → P0, P1 Delay Time	t_{DCP}				100	ns

TIMING CHART

Host Read Operation

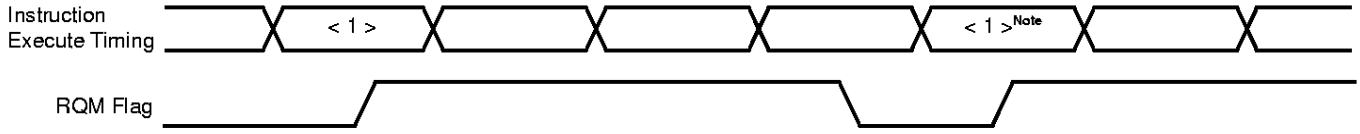


Host Write Operation

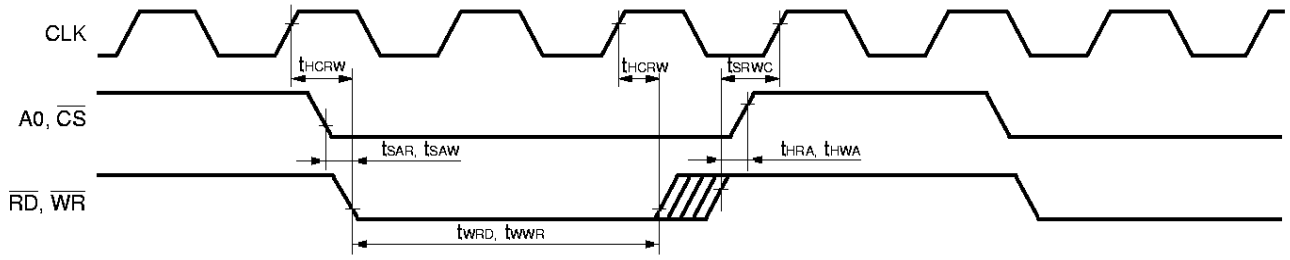


Normal Operation-1 8 bit Mode

Internal Timing

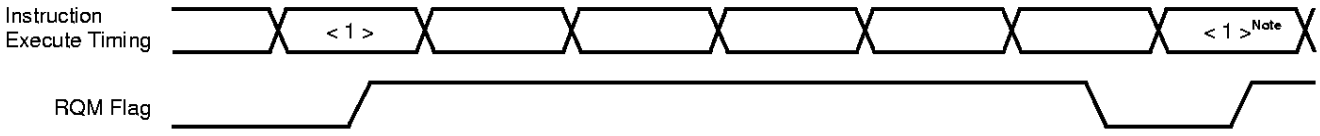


External Timing

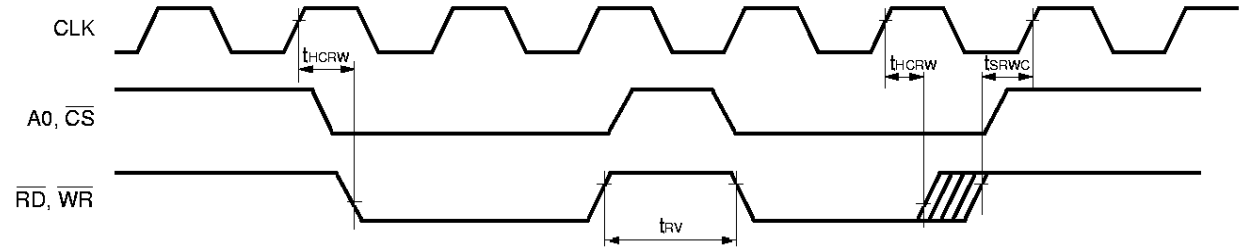


Normal Operation-2 16 bit Mode

Internal Timing



External Timing

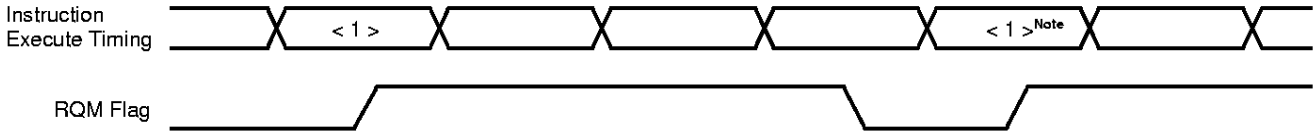


<1> Setting RQM flag to "1" (MOV @DR, xxx or MOV @xxx, DR)

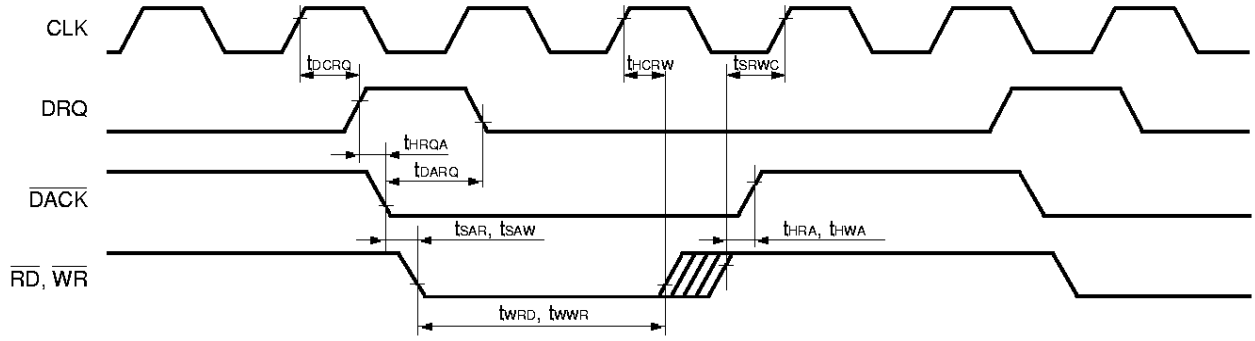
Note The RQM flag is recognized as "0" from this instruction.

DMA Operation-1 8 bit Mode

Internal Timing

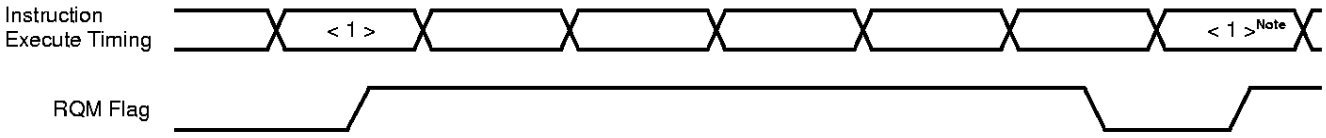


External Timing

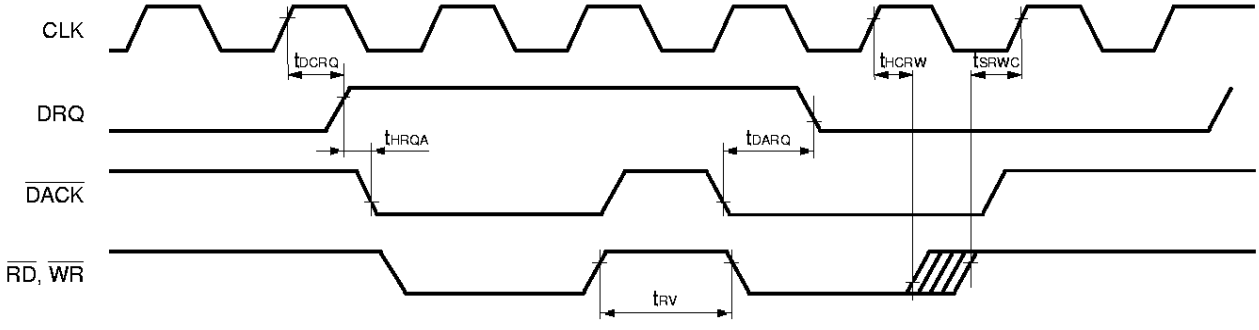


DMA Operation-2 16 bit Mode

Internal Timing



External Timing



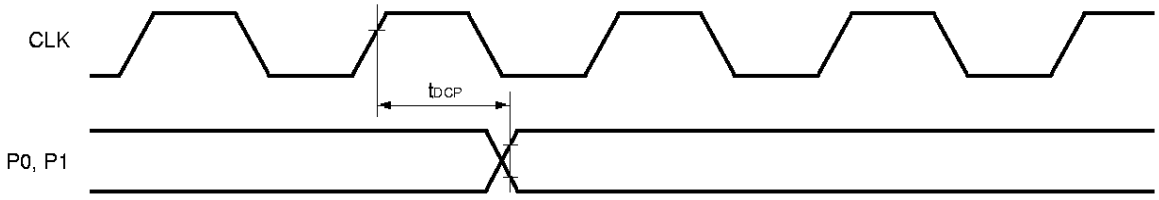
<1> Setting RQM flag to "1" (MOV @DR, xxx or MOV @xxx, DR)

Note The RQM flag is recognized as "0" from this instruction.

Port

Internal Timing

External Timing



<1> Setting P0 or P1 (LDI @SR, I mm)

INTERRUPT RESET TIMING

Timing Requirements (μPD77C25: T_A = –40 to +85 °C, μPD77P25: T_A = –10 to +70 °C, V_{DD} = 5 V ± 10 %)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RST Setup Time for CLK	t_{SRSC}	**Note**	50			ns
RST Hold Time for CLK	t_{HCRS}	**Note**	50			ns
RST Pulse Width	t_{RST}	System reset	$2t_{CYC}$			ns
		enter power saving state	$3t_{CYC}$			
INT Setup Time for CLK	t_{SINC}	**Note**	50			ns
INT Hold Time for CLK	t_{HCIN}	**Note**	50			ns
INT Pulse Width	t_{INT}		$3t_{CYC}$			ns
INT Recovery Time	t_{RINT}		$2t_{CYC}$			ns

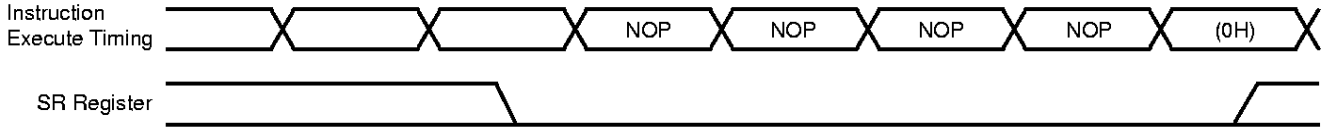
Note Setup and hold requirement for asynchronous signal only guarantee recognition at next CLK.

Switching Characteristics (μPD77C25: T_A = –40 to +85 °C, μPD77P25: T_A = –10 to +70 °C, V_{DD} = 5 V ± 10 %, C_L = 100 pF)

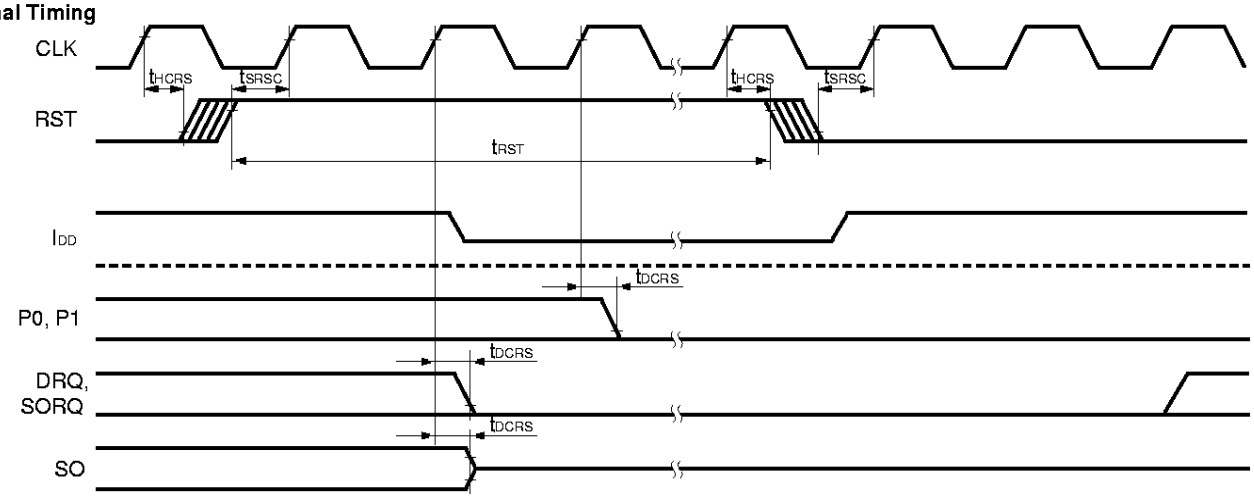
Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLK ↑ → Reset State Delay Time	t_{DCRS}				100	ns

Reset Operation

Internal Timing



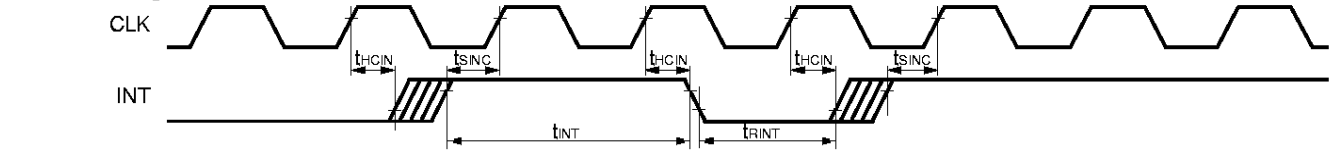
External Timing



Interrupt Operation

Internal Timing

External Timing



<1> Setting EI bit to "1" (LDI @SR, I mm)

Note EI bit can be set to "1" from this instruction.

SERIAL INTERFACE TIMING

Timing Requirements (μPD77C25: T_A = –40 to +85 °C, μPD77P25: T_A = –10 to +70 °C, V_{DD} = 5 V ± 10 %)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SIEN}$, SI Setup Time for SCK	t_{SSIS}		50			ns
$\overline{SIEN}$, SI Hold Time for SCK	t_{HSSI}		30			ns
$\overline{SOEN}$ Setup Time for SCK	t_{SSES}		50			ns
$\overline{SOEN}$ Hold Time for SCK	t_{HSSE}		30			ns
CLK Setup Time for SCK	t_{SCS}	**Note**	50			ns
CLK Hold Time for SCK	t_{HSC}	**Note**	50			ns
SCK Setup Time for CLK	t_{SSC}	**Note**	50			ns
SCK Hold Time for CLK	t_{HCS}	**Note**	50			ns

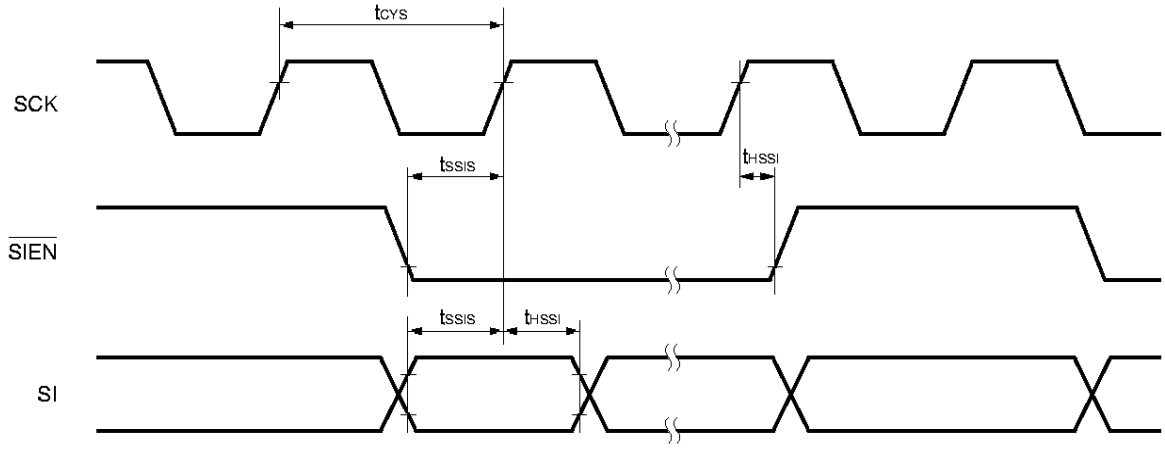
Note Setup and hold requirement for asynchronous signal only guarantee recognition at next CLK.

Switching Characteristics (μPD77C25: T_A = –40 to +85 °C, μPD77P25: T_A = –10 to +70 °C, V_{DD} = 5 V ± 10 %, C_L = 100 pF)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCK ↑ → SORQ Delay Time	t_{DSSQ}		30		150	ns
SCK ↓ → SO Delay Time	t_{DSLSO}				60	ns
SCK ↓ → SO Hold Time	t_{HSLSO}		0			ns
SCK ↓ → SO Float Time	t_{FSSO}				60	ns

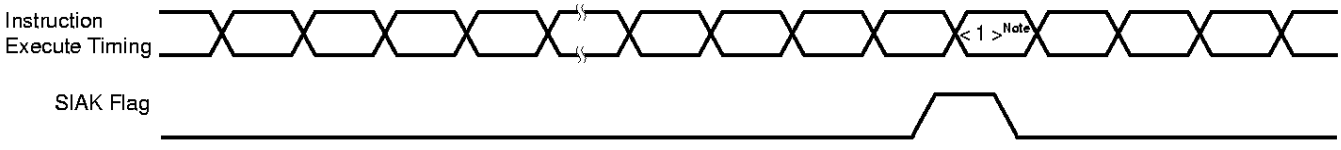
TIMING CHART

Serial Input Operation

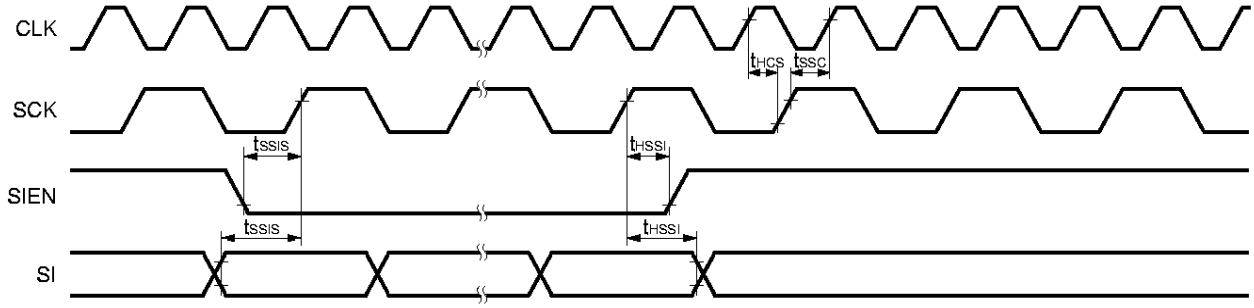


Serial Input Operation

Internal Timing



External Timing

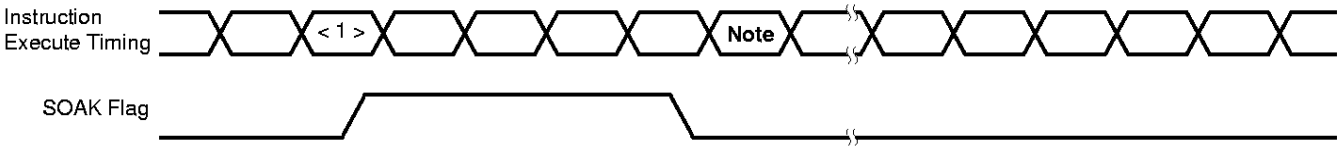


<1> Setting SIAK flag to "0" (MOV @xxx, SI)

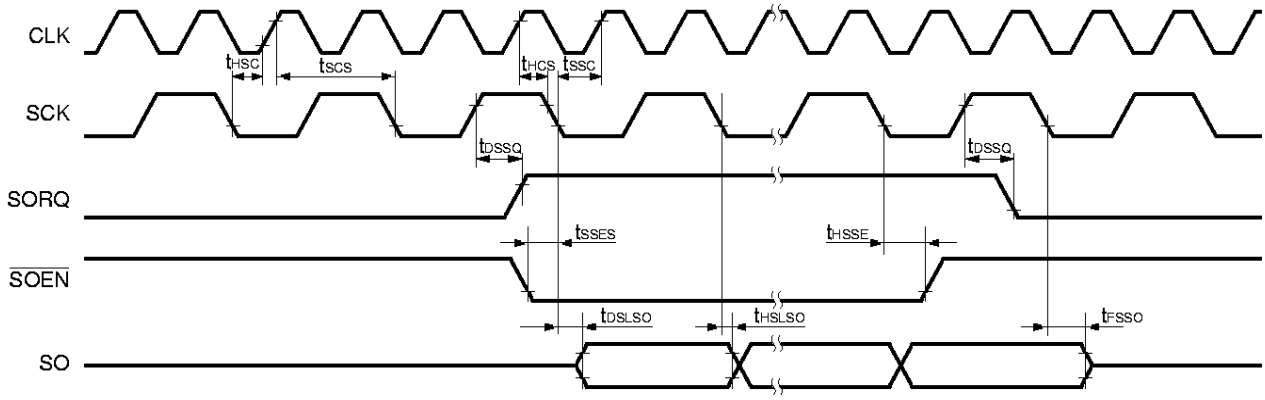
Note The SIAK flag is recognized as "1" from this instruction.

Serial Output Operation

Internal Timing



External Timing

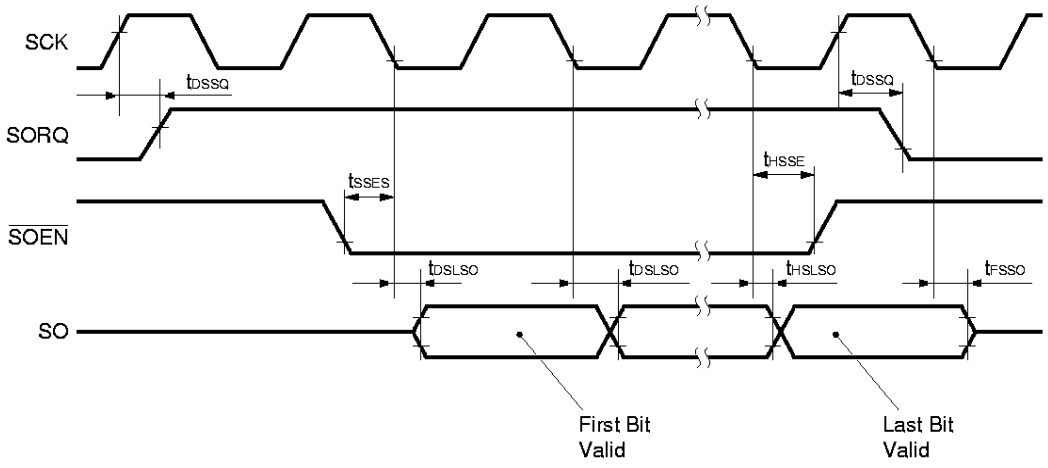


<1> Setting SOAK flag to "1" (MOV @SO, xxx)

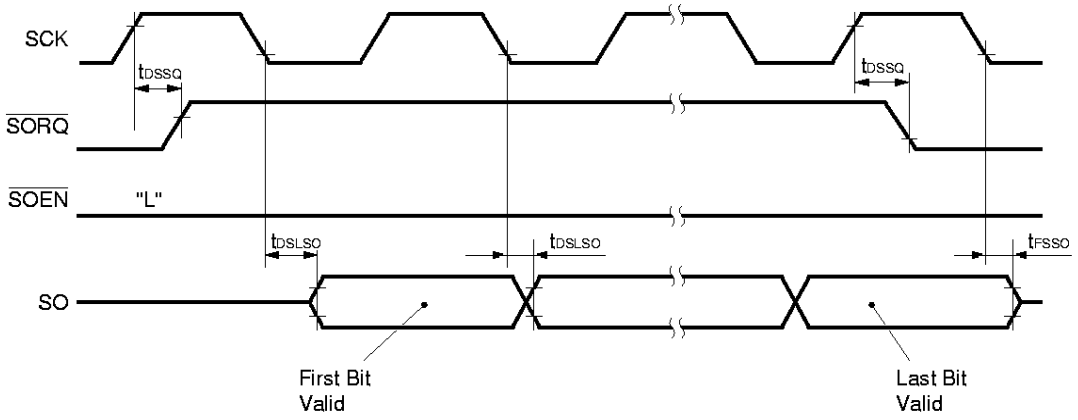
Note The SOAK flag is recognized as "0" from this instruction.

Serial Output Operation

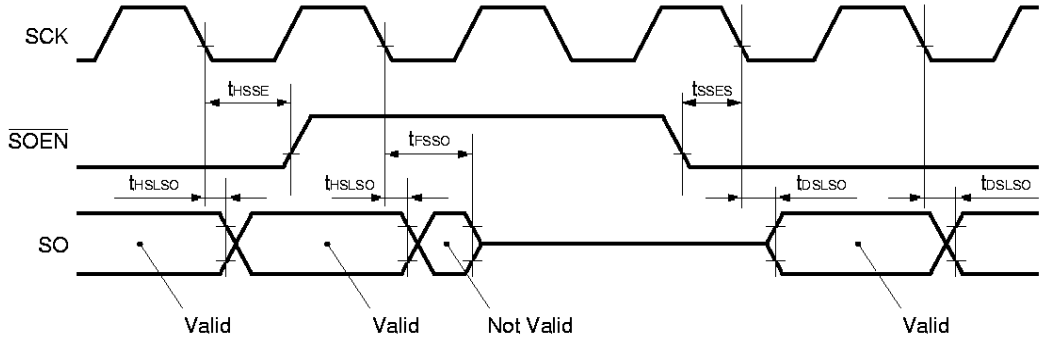
Serial Output Case #1: $\overline{SOEN}$ Asserted in Response to SORQ



Serial Output Case #2: $\overline{SOEN}$ Active before SORQ is High



Serial Output Case #3: if $\overline{SOEN}$ is Released in the Middle of a Transfer



UVPROM PROGRAMMING TIMING

DATA READ TIMING [PROM MODE]

Timing Requirements (T_A = 25 ± 5 °C, V_{DD} = 5.0 ± 0.5 V, V_{PP} = V_{DD}, V_{IHR} = 12.0 ± 0.5 V)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{CE}$ Setup Time for RST	t_{SRSCE}		2			μs
$\overline{OE}$ Setup Time for RST	t_{SRSOE}		2			μs

Switching Characteristics (T_A = 25 ± 5 °C, V_{DD} = 5.0 ± 0.5 V, V_{PP} = V_{DD}, V_{IHR} = 12.0 ± 0.5 V)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Address to Output Delay	t_{DAD}				200	ns
$\overline{CE}$ to Output Delay	t_{DCD}				200	ns
$\overline{OE}$ to Output Delay	t_{DODR}				75	ns
$\overline{OE}$ High to Output Float	t_{FCD}		0		60	ns
Address to Output Hold	t_{HAD}		0			ns

DATA PROGRAM TIMING [PROM MODE]

Timing Requirements (T_A = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{IHR} = 12.0 ± 0.5 V)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{CE}$ Setup Time for RST	t_{SRSCE}		2			μs
$\overline{CE}$ Setup Time for Address	t_{SAC}		2			μs
$\overline{CE}$ Setup Time for Data	t_{SDC}		2			μs
$\overline{CE}$ Setup Time for V_{PP}	t_{SVPC}		2			μs
$\overline{CE}$ Setup Time for V_{DD}	t_{SVDC}		2			μs
$\overline{OE}$ Setup Time for Data	t_{SDO}		2			μs
Address Hold Time	t_{HCA}		2			μs
Data Hold Time	t_{HCD}		2			μs
Initial Program Pulse Width	t_{WC0}		0.95	1.0	1.05	ms
Overprogram Pulse Width	t_{WC1} Note		2.85		78.75	ms

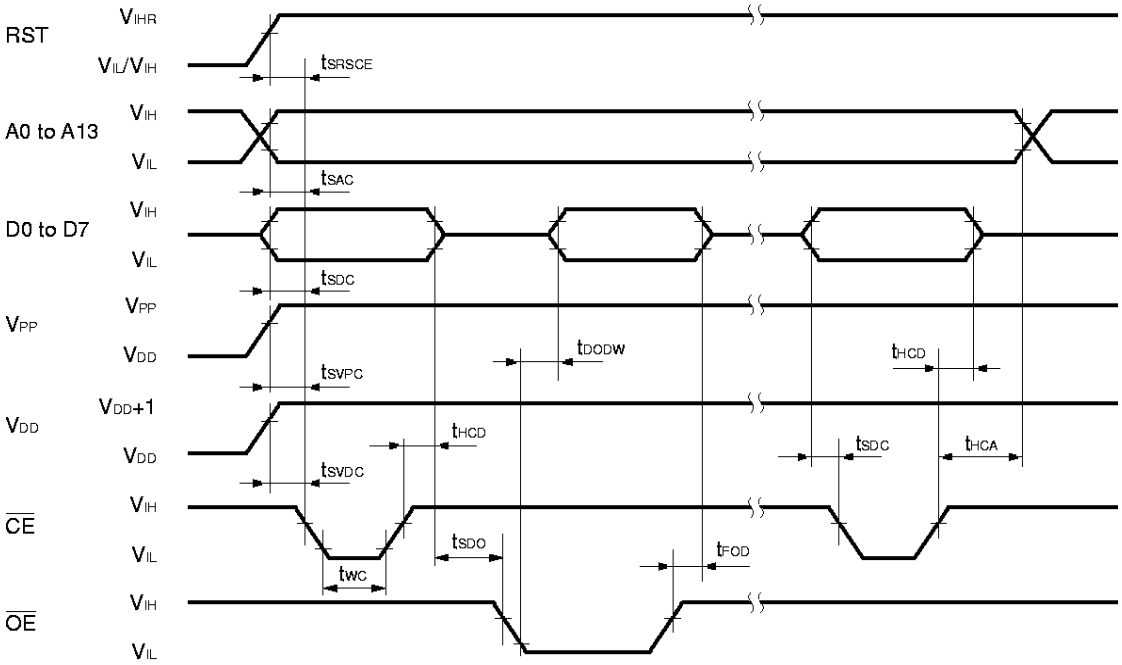
Note t_{WC1} = 3n t_{WC0} assuming initial program pulse is applied n times.

Switching Characteristics (T_A = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{IHR} = 12.0 ± 0.5 V)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{OE}$ to Output Float Time	t_{FOD}		0		130	ns
$\overline{OE}$ to Output Delay	t_{DODW}				150	ns

TIMING CHART

PROM Program Operation



PROM Read Operation