DESCRIPTION

The Hyundai HY57V164010B is a 16,777,216-bits CMOS Synchronous DRAM, ideally suited for the main memory applications which require large memory density and high bandwidth. HY57V164010B is organized as 2banks of 2,097,152x4.

HY57V164010B is offering fully synchronous operation referenced to a positive edge clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

Programmable options include the length of pipeline (Read latency of 1, 2, or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1, 2, 4, 8, or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipeline design is not restricted by a `2N` rule.)

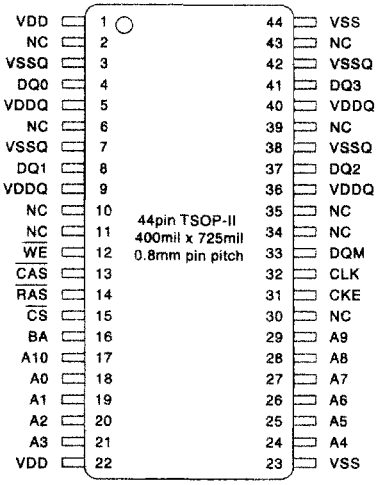
FEATURES

- Single 3.3V ± 0.3V power supply
- All device pins are compatible with LVTTL interface
- JEDEC standard 400mil 44pin TSOP-II with 0.8mm of pin pitch
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by DQM
- Internal two banks operation
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 and Full Page for Sequence Burst
  - 1, 2, 4 and 8 for Interleave Burst
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3 Clocks

ORDERING INFORMATION

Part No.	Clock Frequency	Organization	Interface	Package
HY57V164010BTC-10	100MHz	2Banks x 512Kbits x16	LVTTL	400mil 44pin TSOP II
HY57V164010BTC-12	83MHz			
HY57V164010BTC-15	66MHz			
HY57V164010BLTC-10	100MHz			
HY57V164010BLTC-12	83MHz			
HY57V164010BLTC-15	66MHz			

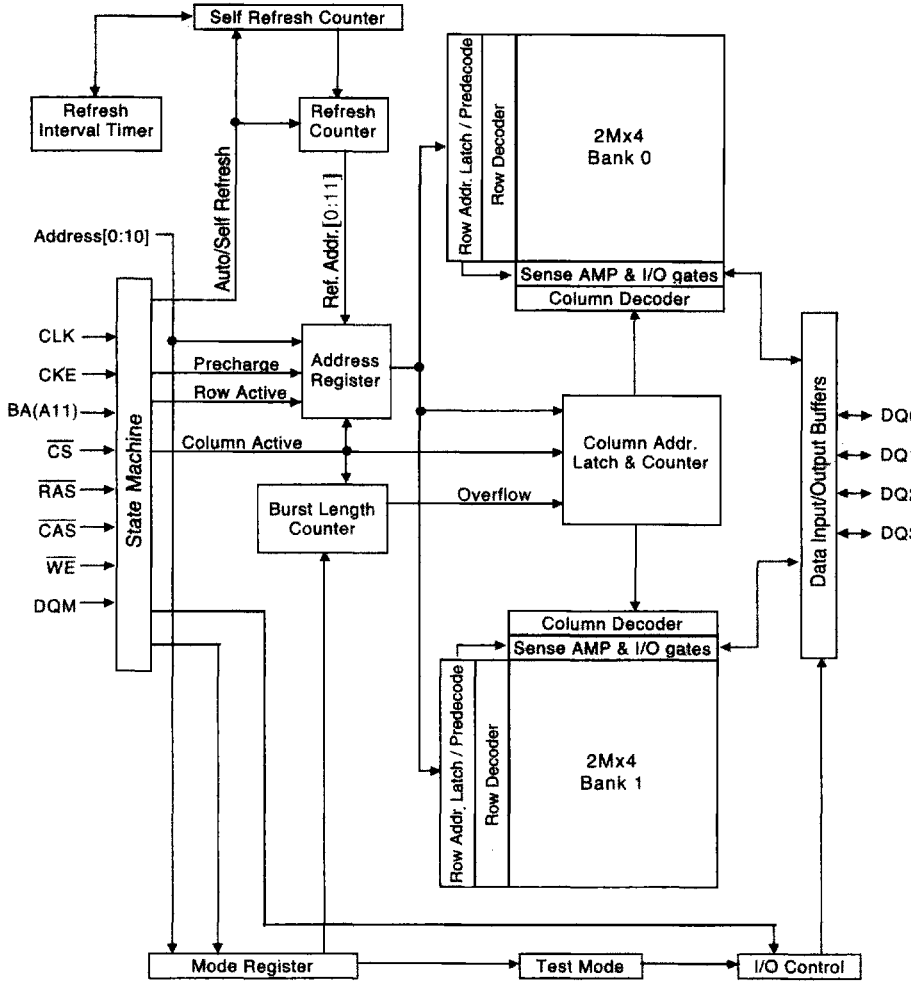
PIN CONFIGURATION



PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are referenced to the SDRAM on the rising edge of CLK.
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh.
$\overline{CS}$	Chip Select	Command input enable or mask except CLK, CKE and DQM
BA	Bank Address	Select either one of banks during both $\overline{RAS}$ and $\overline{CAS}$ activity.
A0 ~ A10	Address	Row Address : RA0 ~ RA10, Column Address : CA0 ~ CA9 Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation. Refer function truth table for details
DQM	Data Input/Output Mask	DQM control output buffer in read mode and mask input data in write mode
DQ0 ~ DQ3	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	*Power Supply/Ground*	*Power supply for internal circuit and input buffer*
VDDQ/VSSQ	Data Output Power/Ground	Power supply for DQ
NC	No Connection	No connection

4Mx4 Synchronous DRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.5 ~ 4.6	V
Voltage on VDD relative to VSS	VDD	-1.0 ~ 4.6	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	1	W
Soldering Temperature·Time	TSOLDER	260·10	°C·Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability.

DC OPERATING CONDITION (TA=0°C to 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	VDD, VDDQ	3.0	3.3	3.6	V	1
Input high voltage	VIH	2.0	3.0	VDD + 0.3	V	1,2
Input low voltage	VIL	-0.5	0	0.8	V	1,3

Note :
1.All voltages are referenced to VSS = 0V.
2.VIH(max) is acceptable 4.6V AC pulse width with ≤ 10ns of duration.
3.VIL(max) is acceptable -1.5V AC pulse width with ≤ 10ns of duration.

AC OPERATING CONDITION (TA=0°C to 70°C, VDD=3.3V ± 0.3V, VSS=0V)

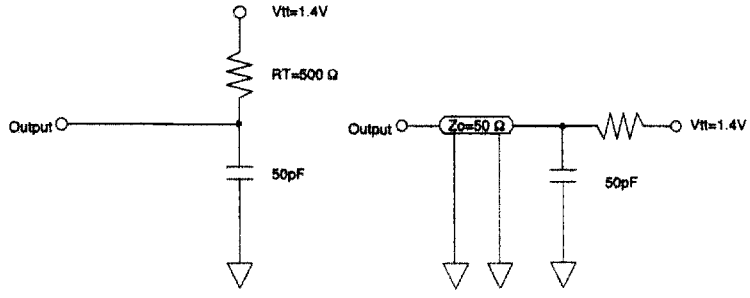
Parameter	Symbol	Value	Unit	Note
AC input high / low level voltage	VIH / VIL	2.4/0.4	V	
Input timing measurement reference level voltage	Vtrip	1.4	V	
Input rise / fall time	tR / tF	1	ns	
Output timing measurement reference level	Voutref	1.4	V	
Output load capacitance for access time measurement	CL	50	pF	1

Note :
1. Output load to measure access times (tAC, tOH, etc) varies to clock frequency.
A load is equivalent to one TTL gate and one capacitance.

CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Pin	Symbol	Max	Unit
Input capacitance	CLK	CI1	5	pF
	A0 ~ A10, BA CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$,DQM	CI2	5	pF
Data input / output capacitance	DQ0 ~ DQ3	CI/O	7	pF

OUTPUT LOAD CIRCUIT



DC Output Load Circuit

AC Output Load Circuit

DC CHARACTERISTICS I (TA=0°C to 70°C, VDD=3.3V ± 0.3V)

Parameter	Symbol	Min.	Max	Unit	Note
Input leakage current	IL	-5	5	uA	1
Output leakage current	IO	-5	5	uA	2
Output high voltage	VOH	2.4	-	V	IOH = -2mA
Output low voltage	VOL	-	0.4	V	IOL = +2mA

Note :
1.VIN = 0 to 3.6V, All other pins are not under test = 0V
2.DOUT is disabled, VOUT=0 to 3.6V

DC CHARACTERISTICS II (TA=0°C to 70°C, VDD=3.3V ± 0.3V, VSS=0V)

Parameter	Symbol	Test Condition		Speed			Unit	Note
				-10	-12	-15		
Operating Current	IDD1	Burst Length=1, One bank active tRAS ≥ tRAS(min), tRP ≥ tRP(min), IO=0mA		100	80	75	mA	1
Precharge Standby Current in power down mode	IDD2P	CKE ≤ VIL(max), tCK = min.		3			mA	
	IDD2PS	CKE ≤ VIL(max), tCK = ∞		2				
Precharge Standby Current in non power down mode	IDD2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = min Input signals are changed one time during 2Clks. All other pins ≥ VDD-0.2V or ≤ 0.2V		20			mA	
	IDD2NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.		15				
Active Standby Current in power down mode	IDD3P	CKE ≤ VIL(max), tCK = min		30			mA	
	IDD3PS	CKE ≤ VIL(max), tCK = ∞		30				
Active Standby Current in non power down mode	IDD3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = min Input signals are changed one time during 2CLKs. All other pins ≥ VDD-0.2V or ≤ 0.2V		50			mA	
	IDD3NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable		30				
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), tRAS ≥ tRAS(min), IO=0mA All banks active	CL=3	100	80	75	mA	1
			CL=2	80	60	55		
Auto Refresh Current	IDD5	tRRC ≥ tRRC(min), All banks active		100	80	75	mA	
Self Refresh Current	IDD6	CKE ≤ 0.2V		2			mA	
				400			uA	L-part

Note :
1.IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open.

AC CHARACTERISTICS I

Paramter		Symbol	-10		-12		-15		Unit	Note
			Min	Max	Min	Max	Min	Max		
System clock cycle time	$\overline{CAS}$ Latency = 3	tCK3	10	-	12	-	15	-	ns	
	$\overline{CAS}$ Latency = 2	tCK2	15	-	18	-	22.5	-		
Clock high pulse width		tCHW	3	-	4	-	5	-	ns	1
Clock low pulse width		tCLW	3	-	4	-	5	-	ns	1
Access time from clock	$\overline{CAS}$ Latency = 3	tAC3	-	8	-	8.5	-	9	ns	
	$\overline{CAS}$ Latency = 2	tAC2	-	9	-	9.5	-	10		
Data-out hold time		tOH	3	-	3	-	3	-	ns	
Data-Input setup time		tDS	3	-	3	-	3	-	ns	1
Data-Input hold time		tDH	1	-	1.5	-	1.5	-	ns	1
Address setup time		tAS	3	-	3	-	3	-	ns	1
Address hold time		tAH	1	-	1.5	-	1.5	-	ns	1
CKE setup time		tCKS	3	-	3	-	3	-	ns	1
CKE hold time		tCKH	1	-	1.5	-	1.5	-	ns	1
Command setup time		tCS	3	-	3	-	3	-	ns	1
Command hold time		tCH	1	-	1.5	-	1.5	-	ns	1
CLK to data output in low Z-time		tOLZ	2	-	2	-	2	-	ns	
CLK to data output in high Z-time	$\overline{CAS}$ Latency = 3	tOHZ3	3	8	3	8.5	3	9	ns	
	$\overline{CAS}$ Latency = 2	tOHZ2	3	9	3	9.5	3	10	ns	

Note :
1.Assume tR / tF (input rise and fall time) is 1ns.
2.Access times to be measured with input signals of 1V/ns edge rate, 0.8V to 2.0V

AC CHARACTERISTICS II

Parameter		Symbol	-10		-12		-15		Unit	Note
			Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ cycle time	Operation	tRC	100	-	108	-	120	-	ns	
	Auto Refresh	tRRC	100	-	108	-	120	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD	30	-	36	-	45	-	ns	
$\overline{RAS}$ active time		tRAS	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ precharge time		tRP	30	-	36	-	45	-	ns	
$\overline{RAS}$ to $\overline{RAS}$ bank active delay		tRRD	20	-	24	-	30	-	ns	
$\overline{CAS}$ to $\overline{CAS}$ bank active delay		tCCD	1	-	1	-	1	-	CLK	
Write command to data-in delay		tWTL	0	-	0	-	0	-	CLK	
Data-in to precharge command		tDPL	1	-	1	-	1	-	CLK	
Data-in to active command		tDAL	4	-	4	-	4	-	CLK	
DQM to data-in Hi-Z		tDQZ	2	-	2	-	2	-	CLK	
DQM to data mask		tDQM	0	-	0	-	0	-	CLK	
MRS to new command		tMRD	2	-	2	-	2	-	CLK	
Precharge to data output Hi-Z	$\overline{CAS}$ Latency = 3	tPROZ3	3	-	3	-	3	-	CLK	
	$\overline{CAS}$ Latency = 2	tPROZ2	2	-	2	-	2	-	CLK	
Power down exit time		tPDE	1	-	1	-	1	-	CLK	
Self refresh exit time		tSRE	1	-	1	-	1	-	CLK	1
Refresh Time		tREF	64	-	64	-	64	-	ms	

Note :
1. A new command can be given tRRC after self refresh exit.

DEVICE OPERATING OPTION TABLE

HY57V164010B-10

	$\overline{CAS}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
100MHz	3CLKs	3CLKs	6CLKs	10CLKs	3CLKs	8ns	3ns
83MHz	3CLKs	3CLKs	5CLKs	9CLKs	3CLKs	8ns	3ns
66MHz	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	9ns	3ns
50MHz	2CLKs	2CLK	3CLKs	5CLKs	2CLKs	9ns	3ns

HY57V164010B-12

	$\overline{CAS}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
83MHz	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	8.5ns	3ns
66MHz	3CLKs	3CLKs	5CLKs	8CLKs	3CLKs	8.5ns	3ns
50MHz	2CLKs	2CLK	4CLKs	6CLKs	2CLKs	8.5ns	3ns

HY57V164010B-15

	$\overline{CAS}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
66MHz	3CLKs	3CLKs	6CLKs	8CLKs	3CLKs	9ns	3ns
50MHz	3CLKs	3CLKs	5CLKs	7CLKs	3CLK	9ns	3ns

COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	CS	RAS	CAS	WE	DQM	A0~A9	A10/AP	BA	Note
Mode Register Set		H	X	L	L	L	L	X	OP code			
No Operation		H	X	H	X	X	X	X	X			
				L	H	H	H					
Bank Active		H	X	L	L	H	H	X	Row Address		V	
Read		H	X	L	H	L	H	X	Column Address	L	V	
Read with Auto precharge										H		
Write		H	X	L	H	L	L	X	Column Address	L	V	
Write with Auto precharge										H		
Precharge All Bank		H	X	L	L	H	L	X	X	H	X	
Precharge selected Bank										L	V	
Burst Stop		H	X	L	H	H	L	X	X			
DQM		H	X					V	X			
Auto Refresh		H	H	L	L	L	H	X	X			
Self Refresh[1]	Entry	H	L	L	L	L	H	X	X			
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Precharge power down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X				X	X			

Note :
1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high.
2. X=Do not care, L=Low, H=High, BA=Bank Address, RA= Row Address, CA=Column Address, Opcode=Operand Code, NOP=No Operation.

PACKAGE INFORMATION

400mil 44pin Thin Small Outline Package (TC)

4Mx4 Synchronous DRAM