TMC2310
FFT Processor
16/19-Bit, 20 MHz

Description

The TMC2310 is an advanced integrated circuit which can execute complex Fast Fourier Transforms (FFT), forward or inverse, of up to 1024 points, with or without data windowing. The device operates with either unconditional or conditional overflow block floating-point rescaling. Adaptive and static Finite Impulse Response filtering, real and complex multiplication or multiply-accumulation, and magnitude squared operations are also supported. Sinusoidal coefficients ("Roots of Unity") for Fourier Transforms are provided in a Coefficient Look-Up Table in on-chip ROM. At the maximum clock rate of 20 MHz, the device will execute radix-2 butterflies in 100 ns, and 1024-point complex transforms (5120 butterflies) in 514 µSec.

The TMC2310 provides the arithmetic, control, coefficient memory and address generation logic for a variety of signal processing and vector algorithms. External memory is used for storage of complex data and window or filter coefficients. Each data port is bidirectional and the device can be used with one or two banks or memory for either in-place or bank switched memory configurations, allowing the user to overlap I/O operations with arithmetic execution. All functions utilize the same basic system architecture, ensuring maximum flexibility.

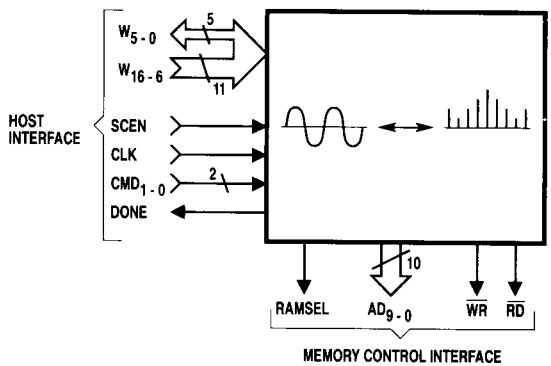
The control structure has been designed to simplify its use as a high-speed arithmetic accelerator. The device is programmed by initializing two internal configuration registers to set device parameters such as function, transform length, data addressing modes, single or bank switching memory architecture, and other options. Once initialized, the device generates data addresses and control for external memory, transfers data, executes the algorithm, and provides a DONE flag to indicate completion.

Built with Raytheon Semiconductor's OMICRON-C™ CMOS process, the TMC2310 is available in 89-pin plastic and 88-pin ceramic pin grid arrays and a 100 leaded ceramic chip carrier.

Features

- Stand alone execution of forward or inverse complex Fast Fourier Transforms, adaptive and non-adaptive FIR filtering, multiplication or multiplication-accumulation (real or complex) magnitude squared
- Fast 100 ns per butterfly yields a 2 MHz to 4 MHz sampling rate in single-device systems (16-point FFT in 4 µsec, 1024-point in 514 µsec)
- Pipelined addressing mode and internal data storage to reduce memory bandwidth
- Multiple-transform array mode to increase throughput
- On-chip ROM coefficient look-up table for FFT coefficients ("Twiddle Factors")
- 16-bit fixed-point data format with 19-bit intermediate and final results for improved precision
- Conditional overflow rescaling or manual scaling (block floating-point) for high signal-to-noise performance
- Scaler (block exponent) output
- User-programmable window functions
- Complete on-chip address generation and control for off-chip data and window/(FIR) coefficient memory

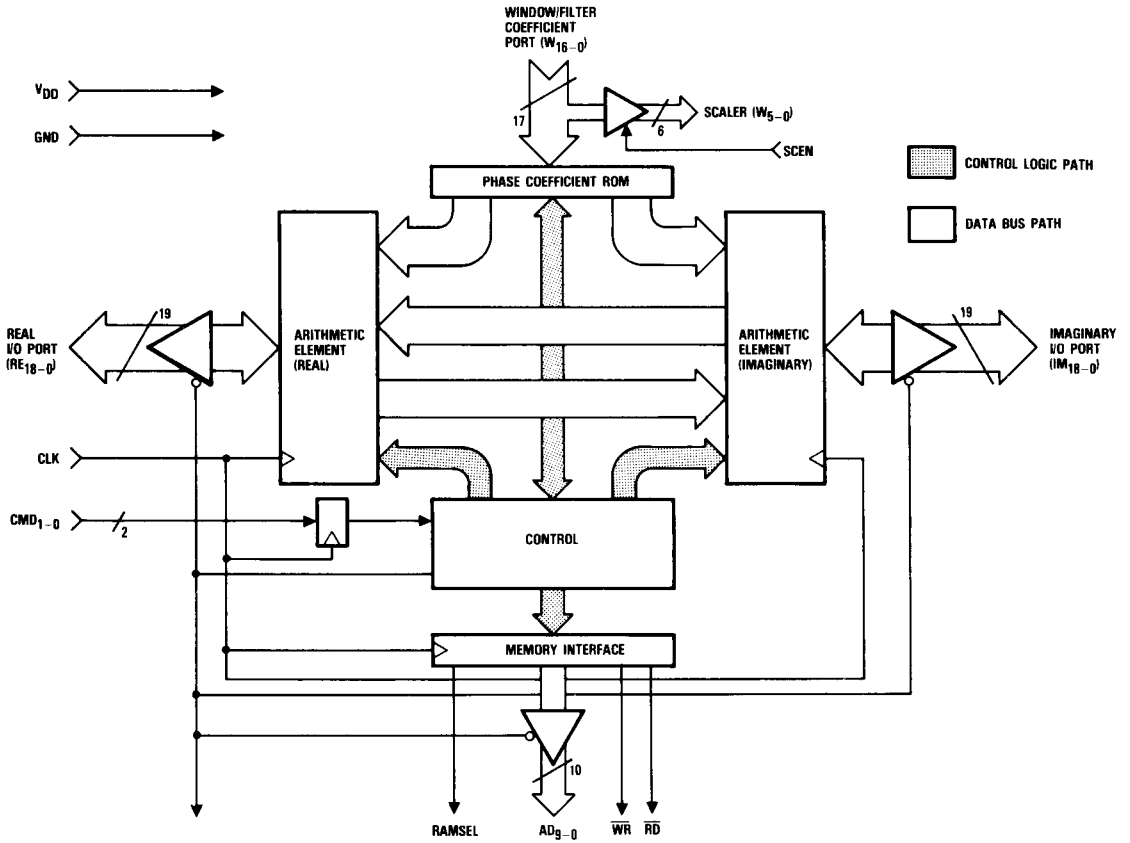
Logic Symbol



Applications

- Radar
- Sonar
- Digital Communications
- High–Speed Modems
- Image Processing, Graphics
- Test Instrumentation
- Medical Electronics
- Spectral Decomposition/Analysis
- Frequency–Multiplex Demodulation
- Adaptive Filtering And Equalization
- Pulse And Image Compression
- Frequency And Time Domain Digital Filtering
- High–Speed Complex Multiplication

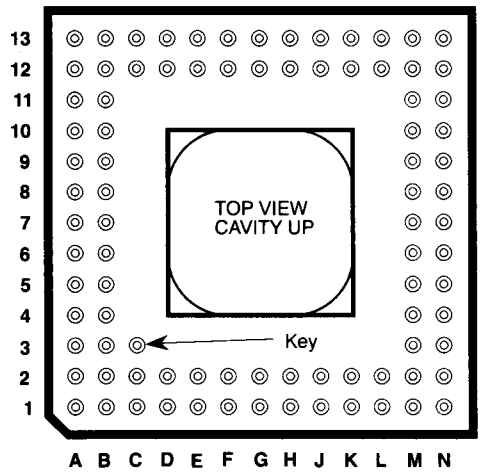
Functional Block Diagram



Pin Assignments — 88 Pin Ceramic (G5) or 89 Pin Plastic (H7) Pin Grid Array

Pin	Name	Pin	Name	Pin	Name	Pin	Name
B1	GND	N2	GND	M13	GND	A12	RE_0
C2	CMD_0	M3	IM_{18}	L12	SCEN	B11	RE_1
C1	CMD_1	N3	IM_{17}	L13	W_0	A11	RE_2
D2	DONE	M4	IM_{16}	K12	W_1	B10	RE_3
D1	RAMSEL	N4	IM_{15}	K13	W_2	A10	GND
E2	RD	M5	IM_{14}	J12	W_3	B9	RE_4
E1	WR	N5	IM_{13}	J13	W_4	A9	RE_5
F2	CLK	M6	IM_{12}	H12	W_5	B8	RE_6
F1	AD_0	N6	IM_{11}	H13	W_6	A8	RE_7
G1	GND	N7	IM_{10}	G13	W_7	A7	RE_8
G2	GND	M7	GND	G12	GND	B7	GND
H1	V_{DD}	N8	V_{DD}	F13	V_{DD}	A6	V_{DD}
H2	V_{DD}	M8	IM_9	F12	W_8	B6	RE_9
J1	AD_1	N9	IM_8	E13	W_9	A5	RE_{10}
J2	AD_2	M9	IM_7	E12	W_{10}	B5	RE_{11}
K1	AD_3	N10	IM_6	D13	W_{11}	A4	RE_{12}
K2	AD_4	M10	IM_5	D12	W_{12}	B4	RE_{13}
L1	AD_5	N11	IM_4	C13	W_{13}	A3	RE_{14}
L2	AD_6	M11	IM_3	C12	W_{14}	B3	RE_{15}
M1	AD_7	N12	IM_2	B13	W_{15}	A2	RE_{16}
N1	AD_8	N13	IM_1	A13	W_{16}	A1	RE_{17}
M2	AD_9	M12	IM_0	B12	GND	B2	RE_{18}

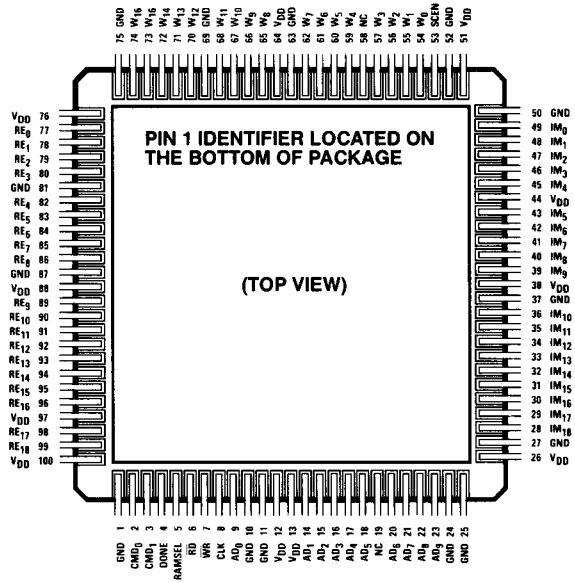
C3 Index Pin (H7 packge only)



Transforms

Pin Assignments

100 Leaded Ceramic Chip Carrier, L4 Package



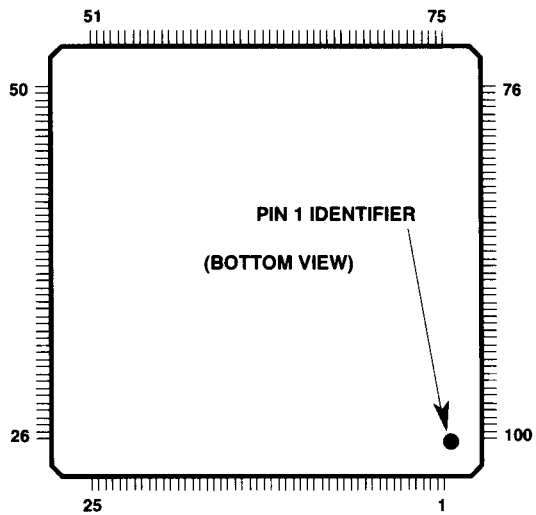


Figure 1. Basic TMC2310 System

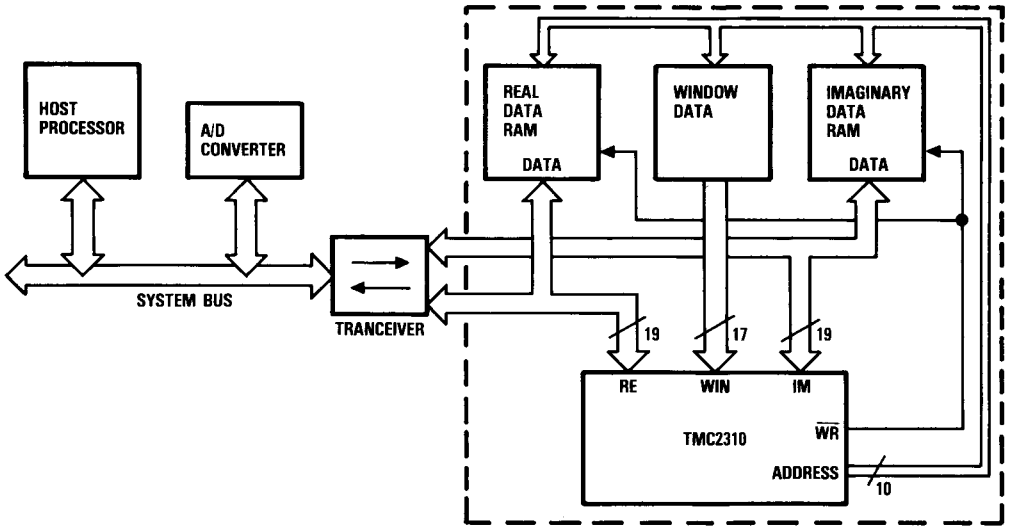
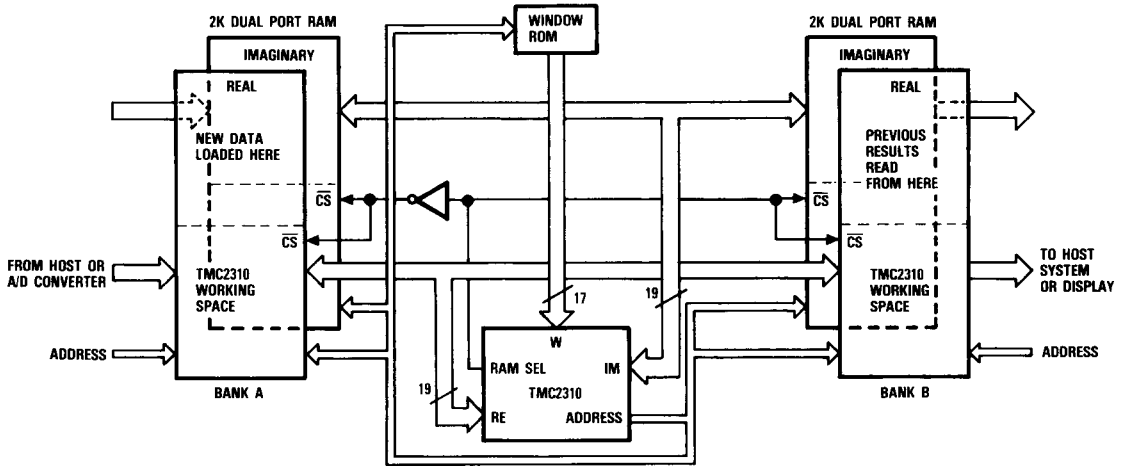


Figure 2. TMC2310 with Dual – Port Memory



Functional Description

General Information

The TMC2310 performs radix-2. Decimation In Time (DIT) Fast Fourier Transforms. It accepts 16-bit input data and maintains 19-bit (RE, IM) data either automatic pass-by-pass or unconditional data rescaling (block floating-pointing). The 19-bit (RE, IM) data buses will accommodate up to three bits of word growth per data pass. Incoming data are rescaled to 16-bit, two's complement fractions on subsequent passes based on the maximum overflow detected during the previous pass (auto scale) or under user control (manual scale). To reduce memory bandwidth requirements (number of passes), the device performs radix-2 butterflies in sets of four (radix-4 addressing). A "pass" is defined as one arithmetic operation performed on the entire data array. Therefore, a butterfly operation is considered to be one data pass. Fourier Transforms require multiple data passes with external memory used for storage of intermediate and final results. All other (non-FFT) operations are completed in one pass.

As shown in Figures 1 and 2, a system can be configured with either single or multi-port RAM, a window coefficient RAM/ROM, and very little additional hardware (see Applications Section). Multi-port memory architecture (Figure 2) allows I/O operations to be overlapped with data processing, maximizing system performance. The internal sequencing and control logic allows the device to operate with minimal support from the host system. External control consists of the programming of two internal configuration registers and a START, LOAD or RESET command. System performance is limited by either the maximum system clock rate or the memory access time. The architecture and sequencing of the TMC2310 are designed to minimize the number of wasted clock cycles between passes, ensuring that each butterfly can be executed in two clock cycles.

The TMC2310 also supports the use of window functions for Fourier transforms. To perform windowing, the user need only provide a set of coefficients in external ROM or RAM and program the device accordingly. Window functions are applied to (multiplied by) the input data during the first data pass. Typical configurations utilize a 1K x 17 (x16 for positive coefficients) block of RAM or ROM on the dedicated window memory bus. For additional information regarding window functions consult reference (1).

The TMC2310 also performs in-place, memory based Finite Impulse Response (FIR) filtering. This function utilizes the external window port memory for storage of filter coefficients. Fixed coefficient and adaptive FIR filters can be implemented with 16 to 1024 coefficients (taps). Time domain filtering is accomplished with a memory based shift register technique in which the accumulated sum of products is determined (convolution of filter coefficients with stored data samples). Adaptive filtering allows real-time updates to filter coefficients by a dynamic update value.

Real and Complex vector arithmetic functions include multiplication, multiply-accumulation, and magnitude squared ($I^2 + Q^2$). By combining functions, a variety of signal processing algorithms can be performed, including frequency domain filtering, signal analysis and signal synthesis.

A multiple-transform array mode offers multiple equal-length transform capability. Any number of equal-length transforms may be selected up to a maximum of 1024 points. For example, the user may execute 16 contiguous 64-point transforms, reducing the computation overhead associated with starting and executing single transforms. The window coefficients may be identical or unique to each transform. Scaling is performed on all points of all transforms equally, based on the maximum overflow of the previous data pass or on the user specified value.

At the end of the transform, the user may read the 19-bit data output and the 6-bit scaling factor ("block exponent") generated by the internal shift/rescale circuitry. The 4-bit "Total Scaler" value indicates the number of shifts performed on the data (block exponent) while the remaining 2 bits indicate the overflow encountered during the final data pass. Nineteen bits are used for intermediate results in order to minimize roundoff error during transforms. Provisions have been made, however, to allow the use of 16-bit wide memory systems. This can reduce memory component count but may increase roundoff error (arithmetic noise).

The TMC2310 consists of five major sections: two arithmetic elements, external memory interface, control logic and coefficient ROM.

Arithmetic Elements (AEs)

Each AE consists of an 18 x 18 bit multiplier, adders/ accumulators and data storage. The AEs interface to external data and window memory as well as internal coefficient ROM. Communication between AEs allows the device to perform complex arithmetic operations. To minimize arithmetic error, each AE retains maximum precision until the output stage where data are rounded to 19 bits (Real and Imaginary). The bidirectional data buses transfer data between the AE and external memory. 19-bit input values are shifted at the input to the multiplier array. This shift is either automatic (FFT auto scale modes) or user controlled (manual scale). On the first pass, if the upper three bits contain significant data, the user must right shift the input data using manual scaling.

External Memory Interface

The TMC2310 provides all the necessary addressing and control for external memory. Read and write address are provided as well as control outputs for write strobes, read enables and a source/destination RAM select for multiple memory bank systems. The single, 10-bit address output is multiplexed for read and write operations. The sequence is determined by the selected function as well as other user specified options.

The sequence may be specified as bit-reversed or sequential for FFT/IFFT operations. The selected sequence has no effect on execution time. However, it does affect the ordering of input data and whether additional memory is required (scratch pad). The device supports a special "pipelined" addressing mode for all operations. Under normal addressing, the address and controls are output during the same clock period as the data. In the pipelined mode, address and controls are output one clock cycle prior to the data, providing added flexibility in the host system interface as well as reducing memory speed requirements (see Timing and Applications).

Coefficient ROM

An internal ROM is included as a coefficient look-up table to the AEs. The ROM supplies the sinusoidal coefficients ("Roots of Unity") required for forward and inverse FFTs. The ROM is accessed under internal control and outputs data to the arithmetic elements during FFT passes (Sine and Cosine values). The ROM contains coefficients to support transforms of up to 1K (1024) data points.

Control

The control section configures the data paths and provides internal sequencing. The device operation is defined by two internal configuration registers. Once the function has been "STARTed", the device performs all sequencing and activates the DONE flag upon completion.

Signal Definitions

Power

V_{DD}, GND — The TMC2310 operates from a single +5V supply. All power and ground lines must be connected.

Clock

CLK — The TMC2310 operates from a single system clock. All internal and external operations are referenced to the rising edge of CLK.

Data Buses

RE_{18-0} — RE-Bus is a bidirectional data bus for "Real" data. This bus is time multiplexed for reads and writes. When the device is Idle, this bus is in the high-impedance state. RE_0 is the Least Significant Bit (LSB). RE_{15-3} is also used to load the internal configuration registers. Data placed on the bus are clocked into a configuration register during a LOAD command. Registers may also be programmed by storing configuration data in address 0 of the Real data memory. A LOAD command causes a read operation with the address bus set to address 0.

IM_{18-0} — IM-Bus is a bidirectional data bus for "Imaginary" data. This bus is time multiplexed for reads and writes. When the device is idle, this bus is in the high-impedance state. IM_0 is the LSB>

W_{16-0} — The W-Bus is used to input the 17-bit window and FIR Filter coefficients. W_{5-0} is also used as an output to access the block exponent and last pass overflow.

Data Buses (cont.)

W_{16-0} The scaler exponent (W_{3-0}) indicates the number of shifts performed on the data for multiple pass transforms while W_{5-4} indicates the overflow (in bits) that occurred during the previous pass. W_{5-4} indicates how many, if any, of the three MSBs (RE_{18-16}, IM_{18-16}) of the final results contain significant data (i.e. bits which are not an extension of the sign). If the largest magnitude result mantissa of a pass falls between -32,768 and +32,767, inclusive, W5-4 following that pass will be 0. If, instead, it falls between -65,536 and -32,769, inclusive, or between +32,768 and +65,535, inclusive, W_{5-4} will be a 1, denoting 1 bit of net word growth to be compensated at the start of the next pass by a right shift.

Control Inputs

CMD1-0 The manifold functions of the TMC2310 FFT processor are selected by the information loaded into its Configuration Registers, CR1 and CR2. The loading of these registers is controlled by the CMD_{1-0} input pins and the clock. The TMC2310 must be RESET and both Command Registers loaded before the first operation (FFT or other transformation) begins. The TMC2310 RESETs automatically after each complete transform, and then CR1 and/or CR2 may be updated for a different operation. If neither CR1 nor CR2 is updated, the previous operation will be repeated on the next data set.

Each register value may be loaded in a separate LOAD sequence, or both values may be loaded sequentially in the same LOAD sequence. CR1 and CR2 may be loaded in any order because bit 15 is an identification bit. The values for CR1 and CR2 may be presented to pins RE_{15-3} from any source. A clever source for one of these values is memory location 0, which is called by the TMC2310 during the LOAD operation.

The LOAD command is given by the first clock rising edge at least t_S after setting CMD_{1-0} =01. The Command Register value is read by the TMC2310 at its RE_{15-3} pins on the third (and fourth, for sequential loading) rising clock edge after the LOAD command. CMD_{1-0} must be held at 01 during the entire LOAD sequence. As long as CMD_{1-0} is held at 01, the TMC2310 command registers track the RE_{15-3} inputs. See the timing diagram 7 and 8 for further information.

Here are the step-by-step instructions:

For the first operation after applying power, the TMC2310 must be RESET. (This step is not required for subsequent operations.)

1. Set CMD_{1-0}=00 for at least 4 clock rising edges. (DONE, WR\and RAMSEL will go HIGH.)

Load the Configuration Registers by entering a LOAD command and presenting the values for CR1 and/or CR2 to the TMC2310.

2. Set CMD_{1-0}=01 at least t_S before a clock rising edge, which we'll label "0."
3. Present the data for CR1 or CR2 to the RE_{15-3} pins at least t_S before clock rising edge 3.
4. To load the selected operation, set CMD_{1-0} =11 to enter the CONTINUE mode, during which the TMC2310 waits for a start command. The START command is given by setting CMD_{1-0} =10 at least t_S before a clock rising edge. For proper operation CMD_{1-0} must be set to 11 (CONTINUE) within 4 clock cycles after to START command. The selected operation is performed to completion.

The registered CoMmanD input is used to RESET the device, LOAD configuration registers, and START an operation. Commands are issued by placing a valid command on the input for one (or more) clock cycle(s) then returning to the CONT command. The input should normally remain in the inactive (CONT) state. The operation of each command is as follows:

CMD_{1-0}	Command	Operation
00	RESET	If RESET is held for at least 4 clock cycles, the DONE flag, WR, RAMSEL are set HIGH. The address bus (AD_{9-0}), data buses RE_{18-0}, IM_{18-0} and W_{16-0} are set to high-impedance state, and the RD output is LOW. A RESET command held for only one cycle does not reset the chip, but causes the last pass scaler (W_{5-4}) to be added to the current scaler exponent (W_{3-0}). The sum then appears on W_{5-0} until cleared. RESET held for more than one cycle will clear the scaler exponent field (W_{5-0}).
01	LOAD	AD_{9-0} is activated and a read is performed with the address set to zero. If LOAD is followed by a CONT then the device will be put into a RESET state.
10	START	START causes the device to begin an operation. The START command must be valid for at least one clock cycle, but not longer than 4 clock cycles. After two start-up cycles, the DONE flag is set LOW and the data and addresses buses become active. Upon completion of the operation, $\overline{WR}$, and DONE are HIGH, $\overline{RD}$ is LOW, AD_{9-0}, RE_{18-0} and IM18-0 are in high-impedance, and execution suspended until the next command. The state of the RAMSEL pin depends on the mode determined in Configuration Register 2. The START command clears the current contents of the scaler exponent (W_{3-0}).
11	CONT	CONTinue is the inactive state for the command input. It has no internal effect. After a command has been issued, the CMD input should be set to this state. Following a start, the CMD input must be set to CONT for the operation to complete properly. If the previous command was a RESET or LOAD then the device remains in RESET.

SCEN

By the end of each N-point transform, the TMC2310 has output a block of N complex results, all of which have been right shifted (rescaled) internally by a common power-of-two scale factor. By bringing SCEN HIGH, the user can read the base-2 logarithm of this scale factor, "A," over W_{3-0}. The unsigned binary value "A" tells how much rescaling, i.e., how many one-binary-place right shifts, occurred cumulatively during all but the first radix-4 pass of the transform.

In general, the largest output word will have grown past the nominal 16-bit input format (the LSBs of the data I/O ports), into bits D_{18}, D_{17}, and D_{16}. While reading "A" over W_{3-0}, the user can also read "C," which tells how much word growth occurred during the final pass, on W_{5-4}. If C=0, then all outputs fit within the 16 LSBs of the data port; if C=1, 2, or 3, then 17, 18, or 19 bits (respectively) are needed to express the largest output value.

After issuing a single RESET (CMD_{1-0}=00) pulse, the user can read unsigned binary value B = A+C over W_{3-0}. This exponent is used when the final results are to be rescaled to 16 bits, via a sign-extending right-shift of C bits. B is read ONLY over W_{3-0} and thus has a maximum readable value of 15 decimal (binary 1111). This should be large enough for almost all applications, since the maximum word growth of a radix-4 FFT pass is a factor of 2.414 x 2.414 = 5.83. A 1024-point transform would entail five of these factors, or a cumulative factor of 6726, which requires up to 13 bits of shifting, i.e., B<14.

Figure 1 depicts the timing relationships among the SCEN, CMD_{1-0}, A, B, and C. In this example, we denote as "2" the first rising edge of CLK after the chip's DONE flag goes high. If we then bring SCEN HIGH before CLK edge 3, we will observe exponent "A" on W_{3-0} and "C" on W_{5-4}, starting t_{ENA} after CLK edge 3. The RESET pulse we issue on CLK edge 4 (CMD_{1-0}=00) cause the HI-Z output on W_{3-0}, t_{DIS} after CLK edge 5, followed by the value "B" on W_{3-0} t_{ENA} after CLK edge 6. The value B will remain on W_{3-0} until the end of the first pass of the next transform, when the first pass exponent of the next transform will replace it.

In general, A will remain on W_{3-0} until after CLK edge N+1 if CMD_{1-0} is 00 before CLK edge N. The output is then disabled for one clock cycle before B appears over the same pins, W_{3-0}.

The SCaler output ENable is used to read the block exponent and last pass overflow. When SCEN is HIGH, the six LSBs of the W-Bus are enabled and consist of the data block (scaler) exponent (W_{3-0}) and the last pass overflow ($_{5-4}$). When SCEN is LOW, the W-Bus is in high-impedance and acts as an input. At the end of an operation, the scaler exponent will show the total number of right-shift performed on the data array (both from manual and auto scaling), and the last pass scaler (W_{5-4}) will give the overflow occurring during the last pass through the data.

Control Outputs

AD_{9-0} The 10-bit ADdress output provides memory addressing for the data and window memories. The device supports sequential and bit-reversed addressing for FFTs, FIR data shift addressing, and multiple transform addressing for both read and write operations. Under normal conditions, the memory address is output on the same clock cycle as the read or write operation. Selecting pipelined addressing causes the address, $\overline{RD}$ and RAMSEL to appear one clock cycle prior to the read/ write data.

$\overline{WR}$ WRite is an active LOW pulse used to strobe data into the external data memory.

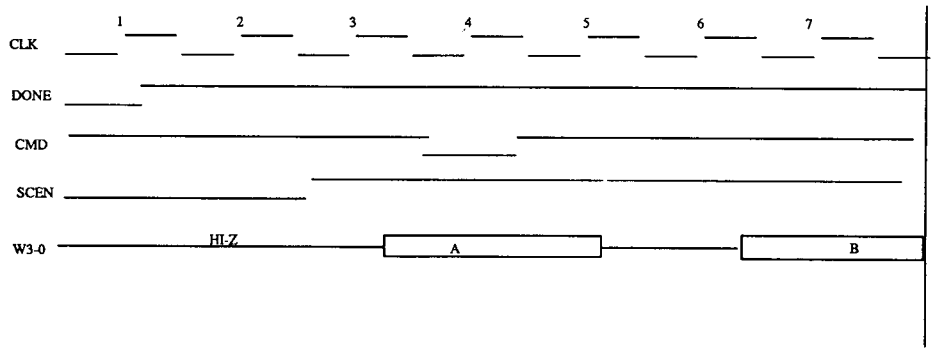


Figure 1.

Control Outputs (cont.)

$\overline{WR}$ (cont.) The address and control outputs are guaranteed to be valid before $\overline{WR}$ is LOW and after $\overline{WR}$ goes HIGH.

$\overline{RD}$ ReaD can be used to control the output enables of external memory. It indicates the direction of the RE and IM data buses. When LOW, the TMC2310 is performing a read (input) operation, and a HIGH indicates a write (outputs enabled) operation. When the DONE output flag is HIGH, $\overline{RD}$ is set LOW.

RAMSEL The RAM SELect output is used to bank select external memory and to identify the location of the initial and final results. Its operation is determined by setting a 2-bit parameter in Configuration Register 2. It can be used to select between physically separate memories or as an additional address line in paged memory systems. Detailed operation of RAMSEL is given in ***Tables 3, 4, 5*** and ***6***.

DONE The DONE flag goes LOW after an operation is "STARTed" and remains LOW until it is complete. One cycle after DONE goes HIGH, the device is idle and final results are available in external memory. DONE = HIGH also indicates that the chip's data (RE and IM) and address (AD_{9-0}) bus drivers are in the high-impedance state, $\overline{WR}$ is inactive (HIGH), and $\overline{RD}$ is LOW. DONE can be used as a host interrupt as well as a control line to allow host system access to data memory and results.

Package Interconnections

Signal Type	Signal Name	Function	G5, H7 Package Pins	L4 Package Pins
Power	V_{DD}	Supply Voltage	H1, H2, N8, F13, A6	12, 13, 26, 38, 44, 51, 64, 76, 88, 97, 100
	GND	Ground	B1, G1, G2, N2, M7, M13, G12, B12, A10, B7	1, 10, 11, 24, 25, 27, 37, 50, 52, 63, 69, 75, 81, 87
Clock	CLK	System Clock	F2	8
Data	RE_{18-0}	Data Bus (Real)	B2, A1, A2, B3, A3, B4, A4, B5, A5, B6, A7, A8, B8, A9, B9, B10, A11, B11, A12	99, 98, 96, 95, 94, 93, 92, 91, 90, 89, 86, 85, 84, 83, 82, 80, 79, 78, 77
	IM_{18-0}	Data Bus (Imaginary)	M3, N3, M4, N4, M5, N5, M6, N6, N7, M8, N9, M9, N10, M10, N11, M11, N12, N13, M12	28, 29, 30, 31, 32, 33, 34, 35, 36, 39, 40, 41, 42, 43, 45, 46, 47, 48, 49
	W_{16-0}	Window/Coefficient Bus	A13, B13, C12, C13, D12, D13, E12, E13, F12, G13, H13, H12, J13, J12, K13, K12, L13	74, 73, 72, 71, 70, 68, 67, 66, 65, 62, 61, 60, 59, 57, 56, 55, 54
Controls	CMD_{1-0}	Command Inputs	C1, C2	3, 2
	SCEN	Scaler Exponent Enable	L12	53
	AD_{9-0}	Address Bus Output	M2, N1, M1, L2, L1, K2, K1, J2 J1, F1	23, 22, 21, 20, 18, 17, 16, 15, 14, 9
	RAMSEL	Source/Target RAM Select	D1	5
	$\overline{RD}$	External Memory Enable	E2	6
	$\overline{WR}$	Write Strobe Output	E1	7
Flags	DONE	Function Complete Flag	D2	4
No Connect	NC	No Connect Pins	-	19, 58
	-	Index Pin	C3	

Device Operation

Upon power-up of the device, the user should immediately issue a RESET command (CMD_{1-0}=00), forcing the device into a "DONE" state. A RESET must be performed prior to any attempt to initialize internal configuration registers. Following the RESET, the DONE flag is HIGH and the address and data (RE, IM and W) buses are set to high-impedance.

Prior to performing any operation, the user must initialize and configure the device by programming two internal configuration registers (CR1, CR2). There are two methods of initializing the registers. Data may be stored in external memory, address location "0" or they may be placed directly on the RE-Bus (RE_{15-3}). A LOAD command (CMD_{1-0}=01) causes a read on the RE-Bus with AD_{9-0}=0. Data read from memory (or directly from the bus) are stored into the configuration register selected by bit 15 of the data word. A minimum of two load commands are required to input the two words, CR1 and CR2. The loads of CR1 and CR2 may be performed consecutively or separately by one or more "continue" cycles.

The configuration registers define the function to be performed as well as other operating parameters. Once programmed, device operation is controlled by the two-bit command control (CMD_{1-0}). Commands are used to begin or suspend operations and to load configuration registers. Operations may be repeated (under the same conditions) without reloading the configuration registers by issuing additional START commands. If the RESET command has been applied after the configuration registers have been loaded, however, it may be necessary to reload Configuration Register 2, since RESET will clear bits 3, 4 and 5 of CR2 and the internal SCaler ENable (SCEN) register.

Once the input data have been stored in external memory (beginning at address 0) and the configuration registers initialized, device operation begins following a START command. After the START command has been initiated, the command input must be set to CONT (CMD_{1-0}=11) within 4 clock cycles for proper operation. During execution, the device takes control of the local data memory bus, enables the address output bus and generates external memory control. The DONE flag will be set HIGH to indicate that the TMC2310 has completed its operations and final results are available in memory.

All intermediate and final results are stored in external memory in 19-bit, two's complement format. Upon completion of the operation, the SCaler ENable input (SCEN) can be used to read the last pass overflow and the scaler exponent. The last pass overflow (W_{5-4}) indicates the word growth that occurred during execution of single pass operations or, during the final butterfly pass of a transform. The 4-bit scaler exponent (W_{3-0}) indicates the number of right-shifts performed on the data array during a multiple pass transform (common data exponent). At the end of an operation, the host system must read the scaler exponent prior to a RESET command. Failure to do so will result in an incorrect scaler exponent value. A RESET command applied for one cycle will cause the last pass overflow to be added to the current value of the scaler exponent. RESET held for more than one clock cycle will clear the scaler exponent field (W_{5-0}). Immediately after a START command, the scaler exponent will be initialized.

Configuration Register 1 (CR1)

Configuration Register 1 defines the operation, transform length, FFT addressing sequence and scaling modes.

Function Codes

Table 1 indicates the input and output values for each function. The RE and IM buses are multiplexed for reads and writes while the W-Bus is used for input only. W-Bus(1) and W-Bus(2) indicate the input for first and second cycle read on the W-Bus, respectively. To input two words, the read address for both W-Bus operands is available during the first (read) cycle. It may be necessary for the user to register the address or data externally for proper synchronization (see Applications Section).

In general, single pass operations (MPY, MAC, MAGSQ) read data from memory and output results to the same address, overwriting the original input data. If the input data are to be saved, use of the RAMSEL allows results to be output to a separate result memory or directly to the host system. All data should be stored in external memory beginning at address 0. The TMC2310 begins all operations at address 0.

Table 1 includes operations designated as "2-Re" (2 Real). "R/I" (Real/Imaginary), and "Cmplx" (Complex). The distinction is as follows:

2-Re These operations involve only a single data word from the W-Bus. The data word

Function Codes (continued)

input in the W–Bus is applied to the data input on both the RE and IM data buses.

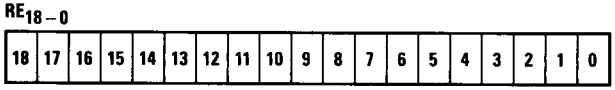
R/I — These operations involve two values input from the W–Bus with the first W–Bus operand applied to the RE data and the second applied to the IM data. No cross terms are evaluated.

Cmplx — These operations involve two W–Bus operands, interpreted as a complex data value. The function involves a complex operation including cross terms.

Table 1. Function Codes vs. Bus Function

Code	Function	Inputs				Outputs	
		RE–Bus	IM–Bus	W–Bus(1)	W–Bus(2)	RE–Bus	IM–Bus
0000	IFFT No–Window	R	I	–	–	Complex IFFT Results	
0001	MPY–ACC 2–Re	R	I	W	–	Σ RW	Σ IW
0010	MPY–ACC R/I	R	I	W_1	W_2	Σ RW_1	Σ IW_2
0011	MPY–ACC Cmplx	R	I	W_R	W_I	Σ $RW_R - IW_I$	Σ $IW_R + \Sigma$ RW_I
0100	MAGSQ	R	I	–	–	$[R^2 + I^2]/2$	$[R^2 + I^2]/2$
0101	MPY 2–Re	R	I	W	–	RW	IW
0110	MPY R/I	R	I	W_1	W_2	RW_1	IW_2
0111	MPY Cmplx	R	I	W_R	W_I	$RW_R - IW_I$	$IW_R + RW_I$
1000	FFT No–Window	R	I	–	–	Complex FFT Results	
1001	FIR 2–Re	R_m	I_m	W_n	–	Σ R_mW_n	Σ I_mW_n
1010	FIR R/I	R_m	I_m	W_{1n}	W_{2n}	Σ R_mW_{1n}	Σ I_mW_{2n}
1011	FIR Adaptive	R_m	C_n	σ	–	Σ R_mC_n	$C_n(1 - \sigma)$
1100	FFT Re–Window	R	I	W	–	Complex FFT Results	
1101	IFFT Re–Window	R	I	W	–	Complex IFFT Results	
1110	Cmplx MPY + FFT	R	I	W_R	W_I	Complex FFT Results	
1111	Cmplx MPY + IFFT	R	I	W_R	W_I	Complex IFFT Results	

Configuration Register 1 (CR1) Format



Not Used (Don't Care)

Manual Scale Factor
- 00 Shift 0 Bits
- 01 Shift 1 Bit
- 10 Shift 2 Bits
- 11 Shift 3 Bits

Scaling Mode
- 0 Auto Scale (Manual On First Pass)
- 1 Manual Scale (All Passes)

FFT Addressing Sequence
- 00 No Bit – Reverse (In – Place FFT)
- 01 Bit – Reverse On First Pass Read
- 10 Bit – Reverse On Last Pass Write
- 11 Bit – Reverse On First Pass Read And Last Pass Write

Single Transform Length
- 000 Undefined
- 001 16 Points
- 010 32 Points
- 011 64 Points
- 100 128 Points
- 101 256 Points
- 110 512 Points
- 111 1024 Points

Function Code
- 0000 IFFT No Window
- 0001 Multiply – Accumulate 2 Real Inputs
- 0010 Multiply – Accumulate RE/IM Inputs
- 0011 Multiply – Accumulate Complex Input
- 0100 Magnitude Squared
- 0101 Multiply 2 Real Inputs
- 0110 Multiply RE/IM Inputs
- 0111 Multiply Complex
- 1000 FFT No Window
- 1001 FIR Filter, 2 Real Inputs
- 1010 FIR Filter, Dual RE/IM Inputs
- 1011 FIR Adaptive
- 1100 FFT Real Window
- 1101 IFFT Real Window
- 1110 Complex Multiply + FFT
- 1111 Complex Multiply + IFFT

Configuration Register Select Bit
- 0 Configuration Register 1 (CR1)

Not Used (Don't Care)

CR1[14:11]

0000 IFFT No Windowing. A complex Inverse Fast Fourier Transform is performed on data stored in external memory. No windowing is performed (rectangular window) during the IFFT and the W–Bus is unused. The memory addressing sequence and the transform length are determined by other parameters. The N–point inverse FFT is defined by:

$$h(n) = \sum_{k=0}^{N-1} H(k)e^{+j2\pi nk/N}$$

0001 Multiply–Accumulate Two Real Inputs. Both the RE and IM data are multiplied by the data word input on the W–Bus. Results are accumulated and written back to external memory. The output to memory is the sum of all previous multiplications. (e.g. Address 20_{10} = sum of first 21 products (0–20), Address 49_{10} = sum of first 50 products, etc.)

0010 Multiply–Accumulate Real/Imaginary. The RE data input is multiplied by the first word input on the W–Bus. The IM input is multiplied by the second word input on the W–Bus. The output to memory is the accumulation of all previous multiplications.

$$RE_{out}(N) = \sum_{K=0}^{N} RE_{in}(k)W_1(k)$$

$$IM_{out}(N) = \sum_{K=0}^{N} IM_{in}(k)W_2(k)$$

0011 Multiply–Accumulate Complex. Complex multiplication is performed on each (RE, IM) and (W_R, W_I) pair. The output to memory is the accumulation of all previous complex multiplications. Input of a complex operand on the W–Bus is done on two consecutive clock cycles.

$$RE_{out}(N) = \sum_{K=0}^{N} [RE_{in}(k)W_R(k) - IM_{in}(k)W_I(k)]$$

$$IM_{out}(N) = \sum_{K=0}^{N} [IM_{in}(k)W_R(k) + RE_{in}(k)W_I(k)]$$

($W_R = W_1$, $W_I = W_2$)

0100 **Magnitude Squared. The RE and IM data are squared separately. The squares are summed, halved and their most significant portions are output to both the RE and IM data memories.**

$$RE_{out}(n) = IM_{out}(n) = [RE_{in}^2(n) + IM_{in}^2(n)]/2$$

0101 Multiply 2–Real. The RE and IM data are multiplied by the single data word input on the W–Bus during the read cycle. Results are output to the corresponding memory address.

$$RE_{out}(n) = RE_{in}(n)W_1(n)$$
$$IM_{out}(n) = IM_{in}(n)W_1(n)$$

0110 Multiply Real/Imaginary. The RE data value is multiplied by the data input on the first W–Bus cycle. The IM input is multiplied by the data input on the second W–Bus cycle. The result output to memory is:

$$RE_{out}(n) = RE_{in}(n)W_1(n)$$
$$IM_{out}(n) = IM_{in}(n)W_2(n)$$

0111 Multiply Complex. A complex multiplication is performed on the data input on the RE, IM and W–Bus inputs. The complex output to memory is:

$$(RE + jIM)(W_R + jW_I) =$$
$$RE_{out}(n) = [RE_{in}(n)W_R(n)] - [IM(n)_{in}W_I(n)]$$
$$IM_{out}(n) = [IM_{in}(n)W_R(n)] + [RE(n)_{in}W_I(n)]$$

1000 FFT No Windowing. A complex Fast Fourier Transform is performed on data stored in external memory. No windowing is performed (rectangular window) during the FFT and the W–Bus is unused. The memory addressing sequence and the transform length are determined by other parameters. The forward FFT is defined by:

$$H(k) = \sum_{n=0}^{N-1} h(n)e^{-j2\sigma nk/N}$$

CR1[14:11] (continued)

1001 FIR 2–Real. Finite Impulse Response filtering is done by performing a RAM based multiplication–accumulation on data and coefficients stored in external memory. Multiplication with accumulation is performed between filter coefficients input on the W–Bus and the RE and IM data. The RE and IM data are shifted down one location in memory with the final accumulated result written into location N – 1. Two separate data sets may be convolved simultaneously, using the RE and IM data and one filter coefficient data set. (See Applications section for more detailed descriptions of FIR operation.) The output is:

$$RE(i)_{out} = RE(i+1)_{in},\ RE(N-1)_{out} = \sum_{n=0}^{N-1} RE(n)W_1(n)$$

$$IM(i)_{out} = IM(i+1)_{in},\ IM(N-1)_{out} = \sum_{n=0}^{N-1} IM(n)W_1(n)$$

1010 FIR Real/Imaginary. Finite Impulse Response filtering is done by performing a RAM based multiplication–accumulation on data and coefficients stored in external memory. Multiplication with accumulation is performed between filter coefficients input on the W–Bus, and the RE and IM data. The RE and IM data are shifted down one location in memory with the final accumulated result written into location N – 1. When the next input sample is loaded into address N – 1 the operation may be re–STARTed to form the next sum. Two sets of coefficients are used, both input through the W–Bus, one for RE data and a second for IM data. (See Applications section for more detailed description of FIR Operation.) The data outputs are:

$$RE(i)_{out} = RE(i+1)_{in},\ RE(N-1)_{out} = \sum_{n=0}^{N-1} RE(n)W_1(n)$$

$$IM(i)_{out} = IM(i+1)_{in},\ IM(N-1)_{out} = \sum_{n=0}^{N-1} IM(n)W_2(n)$$

1011 FIR Adaptive. Adaptive FIR filtering allows concurrent updates to filter coefficients by the value specified on the W–Bus. The RE–Bus is used for input data and the IM–Bus used for filter coefficients. The W–Bus determines the coefficient update value (σ). The data on the RE–Bus is multiplied, accumulated and shifted down one address in memory. The final convolution result is output to address N – 1. The next input sample is stored in address N – 1, and the operation re–STARTed to form the next sum. The filter coefficients, input on the IM–Bus, are modified and stored back to their original address locations as follows:

$IM(i)_{out} = IM(i)_{in}(1 - \sigma(i))$ or,
New Coefficient = [Old Coefficient] • [1 – update value]

Update values are input on the W–Bus for each coefficient (during the read cycle). The data output is:

$$RE(i)_{out} = RE(i+1)_{in},\ RE(N-1) = \sum_{k=0}^{N-1} RE(k)IM(k)$$

1100 FFT Real Window. An FFT is performed on complex data in external memory. During the first FFT pass, the RE and IM data are multiplied by the window coefficients input through the W–Bus. The real data window is applied to both the RE and IM data. The forward FFT with real windowing is defined by:

$$H(k) = \sum_{n=0}^{N-1} h(n)w(n)e^{-j2\pi nk/N}$$

1101 IFFT Real Window. An Inverse FFT is performed on the complex data in external memory. During the first IFFT pass, the RE and IM data are multiplied by the window coefficients input through the W–Bus. The real data window is applied to both the RE and IM data. The inverse FFT with real windowing is defined by:

$$h(n) = \sum_{k=0}^{N-1} H(k)w(k)e^{+j2\pi nk/N}$$

Transforms

1110 Complex Multiplication + FFT. Prior to performing the FFT, a complex multiplication is performed between the RE and IM data and complex data stored in external memory input through the W–Bus. This operation requires one additional pass, compared to the FFT with Real Window, to complete the complex multiplication.

1111 Complex Multiplication + IFFT. Prior to performing the inverse FFT, a complex multiplication is performed between the RE and IM data and complex data stored in external memory and input through the W–Bus. This operation requires one additional pass, compared to the IFFT with Real Window, to perform the complex multiplication.

Single Transform Length CR1[10:8]

000 Undefined
001 16 data points (Recommended for Non–FFT/IFFT Operations)
010 32 data points
011 64 data points
100 128 data points
101 256 data points
110 512 data points
111 1024 data points

This field defines the number of data points for a single transform. To reduce computational overhead, multiple transforms can be performed concurrently up to the 1024–point limit. This field sets the number of points for a single transform while the number of concurrent transforms is determined by Configuration Register 2 (CR2[14:8]). The total number of data points for any operation is obtained by multiplying the single transform length by the "number of transforms" in CR2:

(Transform Length)•(No. of Transforms)=Total number of data points

For all non–transform operations, use of transform length = 16 is recommended. This provides the maximum flexibility in selecting the size of the data set, allowing any number of points which is a multiple of 16 (see Table 2).

FFT Addressing Sequence CR1[7:6]

00 No Bit–reverse (In–Place, Sequential Addressing) (Use for Non–FFT Operations)
01 Bit–reverse address during first pass read
10 Bit–reverse address during last pass write
11 Bit–reverse address during first pass read and last pass write

Several types of address sequences are available for transforms. Data scrambling is required when performing the FFT/IFFT. If the data is scrambled in memory prior to the start of the transform, then it can be done "in–place", thereby reducing the external memory requirements (see Applications). If data is stored in sequence, the TMC2310 must perform scrambling during the first pass of the transform (CR1[7:6] = 01 or 11). The scrambling amounts to a bit–wise reversing of the memory address. When performing the "bit–reversed" addressing, the user must provide additional memory for intermediate storage to avoid overwriting unused input data. The user must also store the window function in either bit–reversed or sequential order to match the ordering to the input data. (See Applications section.)

Bit–reversing the memory address during the last data pass write (CR1[7:6] = 10 or 11) may be useful if the data will undergo additional FFT processing. The final results are placed in scrambled order in preparation for the next operation.

Scaling Modes CR1[5]

0 Auto Scaling
1 Manual Scaling (Use for All Non–FFT Operations)

This field determines the input data shifting. For multiple pass transforms using auto scaling, the input data is shifted by the number of bits set by the manual scale factor (CR1[4:3]) for the first pass or by the Last Pass Overflow scaler (W_{5-4}) determined from the last pass of the previous operation (CR2[3]). Subsequent passes shift the data based on the overflow of the previous pass. During each pass of the FFT, the maximum overflow (0–3 bits) is monitored as results are output to external memory. The overflow value is used as a shift count for incoming data on the next pass. The number of shifts performed during all passes (including the first pass) and the overflow from the final data pass are available on the W–Bus using the SCaler ENable control (SCEN).

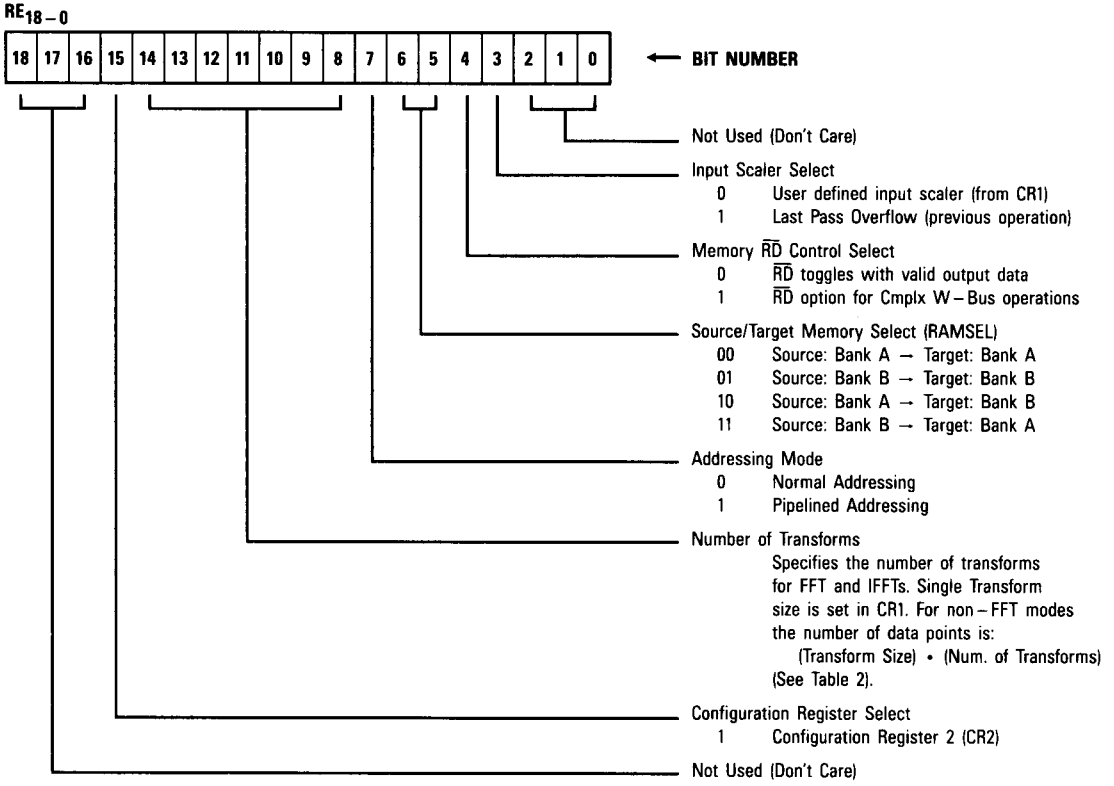
Use of manual scaling disables the overflow detection circuitry and shifts input data on every pass. The shift amount for each pass is determined by the manual scale factor set in CR1[4:3].

Manual Scale Factor CR1[4:3]

00 Shift by 0 bits
01 Shift by 1 bit
10 Shift by 2 bits
11 Shift by 3 bits

This field specifies the number of shifts performed on the input data. In auto scaling, it defines the shift performed on the first data pass only. For manual scaling, the data is shifted by this value on each pass. If the Input Scaler Select (CR2[3]) is activated to use the Last Pass Overflow scaler, then the Manual Scale Factor will be overridden during the first data pass in either the Auto or Manual Scaling modes. Also, the initial or first pass shift factor specified for either Auto or Manual Scaling will not be included in the Data Block (Scaler) exponent. W[3:0]. The user must be cautious when performing manual scaling in order to avoid arithmetic errors due to incorrect scaling. (See Applications Section.) If the original data are all only 16-bits wide, then any initial scale factor may be used, with 0 yielding the best arithmetic noise performance. If one or more 19-bit values are included among the input data, an initial scale factor of 3 is need to guard against first-pass overflow.

Configuration Register 2 (CR2) Format



Configuration Register 2 (CR2)

Configuration Register 2 is used to define the operation of the RAMSEL and $\overline{RD}$ signals, the addressing modes and the total number of data points for each operation.

Number of 16-Point Blocks CR2[14:8]

0000000	Undefined
bbbbbbb	Number of 16-point transforms
bbbbbb0	Number of 32-point transforms
bbbbb00	Number of 64-point transforms
bbbb000	Number of 128-point transforms
bbb0000	Number of 256-point transforms
bb00000	Number of 512-point transforms
1000000	Single 1024-point transform

This parameter is used in conjunction with the single transform lingth set in CR1. The total number of points is determined by multiplying this value by 16. The possible combinations of transform length and number of transform/ data points are specified in Table 2.

Table 2. Possible Combinations of Transform Length and Number of Transforms

Trans. Length CR1[10:8]	Num. Blocks CR2[14:8]	Number of FFT Transforms	Number of Taps or Data Words
xxx	0000000	Undefined for all transform sizes	
000	xxxxxxx	Undefined for all transform sizes	
001 16 – Point	0000001	1 Transform	16 Taps/Words
	0000010	2 Transforms	32 Taps/Words
	0000011	3 Transforms	48 Taps/Words
	•	•	•
	•	•	•
	1000000	64 Transforms	1024 Taps/Words
010 32 – Point	0000010	1 Transform	32 Taps/Words
	0000100	2 Transforms	64 Taps/Words
	0000110	3 Transforms	96 Taps/Words
	•	•	•
	•	•	•
	1000000	32 Transforms	1024 Taps/Words
011 64 – Point	0000100	1 Transform	64 Taps/Words
	0001000	2 Transforms	128 Taps/Words
	0001100	3 Transforms	192 Taps/Words
	•	•	•
	•	•	•
	1000000	16 Transforms	1024 Taps/Words
100 128 – Point	0001000	1 Transform	128 Taps/Words
	0010000	2 Transforms	256 Taps/Words
	0011000	3 Transforms	384 Taps/Words
	•	•	•
	•	•	•
	1000000	8 Transforms	1024 Taps/Words
101 256 – Point	0010000	1 Transform	256 Taps/Words
	0100000	2 Transforms	512 Taps/Words
	0110000	3 Transforms	768 Taps/Words
	1000000	4 Transforms	1024 Taps/Words
110 512 – Point	0100000	1 Transform	512 Taps/Words
	1000000	2 Transforms	1024 Taps/Words
111 1024 – Point	1000000	1 Transform	1024 Taps/Words

Addressing Mode CR2[7]

0 Normal Addressing
1 Pipelined Addressing

This field selects the addressing mode for external memory access. In normal addressing, the memory address, $\overline{RD}$, RAMSEL and the read/write data are output on the same clock cycle. In pipelined addressing, the address, $\overline{RD}$, and RAMSEL outputs appear one clock cycle prior to the data. This enables the system to setup one cycle in advance by externally registering the address and controls. In both modes, the $\overline{WR}$ strobe is synchronized with the data and is guaranteed to meet data setup and hold times. Pipelined addressing is supported for all device operations. (See Applications section.)

Source/Target Memory Select CR2[6:5]

00 Source: Bank A (RAMSEL = HIGH)
Target: Bank A (RAMSEL = HIGH)
01 Source: Bank B (RAMSEL = LOW)
Target: Bank B (RAMSEL = LOW)
10 Source: Bank A (RAMSEL = HIGH)
Target: Bank B (RAMSEL = LOW)
11 Source: Bank B (RAMSEL = LOW)
Target: Bank A (RAMSEL = HIGH)

This field allows the user to select the locations of the initial data inputs and the final data results in multiple memory bank systems. Use of banked memory systems allow I/O operations to be overlapped with arithmetic processing. RAMSEL allows the device to select between the two banks of memory (RAMSEL = HIGH indicating Bank A and RAMSEL = LOW indicating memory Bank B). It may also be used as an additional address line in paged memory systems.

Transform operations require multiple data passes. The state of RAMSEL for each pass is based on the FFT addressing sequence (CR1[7:6]), the pass number and the Source/Target Memory select. Passes involving bit-reversed addressing require that RAMSEL toggle between reading and writing to prevent overwriting unused data. The TMC2310 identifies passes involving bit-reversed addressing and sets RAMSEL accordingly. During a bit-reverse pass, the TMC2310 either reads data with RAMSEL = HIGH and outputs with RAMSEL = LOW, or, reads with RAMSEL = LOW and outputs with RAMSEL = HIGH. Systems utilizing bit-reversed addressing must use RAMSEL for memory control to obtain proper results.

The operation of RAMSEL for transform operations is defined in tables 3, 4, 5 and 6. The state of RAMSEL is shown for each pass. The table indicates the logic level of RAMSEL for input and output during each pass. All single pass (non-FFT) operations (except FIR) allow the source and target data locations to be specified with this two-bit control parameter.

For FIR filter operations, RAMSEL has been designed to differentiate device outputs between shifted data samples and the accumulated convolutional sum output at the end of each pass. When CR2[6:5] is set to "00" or "10" RAMSEL remains HIGH (Bank A) for all reads and writes (data shifting in memory) except during the last write. The last write of an FIR pass is the convolutional sum, which is output with RAMSEL = LOW. When CR2[6:5] is set to "01" or "11" RAMSEL remains LOW (Bank B) for all reads and writes except during the last output cycle when the sum result is written to memory with RAMSEL = HIGH.

Upon power-up RESET, RAMSEL will be in a HIGH state. Once CR2 has been loaded into the device, RAMSEL will reflect the Source/Target Memory Selection specified in CR2[6:5]. After the operation has been completed and the DONE flag has returned to a HIGH state, RAMSEL will return to the "Source" state designated in CR2[6:5] unless a RESET has been applied. RESET will clear CR2[5] and force RAMSEL HIGH.

Application of the RESET command will clear CR2[5] and force RAMSEL = HIGH. CR2 must be loaded into the device to activate this option.

Memory $\overline{RD}$ Control Select CR2[4]

0 $\overline{RD}$ toggles to denote valid output results
1 $\overline{RD}$ option for Complex W-Bus operations

During all device operations, $\overline{RD}$ indicates the direction of the RE and IM data buses. When LOW, the TMC2310 is performing a read (input) operation, and a HIGH indicates a write (outputs enabled) operation. When the device performs operations requiring complex inputs to the W-Bus, real and imaginary inputs are time multiplexed on successive cycles. W_R inputs appear with the RE and IM data inputs ($\overline{RD}$ = LOW) while the W_I inputs appear

on the following cycle, when the device is outputting results ($\overline{RD}$ = HIGH). Due to the latency in the architecture of the device, however, results will not appear for at least seven cycles from the corresponding inputs. Under normal operations (CR2[4] = 0) the $\overline{RD}$ signal will not be activated until the first valid result appears, afterwhich $\overline{RD}$ will toggle on successive cycles. For operations that require complex W–Bus inputs CR2[4] can be set HIGH to allow the $\overline{RD}$ signal to toggle upon application of the START command. This will enable the W_R and W_I inputs to be synchronized with the FALLING and RISING edge of the $\overline{RD}$ signal, respectively. For modes that do not involve complex inputs to the W–Bus the $\overline{RD}$ Control Select should be set LOW.

Application of the RESET command will clear CR2[4], therefore, CR2 must be loaded into the device to activate this option.

Input Scaler Select (First Pass Only) CR2[3]

0 First Pass Input Scaler defined in CR1[4:3]
1 Last Pass Overflow from previous operation used as Scaler Input

Under normal operations, the input data scale factor must be specified for the first pass of any operation using the Manual Scale Factor CR1[4:3]. For some applications, it may be necessary to perform additional signal processing functions on the existing data set. When activated (CR2[3] = 1), this option allows the Last Pass Overflow scaler from the previous operation to be used as the input scaler for the next operation. This feature eliminates the need to extract the W5-4 field from the W-Bus and will be useful to post process the data after a particular application. For example, the user may want to rescale the 19-bit data to 16 bits following an FFT operation. By activating this feature, the Last Pass Overflow scaler (from the FFT) will be used to rescale the data as it is input to the device for a multiplication by 1.0 (0.9999. . .). Additional operations that will benefit from this feature are MAGSQ or a filter multiplication following the FFT.

Application of the RESET command will clear CR2[3] and the scaler exponent field (W_{5-0}). CR2 must be loaded into the device to activate this option.

Tables 3, 4, 5 and 6 show the operation of RAMSEL for multiple pass transforms. The state of RAMSEL is shown for read and write operations during each data pass.

For example:

16–point FFT (Real or No Window)

Source = Bank A; Target = Bank A (CR2[6:5] = 00)
Bit–reverse addressing on first pass read (CR1[7:6] = 01)

Pass 0: Input data with RAMSEL = H (HIGH)
Output data with RAMSEL = L (LOW)
(Data moved from Bank A to Bank B)

Pass 1: Input data with RAMSEL = LOW
Output data with RAMSEL = HIGH
(Data moved from Bank B back to Bank A)

16–point Complex Multiply + FFT

Source = Bank B; Target = Bank B (CR2[6:5] = 01)
Bit–reverse addressing on first pass read (CR1[7:6] = 01)

Pass W: Input data with RAMSEL = L (LOW)
Output data with RAMSEL = L (LOW)
(Data remains in Bank B)

Pass 0: Input data with RAMSEL = L (LOW)
Output data with RAMSEL = H (HIGH)
(Data moved from Bank B to Bank A)

Pass 1: Input data with RAMSEL = HIGH
Output data with RAMSEL = LOW
(Data moved from Bank A back to Bank B)

The tables are valid for single and multiple transforms, however, RAMSEL operation is determined by the single transform size only.

Table 3a. RAMSEL Operation for Source = Bank A (RAMSEL=HIGH); Target = Bank A (RAMSEL=HIGH) Operation: FFT/IFFT Real or No Windowing

Source/Target CR2[6:5]	Addressing Seq. CR1[7:6]	Single Transform Size	Pass 0 [1] Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
00	00	16	H/H	H/H			
		32	H/H	H/H	H/H		
		64	H/H	H/H	H/H		
		128	H/H	H/H	H/H	H/H	
		256	H/H	H/H	H/H	H/H	
		512	H/H	H/H	H/H	H/H	H/H
		1024	H/H	H/H	H/H	H/H	H/H
	01, 10 or 11	16	H/L	L/H			
		32	H/L	L/L	L/H		
		64	H/L	L/L	L/H		
		128	H/L	L/L	L/L	L/H	
		256	H/L	L/L	L/L	L/H	
		512	H/L	L/L	L/L	L/L	L/H
		1024	H/L	L/L	L/L	L/L	L/H

Note: 1. H = HIGH
L = LOW

Table 3b. RAMSEL Operation for Source = Bank A (RAMSEL=HIGH); Target = Bank A (RAMSEL=HIGH) Operation: Complex Multiply + FFT/IFFT

Source/ Target CR2[6:5]	Addressing Sequence CR1[7:6]	Single Transform Size	Pass W [1,2] Read/Write	Pass 0 Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
00	00	16	H/H	H/H	H/H			
		32	H/H	H/H	H/H	H/H		
		64	H/H	H/H	H/H	H/H		
		128	H/H	H/H	H/H	H/H	H/H	
		256	H/H	H/H	H/H	H/H	H/H	
		512	H/H	H/H	H/H	H/H	H/H	H/H
		1024	H/H	H/H	H/H	H/H	H/H	H/H
	01, 10 or 11	16	H/H	H/L	L/H			
		32	H/H	H/L	L/L	L/H		
		64	H/H	H/L	L/L	L/H		
		128	H/H	H/L	L/L	L/L	L/H	
		256	H/H	H/L	L/L	L/L	L/H	
		512	H/H	H/L	L/L	L/L	L/L	L/H
		1024	H/H	H/L	L/L	L/L	L/L	L/H

Notes: 1. H = HIGH
L = LOW
2. Pass "W" is the complex multiplication pass for FFT/IFFTs that perform complex multiplication prior to the transform.

Table 4a. RAMSEL Operation for Source = Bank B (RAMSEL=LOW); Target = Bank B (RAMSEL=LOW) Operation: FFT/IFFT Real or No Windowing

Source/Target CR2[6:5]	Addressing Seq. CR1[7:6]	Single Transform Size	Pass 0 [1] Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
01	00	16	L/L	L/L			
		32	L/L	L/L	L/L		
		64	L/L	L/L	L/L		
		128	L/L	L/L	L/L	L/L	
		256	L/L	L/L	L/L	L/L	
		512	L/L	L/L	L/L	L/L	L/L
		1024	L/L	L/L	L/L	L/L	L/L
	01, 10 or 11	16	L/H	H/L			
		32	L/H	H/H	H/L		
		64	L/H	H/H	H/L		
		128	L/H	H/H	H/H	H/L	
		256	L/H	H/H	H/H	H/L	
		512	L/H	H/H	H/H	H/H	H/L
		1024	L/H	H/H	H/H	H/H	H/L

Note: 1. H = HIGH
L = LOW

Table 4b. RAMSEL Operation for Source = Bank B (RAMSEL=LOW); Target = Bank B (RAMSEL=LOW) Operation: Complex Multiply + FFT/IFFT

Source/ Target CR2[6:5]	Addressing Sequence CR1[7:6]	Single Transform Size	Pass W [1,2] Read/Write	Pass 0 Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
01	00	16	L/L	L/L	L/L			
		32	L/L	L/L	L/L	L/L		
		64	L/L	L/L	L/L	L/L		
		128	L/L	L/L	L/L	L/L	L/L	
		256	L/L	L/L	L/L	L/L	L/L	
		512	L/L	L/L	L/L	L/L	L/L	L/L
		1024	L/L	L/L	L/L	L/L	L/L	L/L
	01, 10 or 11	16	L/L	L/H	H/L			
		32	L/L	L/H	H/H	H/L		
		64	L/L	L/H	H/H	H/L		
		128	L/L	L/H	H/H	H/H	H/L	
		256	L/L	L/H	H/H	H/H	H/L	
		512	L/L	L/H	H/H	H/H	H/H	H/L
		1024	L/L	L/H	H/H	H/H	H/H	H/L

Notes: 1. H = HIGH
L = LOW
2. Pass "W" is the complex multiplication pass for FFT/IFFTs that perform complex multiplication prior to the transform.

Table 5a. RAMSEL Operation Source = Bank A; Target = Bank B
Operation: FFT/IFFT Real or No Windowing

Source/Target CR2[6:5]	Addressing Seq. CR1[7:6]	Single Transform Size	Pass 0 [1] Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
10	00, 01	16	H/L	L/L			
		32	H/L	L/L	L/L		
		64	H/L	L/L	L/L		
		128	H/L	L/L	L/L	L/L	
		256	H/L	L/L	L/L	L/L	
		512	H/L	L/L	L/L	L/L	L/L
		1024	H/L	L/L	L/L	L/L	L/L
	10	16	H/H	H/L			
		32	H/H	H/H	H/L		
		64	H/H	H/H	H/L		
		128	H/H	H/H	H/H	H/L	
		256	H/H	H/H	H/H	H/L	
		512	H/H	H/H	H/H	H/H	H/L
		1024	H/H	H/H	H/H	H/H	H/L
	11	16	Not Allowed				
		32	H/L	L/H	H/L		
		64	H/L	L/H	H/L		
		128	H/L	L/H	H/H	H/L	
		256	H/L	L/H	H/H	H/L	
		512	H/L	L/H	H/H	H/H	H/L
		1024	H/L	L/H	H/H	H/H	H/L

Note: 1. H = HIGH
L = LOW

Table 5b. RAMSEL Operation Source = Bank A; Target = Bank B Operation: Complex Multiply + FFT/IFFT

Source/ Target CR2[6:5]	Addressing Sequence CR1[7:6]	Single Transform Size	Pass W [1,2] Read/Write	Pass 0 Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
10	00	16	H/L	L/L	L/L			
		32	H/L	L/L	L/L	L/L		
		64	H/L	L/L	L/L	L/L		
		128	H/L	L/L	L/L	L/L	L/L	
		256	H/L	L/L	L/L	L/L	L/L	
		512	H/L	L/L	L/L	L/L	L/L	L/L
		1024	H/L	L/L	L/L	L/L	L/L	L/L
	01	16	H/H	H/L	L/L			
		32	H/H	H/L	L/L	L/L		
		64	H/H	H/L	L/L	L/L		
		128	H/H	H/L	L/L	L/L	L/L	
		256	H/H	H/L	L/L	L/L	L/L	
		512	H/H	H/L	L/L	L/L	L/L	L/L
		1024	H/H	H/L	L/L	L/L	L/L	L/L
	10	16	H/H	H/H	H/L			
		32	H/H	H/H	H/H	H/L		
		64	H/H	H/H	H/H	H/L		
		128	H/H	H/H	H/H	H/H	H/L	
		256	H/H	H/H	H/H	H/H	H/L	
		512	H/H	H/H	H/H	H/H	H/H	H/L
		1024	H/H	H/H	H/H	H/H	H/H	H/L
	11	16	Not Allowed					
		32	H/H	H/L	L/H	H/L		
		64	H/H	H/L	L/H	H/L		
		128	H/H	H/L	L/H	H/H	H/L	
		256	H/H	H/L	L/H	H/H	H/L	
		512	H/H	H/L	L/H	H/H	H/H	H/L
		1024	H/H	H/L	L/H	H/H	H/H	H/L

Notes: 1. H = HIGH
L = LOW

2. Pass "W" is the complex multiplication pass for FFT/IFFTs that perform complex multiplication prior to the transform.

Table 6a. RAMSEL Operation Source = Bank B; Target = Bank A
Operation: FFT/IFFT Real or No Windowing

Source/Target CR2[6:5]	Addressing Seq. CR1[7:6]	Single Transform Size	Pass 0 [1] Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
11	00, 01	16	L/H	H/H			
		32	L/H	H/H	H/H		
		64	L/H	H/H	H/H		
		128	L/H	H/H	H/H	H/H	
		256	L/H	H/H	H/H	H/H	
		512	L/H	H/H	H/H	H/H	H/H
		1024	L/H	H/H	H/H	H/H	H/H
	10	16	L/L	L/H			
		32	L/L	L/L	L/H		
		64	L/L	L/L	L/H		
		128	L/L	L/L	L/L	L/H	
		256	L/L	L/L	L/L	L/H	
		512	L/L	L/L	L/L	L/L	L/H
		1024	L/L	L/L	L/L	L/L	L/H
	11	16	Not Allowed				
		32	L/H	H/L	L/H		
		64	L/H	H/L	L/H		
		128	L/H	H/L	L/L	L/H	
		256	L/H	H/L	L/L	L/H	
		512	L/H	H/L	L/L	L/L	L/H
		1024	L/H	H/L	L/L	L/L	L/H

Note: 1. H = HIGH
L = LOW

Table 6b. RAMSEL Operation Source = Bank B; Target = Bank A
Operation: Complex Multiply + FFT/IFFT

Source/ Target CR2[6:5]	Addressing Sequence CR1[7:6]	Single Transform Size	Pass W [1,2] Read/Write	Pass 0 Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
11	00	16	L/H	H/H	H/H			
		32	L/H	H/H	H/H	H/H		
		64	L/H	H/H	H/H	H/H		
		128	L/H	H/H	H/H	H/H	H/H	
		256	L/H	H/H	H/H	H/H	H/H	
		512	L/H	H/H	H/H	H/H	H/H	H/H
		1024	L/H	H/H	H/H	H/H	H/H	H/H
	01	16	L/L	L/H	H/H			
		32	L/L	L/H	H/H	H/H		
		64	L/L	L/H	H/H	H/H		
		128	L/L	L/H	H/H	H/H	H/H	
		256	L/L	L/H	H/H	H/H	H/H	
		512	L/L	L/H	H/H	H/H	H/H	H/H
		1024	L/L	L/H	H/H	H/H	H/H	H/H
	10	16	L/L	L/L	L/H			
		32	L/L	L/L	L/L	L/H		
		64	L/L	L/L	L/L	L/H		
		128	L/L	L/L	L/L	L/L	L/H	
		256	L/L	L/L	L/L	L/L	L/H	
		512	L/L	L/L	L/L	L/L	L/L	L/H
		1024	L/L	L/L	L/L	L/L	L/L	L/H
	11	16	Not Allowed					
		32	L/L	L/H	H/L	L/H		
		64	L/L	L/H	H/L	L/H		
		128	L/L	L/H	H/L	L/L	L/H	
		256	L/L	L/H	H/L	L/L	L/H	
		512	L/L	L/H	H/L	L/L	L/L	L/H
		1024	L/L	L/H	H/L	L/L	L/L	L/H

Notes: 1. H = HIGH
L = LOW

2. Pass "W" is the complex multiplication pass for FFT/IFFTs that perform complex multiplication prior to the transform.

Figure 3. Input/Clock Timing

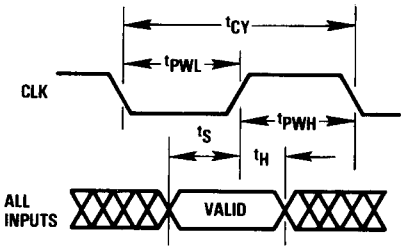


Figure 4. Read Cycle Timing

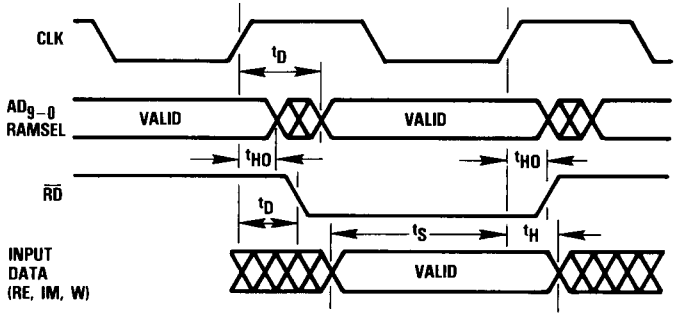


Figure 5. Write Cycle Timing

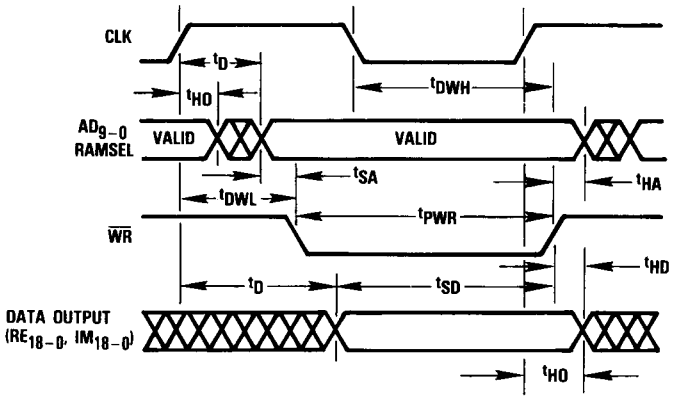
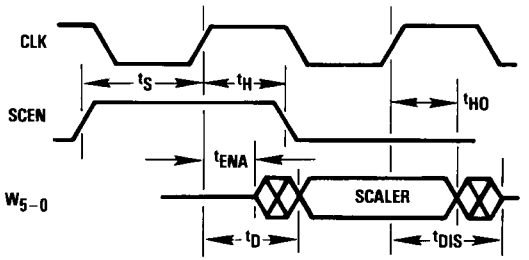


Figure 6. Scaler Timing



Transforms

Figure 7. RESET Timing

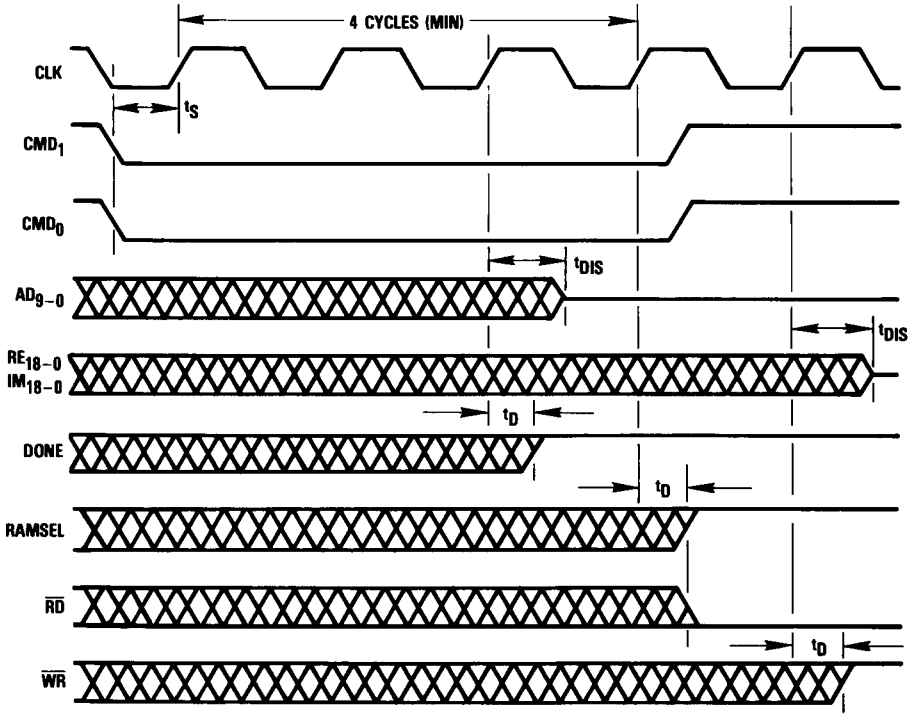


Figure 8. Configuration Register Load Timing

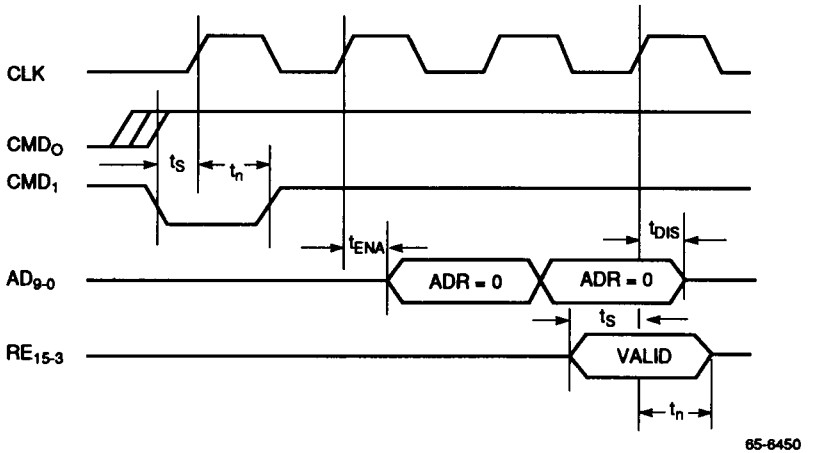


Figure 9. START Timing (Shown for FFT/IFFT with Windowing)

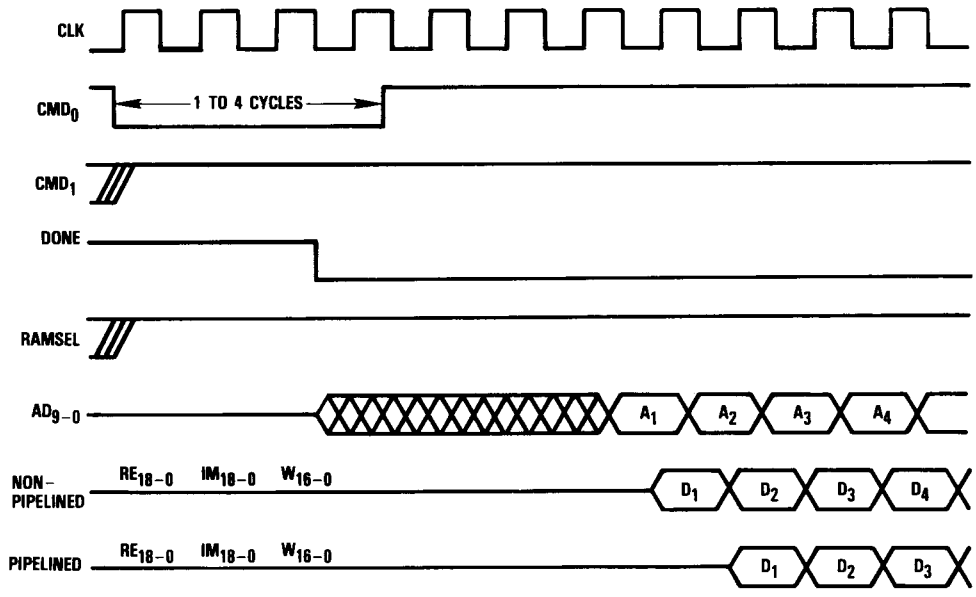


Figure 10. DONE Timing (Shown for FFT/IFFT)

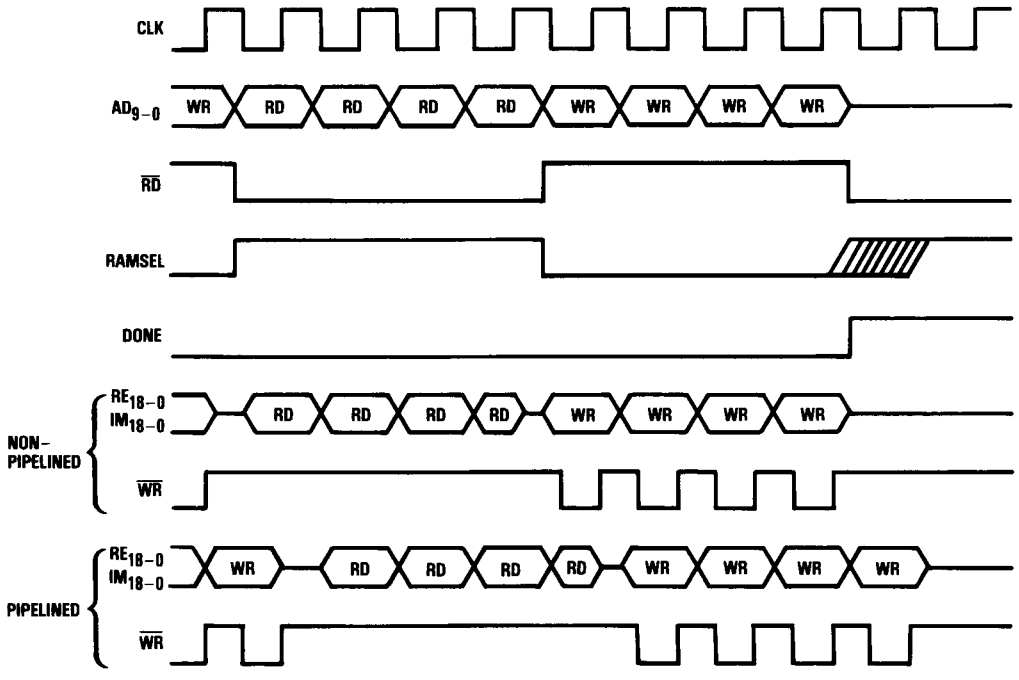
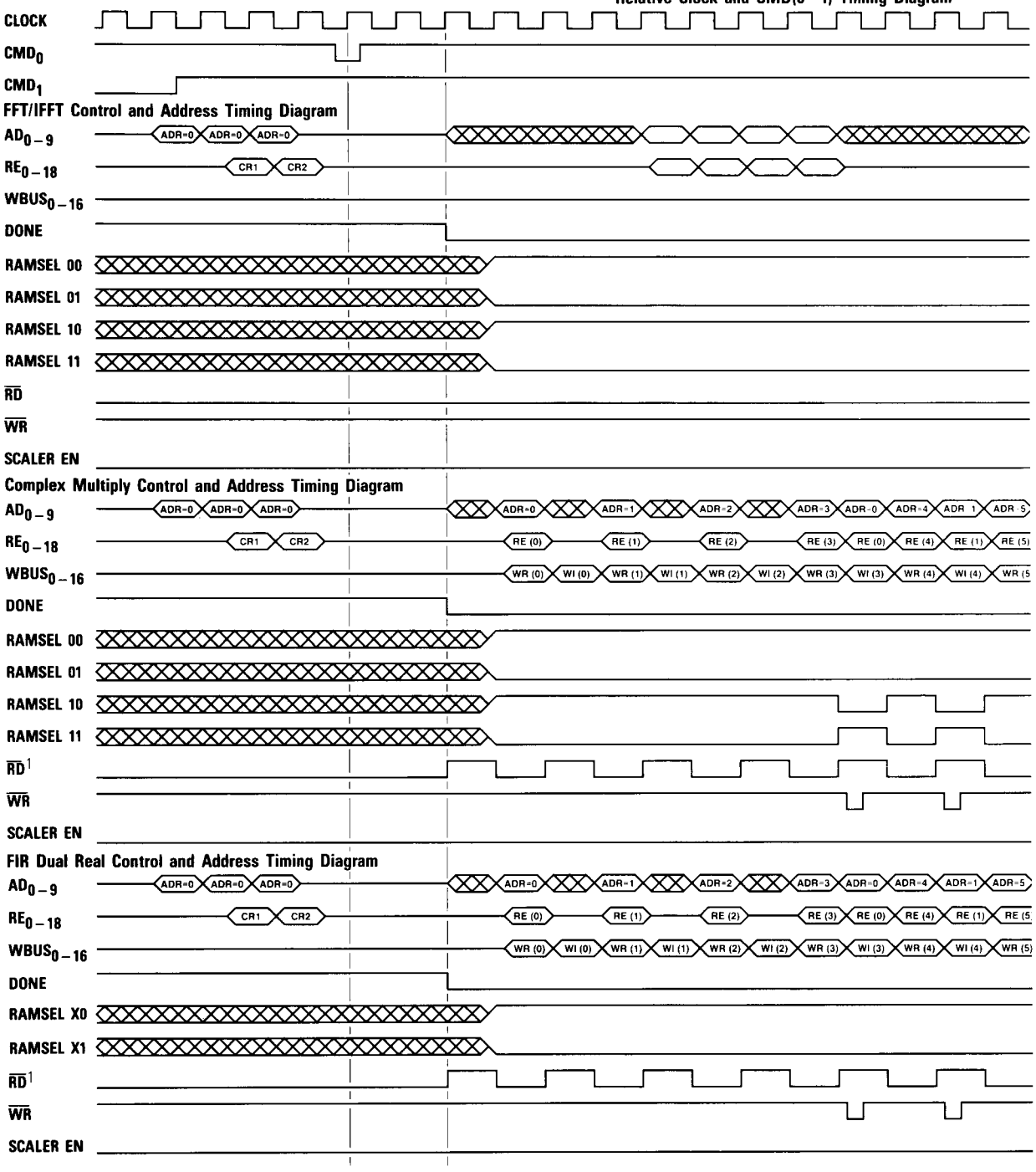


Figure 11. TMC2310 Overall Timing Diagram – Normal Addressing



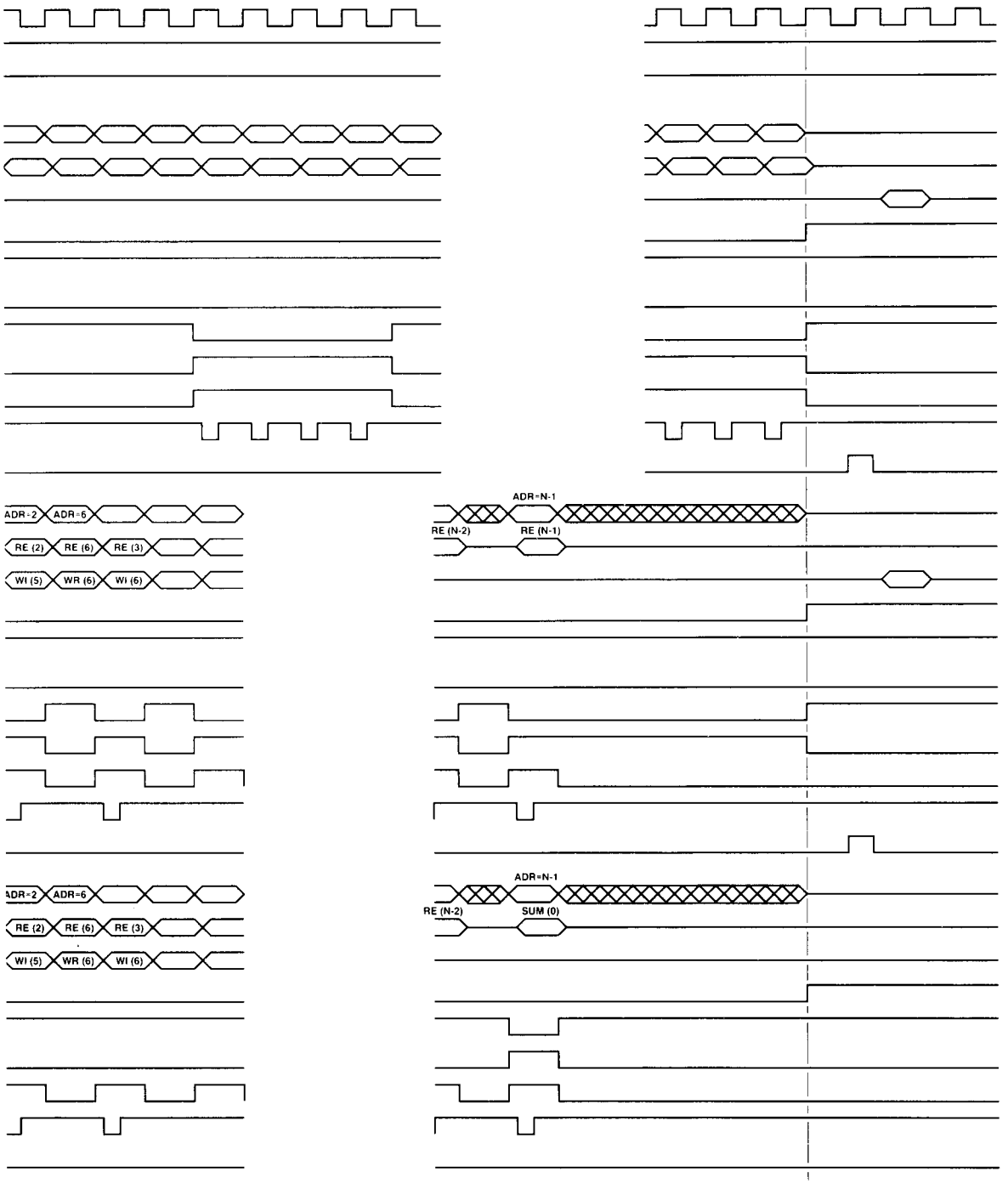
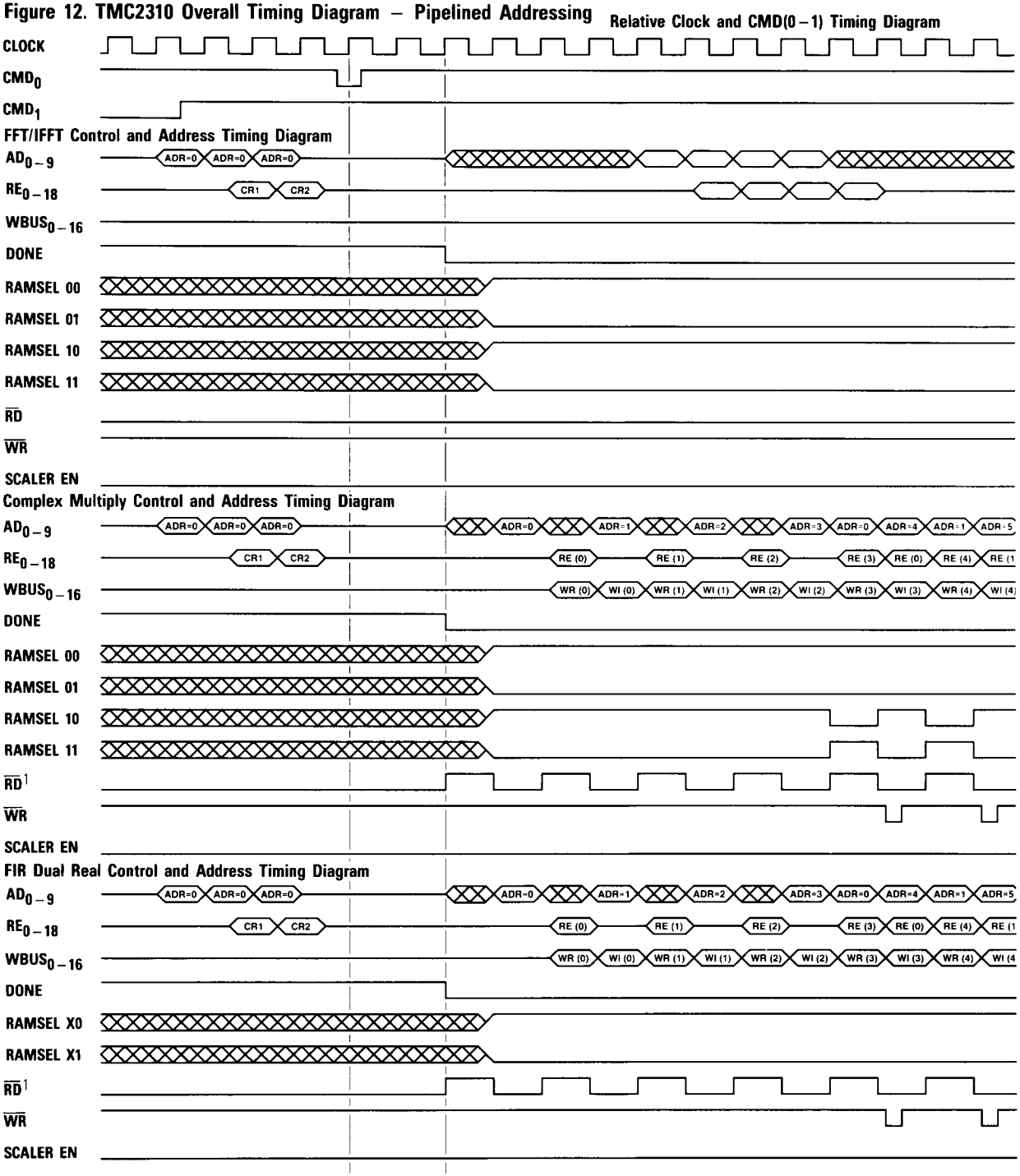

ADR=2
ADR=6
RE (2)
RE (6)
RE (3)
WI (5)
WR (6)
WI (6)
ADR=N-1
RE (N-2)
RE (N-1)
ADR=2
ADR=6
RE (2)
RE (6)
RE (3)
WI (5)
WR (6)
WI (6)
ADR=N-1
RE (N-2)
SUM (0)

Figure 12. TMC2310 Overall Timing Diagram – Pipelined Addressing



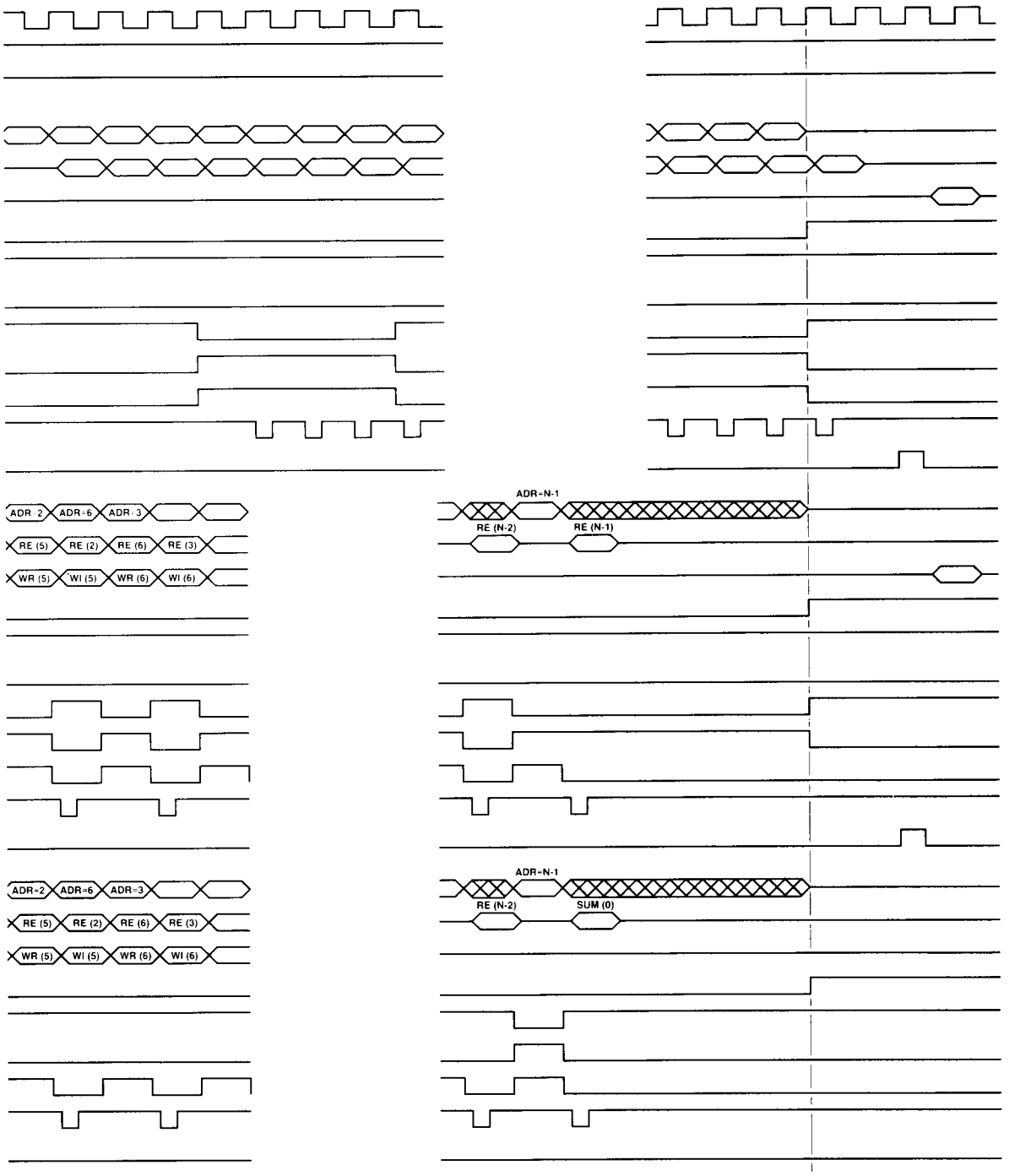

ADR-N-1
RE (N-2)
RE (N-1)
ADR-N-1
RE (N-2)
SUM (0)
ADR-2
ADR-6
ADR-3
RE (5)
RE (2)
RE (6)
RE (3)
WR (5)
WI (5)
WR (6)
WI (6)
ADR-2
ADR-6
ADR-3
RE (5)
RE (2)
RE (6)
RE (3)
WR (5)
WI (5)
WR (6)
WI (6)

Figure 13. Equivalent Input Circuit

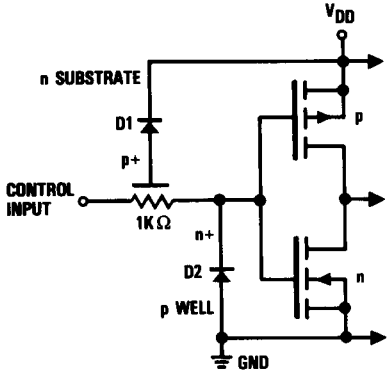
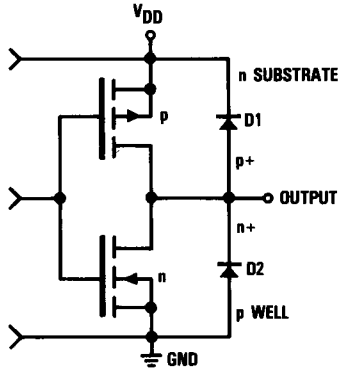


Figure 14. Equivalent Output Circuit



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage [2]	−0.5 to (V_{DD} + 0.5)V
Forced current [3,4]	−3.0 to 6.0mA
Short−circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	−60 to +130°C
junction	+175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Extended −1 Min	Extended −1 Nom	Extended −1 Max	Extended Min	Extended Nom	Extended Max	Units
V_{DD}	Supply Voltage	4.75	5.0	5.25				4.5	5.0	5.5	V
t_{CY}	Clock Cycle Time	50			50			66			ns
t_{PWH}	Clock Pulse Width HIGH	25			25			30			ns
t_{PWL}	Clock Pulse Width LOW	20			20			25			ns
t_S	Input Setup Time	7			9			11			ns
t_H	Input Hold Time	1			2			2			ns
V_{IL}	Input Voltage, Logic LOW			0.8						0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0						2.0			V
V_{IHC}	Input Voltage, Clock HIGH	2.2						2.3			V
I_{OL}	Output Current, Logic LOW			4.0						4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0						−2.0	mA
T_A	Ambient Temperature, Still Air	0		70							°C
T_C	Case Temperature							−55		125	°C

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V, DONE = HIGH		5		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 20MHz		150		160	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V		−10		−10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = 4mA		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = −2mA	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		−20		−20	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		20		20	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		−180		−180	mA
I_{OSW}	Short-Circuit Output Current for WR	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		−180		−180	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note: 1. Actual test conditions may vary from those shown, but guarantee operation as specified.

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended −1 Min	Extended −1 Max	Extended Min	Extended Max	Units
t_D	Delay Clock to Output	V_{DD} = Min, Load = 25pF							
		RE_{18-0}, IM_{18-0}		19		20		25	ns
		AD_{9-0}, RAMSEL		18		18		20	ns
		$\overline{RD}$, DONE		15		16		18	ns
		Scaler (W_{5-0})		32		38		40	ns
t_{HO}	Output Hold Time	V_{DD} = Min, Load = 25pF							
		RE_{18-0}, IM_{18-0}	4				2		ns
		AD_{9-0}, RAMSEL	4				2		ns
		$\overline{RD}$, DONE	2				2		ns
		Scaler (W_{5-0})	5				5		ns
t_{SA}	Setup Time AD_{9-0} to $\overline{WR}$ LOW	V_{DD} = Min, Load = 25pF	0				0		ns
t_{HA}	Hold Time AD_{9-0} to $\overline{WR}$ HIGH	V_{DD} = Min, Load = 25pF	10				5		ns
t_{SD}	Setup Time Data to $\overline{WR}$ HIGH (Data Valid to end of $\overline{WR}$)	V_{DD} = Min, Load = 25pF	24				22		ns
t_{HD}	Hold Time Data to $\overline{WR}$ HIGH (Data Hold from end of $\overline{WR}$)	V_{DD} = Min, Load = 25pF	10				10		ns
t_{PWR}	$\overline{WR}$ Pulse Width LOW	V_{DD} = Min, Load = 25pF	15				14		ns
t_{DWL}	Delay, Clock HIGH to $\overline{WR}$ LOW	V_{DD} = Min, Load = 25pF	11	25			10	28	ns
t_{DWH}	Delay, Clock LOW to $\overline{WR}$ HIGH	V_{DD} = Min, Load = 25pF	7	18				22	ns
t_{ENA}	Three-State Enable Delay	V_{DD} = Min, Load = 25pF		20				21	ns
t_{DIS}	Three-State Disable Delay	V_{DD} = Min, Load = 25pF		14				16	ns

Note: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Table 7. Performance Benchmarks

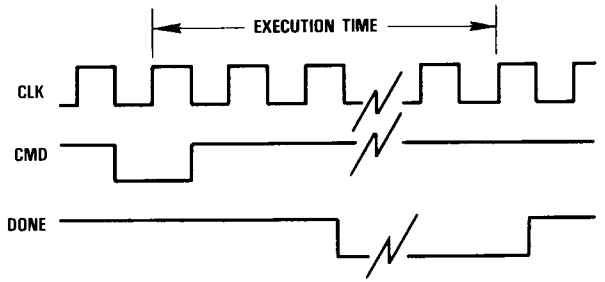
Operation	Number of Points	Execution [1] Cycles	Execution Cycles (Multiple Transform Mode)	Execution Time (20MHz)	Execution Time (20MHz) (Multiple Transform)
FFT/IFFT	16	87	64/Transform + 23	4.35 μS	3.2 μS/Transform + 1.25 μS
(Real Window/No Window)	32	223	192/Transform + 31	11.15 μS	9.6 μS/Transform + 1.55 μS
	64	415	384/Transform + 31	20.75 μS	19.2 μS/Transform + 1.55 μS
	128	1063	1024/Transform + 39	53.15 μS	51.2 μS/Transform + 1.95 μS
	256	2087	2048/Transform + 39	104.35 μS	102.4 μS/Transform + 1.95 μS
	512	5167	5120/Transform + 47	258.35 μS	256.0 μS/Transform + 2.35 μS
	1024	10,287	N/A	514.35 μS	N/A
FFT/IFFT	16	132	96/Transform + 36	6.6 μS	4.8 μS/Transform + 1.8 μS
(w/Complex Multiply)	32	300	256/Transform + 44	15.0 μS	12.8 μS/Transform + 2.2 μS
	64	556	512/Transform + 44	27.8 μS	25.6 μS/Transform + 2.2 μS
	128	1332	1280/Transform + 52	66.6 μS	64.0 μS/Transform + 2.6 μS
FIR Filtering	–		2 Cycles/Point + 9		100ns/Point + 450ns
Multiplication					
Multiply – Accumulate					
Magnitude Squared	–		2 Cycles/Point + 15		100ns/Point + 750ns

Note: 1. Execution times are valid for all FFT addressing and scaling modes.
Execution time is defined as the number of clocks from CMD = START until DONE = HIGH (see below).

The number of clock cycles is obtained in the following manner:

Clock Cycles = (Num. of Passes) • (2•Total Num. of Points) + (Num. of Passes) • 8 + 7
= (2•Total Num. of Butterflies) + (Processing Overhead).

Figure 15. Execution Cycle Time



Note: 1. For multiple transforms, the total time can be obtained by multiplying the value in the table by the number of concurrent transforms.
Example: 16 transforms of length 64 – points:
From Table 7.: 384 clocks per transform + 31 cycles overhead.
Therefore, the total number of cycles is:
Total = (384/transform) • (16 transforms) + 31 = 6175 cycles.

Applications

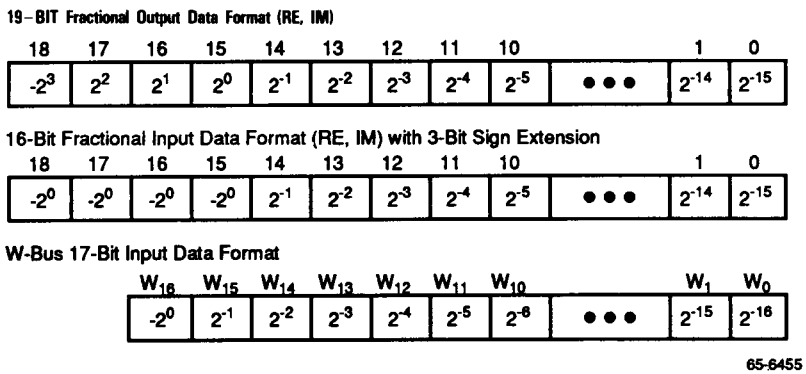
Data Formats

The input and output data formats are shown in Figure 16. Data are output on the RE and IM buses using the two's complement 19-bit data format. Input data must conform to the specified 16-bit data format detailed in Figure 16. During the first pass of any operation data input on the RE and IM buses may require scaling in order to be processed correctly by the device's arithmetic elements. Data input scaling parameters are specified according to the manual scale control set in CR1 or the input scaler select set in CR2. Only the sixteen Least Significant Bits (LSBs) or "shifted" LSBs can be used safely in the arithmetic elements. If no data shift is performed, bits RE_{15} and IM_{15} must be sign extended into the three Most Significant bits (RE_{18-16}, IM_{18-16}) to conform to the internal two's complement data buses. To perform FFTs the device supports an 18 x 17-bit multiply. However, inputs exceeding the 16-bit formats shown above may produce an intermediate overflow within the device's arithmetic elements.

The user is responsible for monitoring and accommodating data overflow for single pass instructions and for multiple pass transforms which utilize manual scaling. During multiple pass transforms, shifting can also be performed automatically (except for the first pass) by selecting the auto scale feature. If an operation may cause an overflow, sufficient memory width must be provided or data shifting performed to prevent loss of significant data. However, certain operation never cause overflow. For example, multiplication of two inputs which are both less than 1.0 will produce a result of less than 1.0. Since the MSBs of the output will always be a sign extension of the result, they can be ignored. This can simplify the memory arrangement by allowing the use of 16-bit memory systems (see Interfacing to Memory).

The W-Bus data may be reduced to 16-bit format to simplify memory interfacing. To maintain maximum accuracy, this can be accomplished in one of two ways. If using only positive window or filter coefficients, the MSB (W_{16}) may be connected to GND through a pull-down resistor (see Interfacing to 16-Bit Memory Systems). If both positive and negative coefficients are used, the LSB (W_0) can be connected to GND through a pull-down resistor.

Figure 16. Data Bus Formats



FIR Filter Operation

The TMC2310 performs both adaptive and non-adaptive coefficient Finite Inpulse Response (FIR) filters by performing a linear convolution between filter coefficients and input data. External data memory is used to store data samples and coefficients. For an N-tap filter, the data (RE, IM) memory retains the N most recent data samples and the window/coefficient memory stores the N filter coefficients.

The output of an N-tap, FIR filter is given by the convolution equation:

$$y(n-N+1) = \sum_{k=0}^{N-1} h(k)x(n-k)$$

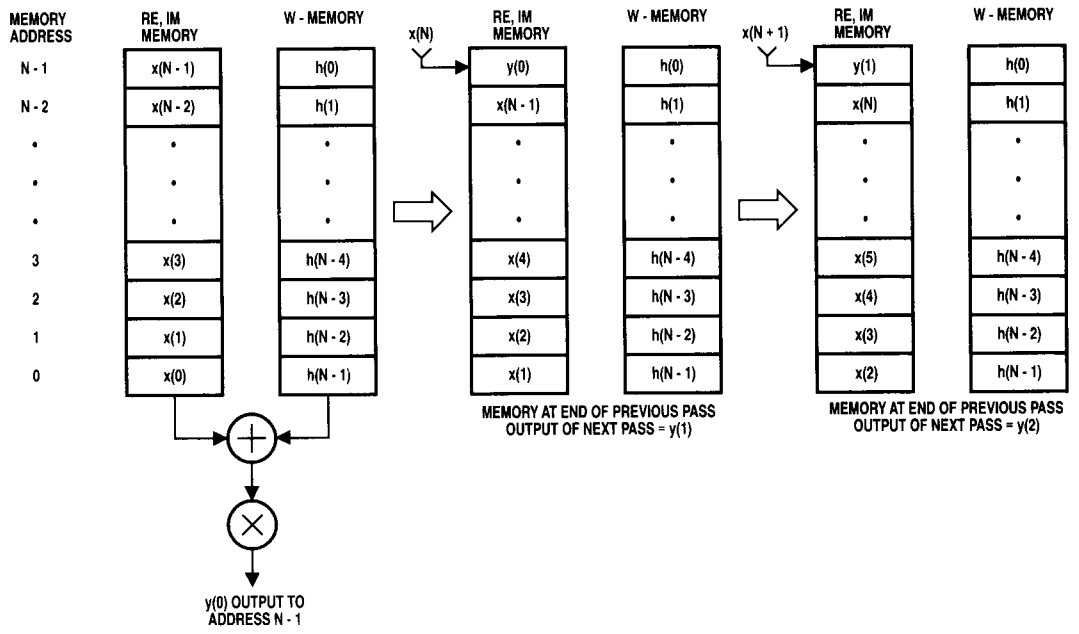
The convolution is accomplished by multiplying data in the RE and IM memories with filter coefficients stored in external RAM or ROM and input on the W-Bus. During the multiplication/accumulation, the RE and IM data are shifted down in memory by one address in preparation for the next pass.

At the start of a pass, the N-most recent data samples (x(n)) are stored in memory addresses from 0 through N−1 in ascending order (oldest sample in address 0).

The filter coefficients are stored in window/coefficient memory in corresponding addresses but in reversed order. After the START command, the coefficients and data are multiplied and accumulated term-by-term, while each value in RE and IM memory is shifted down by one memory location (with RAMSEL=HIGH). Upon completion of the pass, the RE and IM data have been shifted by one location, and the final accumulated result (y(n)) is output to address=N−1 with RAMSEL=LOW. In preparation for the next pass, the result at memory address N−1 is read by the host system. Execution stops at the end of each pass to allow time to read this result and to load the next data sample. To produce the next convolution output, this new data input is stored in location N−1, and a START command is re-issued. This operation is repeated for each output point y(n).

A diagram of the ordering of data samples and filter coefficients before and after successive passes is shown in *Figure 17*. An examination of the arrangement of coefficients (h(k)) and data samples (x(n)) shows that the FIR filter equation is calculated by summing the product of filter coefficients and data points in corresponding addresses.

Figure 17. FIR Filter Operation



FIR Filter Operation (cont.)

The filter order (tap length) is set by the "single transform length" and "number of transform" parameters in CR1 and CR2 respectively. The allowable filter sizes are 16 to 1024 taps, in multiples of 16. The throughput rate is two clock cycles per tap, per channel.

Both the 2-Real and Real/Imaginary FIR filtering are performed as described above. The "FIR 2-Real" (CR1[14:11] = 1001) instruction utilizes one set of filter coefficients for both the $RE_{18\text{-}0}$ and $IM_{18\text{-}0}$ data. The FIR Real-Imaginary instruction allows the use of separate filter coefficients for RE and IM data. This allows simultaneous filtering of two independent Real data sets with different filter functions. Coefficients for each set are input on alternate clock cycles through the W-Bus with the use of the $\overline{RD}$ option available in CR2[4].

Adaptive FIR Filtering

Adaptive FIR filtering modifies the filter coefficients concurrently with the convolution. Adaptive filtering operates differently from non-adaptive FIR filtering. As indicated before, the output y(n), can be obtained by convolving input data with filter coefficients:

$$y(n) = \sum_{k=0}^{N-1} h'(k)x(n-k)$$

Adaptive filters produce an error term for each filter output:

[Actual Filter Output] − [Desired Filter Output] = Error

or,

$$y(n) - y(n)' = \sigma(n)$$

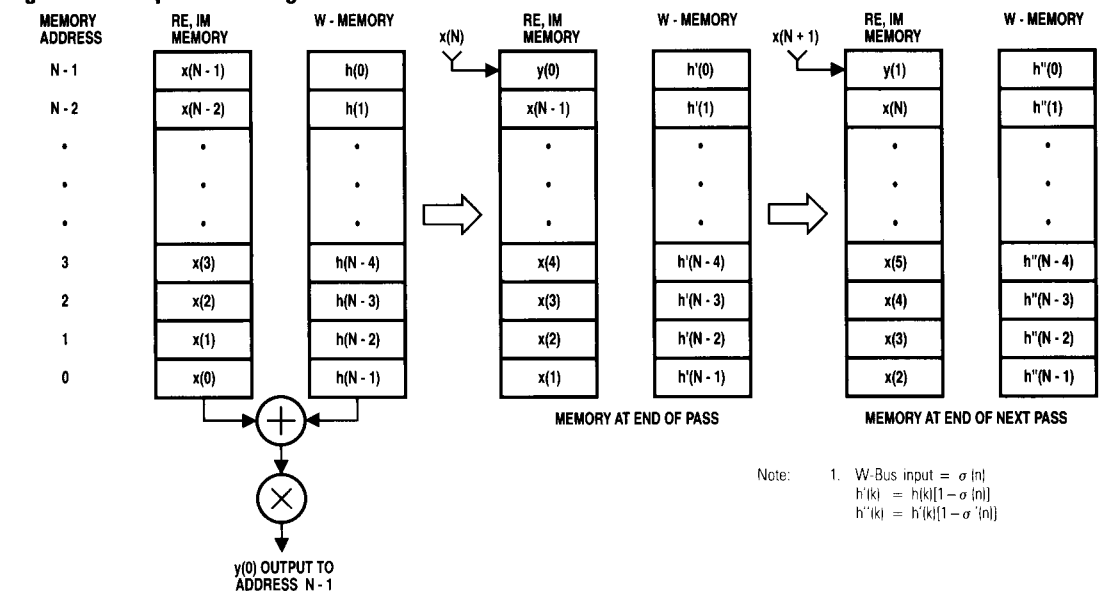
The error term is used to update the filter coefficients for the next data pass. The memory arrangement for adaptive filtering uses the RE memory for data storage and IM memory for existing and modified filter coefficients. During the pass, the data (x(n)) are shifted down one address in memory while the product of data and coefficients is being accumulated (with RAMSEL = HIGH). Concurrent with the determination of the convolution sum and the data shifting in the RE data memory, the filter coefficients are modified by the function:

$$h'(n) = [1 - \sigma(n)]h(n)$$

Where the h' are the filter coefficients used for the next pass.

The update value σ is input on the W-Bus on every read cycle and the modified filter coefficients are stored in IM memory. The operation is shown in ***Figure 18***.

Figure 18. Adaptive Filtering



Note: 1. W-Bus input = $\sigma(n)$
$h'(k) = h(k)[1 - \sigma(n)]$
$h''(k) = h'(k)[1 - \sigma'(n)]$

Interfacing to Memory

Using the TMC2310 with Lower Resolution Data

The TMC2310 allows data inputs of up to 16 bits for all operations without the risk of an internal overflow. When using data values that are smaller than 16 bits it is recommended that they be placed in the upper MSBs of the RE and IM data ports. For instance, when using 12-bit initial inputs for an FFT operation the real and imaginary data should be placed on both RE_{18-7} and IM_{18-7}, respectively. Using the upper MSBs of each 19-bit data port allows the device to operate in either the AUTO or MANUAL scale mode. Configuration Register 1, CR1[4:3], must be set to perform a right shift of 3 bits on the data input during the first pass. Results from the first pass have the potential of growing up to 19 bits, therefore, to maintain maximum precision the outputs should be contained in 19-bit wide memory.

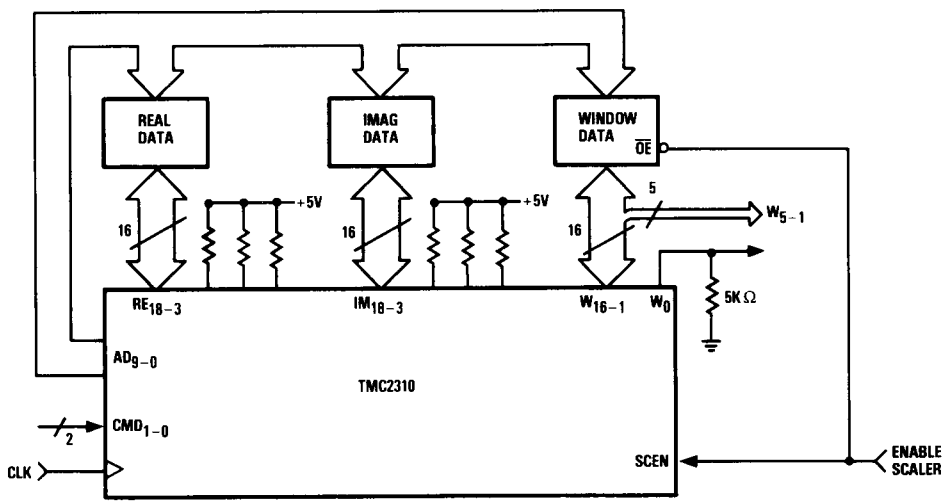
Initial data inputs can be connected to the 12 LSBs, however, since the device uses a two's complement data format each input must be sign extended into RE_{18} and IM_{18}, the MSBs. For operations that require multiple passes (i.e., FFT/IFFT) intermediate results will carry less precision. This will result in a reduction in the overall accuracy of the transform operation.

Interfacing to 16-Bit Memory Systems

The TMC2310 outputs 19 bits of significant data to external memory in order to increase arithmetic precision and minimize roundoff error. To obtain the best results, the memory system should support all 19 data bits. In order to reduce the number of memory devices, the system can be configured with 16-bit wide data memories. While this configuration may reduce system size and cost, there will be a decrease in accuracy due to truncation of the output data. In a 16-bit memory system, data should be left-justified (connected to the 16 MSBs) with the 3 LSBs connected to pull-up (or pull-down) resistors. Configuration Register 1 is programmed to perform auto or manual data scaling with a right shift of 3 bits performed on the data during the first pass (CR[4:3]=11). The 16 MSBs of the output are stored into memory, truncating the three LSBs.

In systems utilizing data windowing, the user may connect either the LSB or the MSB of the W-Bus to ground through a pull-down resistor of 5 kOhms. If both positive and negative window values are to be used, the MSB is required (two's complement format) and the LSB may be grounded. For positive magnitude window functions, the MSB will always be zero, and can therefore be connected to ground through a 5 kOhm resistor.

Figure 19. Interfacing to 16-Bit Memories



Pipelined vs. Non-Pipelined Addressing

Operation of the TMC2310 at its maximum clock rate requires the use of high-speed data memory. By including a special addressing mode, slower memory can be used by the addition of high-speed external address registers. The TMC2310 has been designed to allow the user to make system tradeoffs between memory cost and device count.

Normally, a memory address is output and the data strobed into or out of memory within a single clock cycle. Therefore, the following relationship must be met:

$$t_{CY} \quad [t_{DO}(\text{TMC2310 Addr. Out}) + t_{ACC}(\text{memory}) + t_S(\text{TMC2310 Data In})]$$

or equivalently, the memory access time must meet the requirement:

$$t_{ACC}(\text{memory}) \quad [t_{CY} - t_D(\text{TMC2310}) - t_S(\text{TMC2310})]$$

Use of the "Pipelined Addressing" mode alters the above relationship. In pipelined mode, the address and controls ($\overline{RD}$ and RAMSEL) appear one cycle earlier. For a read operation, the data will be input to the TMC2310 on the following cycle. For a write operation, the output data and the $\overline{WR}$ strobe will occur one cycle after the address and controls. For proper synchronization, the address, $\overline{RD}$ and RAMSEL outputs must be externally registered. The requirement for external memory speed becomes:

$$t_{ACC}(\text{memory}) \quad [t_{CY} - t_D(\text{external register}) - t_S(\text{TMC2310})]$$

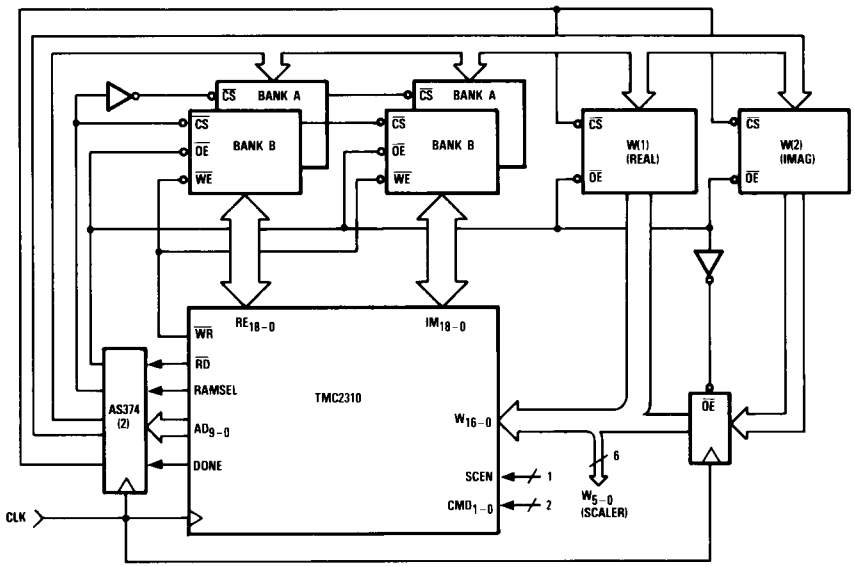
By substitution of the appropriate parameters into the above equation, it can be seen that the use of an external high-speed register ('AS374, F374, etc.) results in a substantial reduction of memory speed (access time) requirements.

Typical System Configuration

Figure 20 shows a typical system configuration utilizing many of the described techniques. The system includes "pipelined addressing", evident by the use of external registers on the TMC2310 memory address and controls. The system also includes a banked (Bank A and Bank B) memory system which may consists of single port or multi-port memory. (External host interface to memories is not shown.)

Finally, the diagram shows a system utilizing two window memories (for dual real and complex operations). If only one window memory is required (Real Windows) then the Imaginary memory, W(2), and associated output register and inverter may be deleted. For a single window memory, the chip select of W(1) can be connected to a LOW and the output enable connected to the DONE flag to disable the memory when the device is idle.

Figure 20. Typical System Configuration



Applications Information

System Memory Options

Single-port memories for both real and imaginary data can be used with the TMC2310. If single port memories are used, system performance will depend not only on the time required to perform the operation but also the time required to load and unload the memory. Systems requiring continuous operation are better supported with dual-port memories. This approach allows data to be loaded into, for example, the upper 1K portion of a 2K deep memory while the TMC2310 is operating on data in the lower 1K addresses. This technique eliminates the need for arbitration logic available in some dual-port memory. It is recommended that the device be used in the Pipelined Addressing mode to eliminate bus contention between the TMC2310 and the local real and imaginary data memory.

Memory Interface

When determining system memory requirements, the user must also take into account the Bit Reversion necessary to perform the FFT. Either the data must be stored in bit-reversed memory locations prior to performing the FFT, or the TMC2310 must perform the bit-reversal of the addresses when accessing the real and imaginary data on the first pass of the FFT. If data are loaded into memory in bit-reversed locations, the system can be operated using only 1 bank of memory. By supporting an additional bank of real and imaginary memory, the user has the option of allowing the bit reversal of the addresses to be performed by the TMC2310. This is a more efficient approach since it allows the host to load the inputs into one bank and unload the results from the other bank. Enabling and disabling of the memory banks is controlled by the RAMSEL flag provided by the TMC2310.

The operation of the RAMSEL flag is determined in conjunction with the bit reverse option. The user can determine the bank where the final results will be written with the Source/Target Memory Select option in Configuration Register 2. If bit-reversal is performed by the TMC2310, the RAMSEL flag will toggle in such a way as to move the intermediate and/or final results into the second bank of the memory. If the data are loaded into bit-reversed locations of the memory initially, then the RAMSEL flag can be used as a signal to indicate when the final results are being written. CR1[7:6]=10, CR2[6:5]=1X. (In this configuration the results will be written to bit-reversed locations).

Rescaling

After the memory configuration scheme has been defined the user can now tackle the issue of memory resolution. Although the device achieves maximum Signal-to-Noise performance using 19-bit wide memories excellent performance can still be attained using narrower memory. A common application is to use 16-bit memories interfaced to the upper 16 MSBs of each 19-bit data port. Independent of the memory width, rescaling of the data during the computation is necessary to prevent overflow. Signal-to-noise is maximized when the **auto scale** feature is activated, however, the user must then extract the scaler information from the W-Bus so that the proper order of magnitude of the data can be determined. Per definition of the FFT, a shift (or rescale) of 2 bits performed following every second radix-2 butterfly is sufficient to maintain accuracy without the threat of overflow. The TMC2310 supports this mode of operation with the **manual scale** option. For example, when using 12-bit inputs the initial data should be loaded into the memory with MSB at RE_{17}/IM_{17}. RE_{18} and IM_{18} are just sign extensions of RE_{17} and IM_{17}, while $RE_{4\text{-}0}$ and $IM_{4\text{-}0}$ should be set to zero. The initial shift performed at the beginning of the first pass will then have no effect on the data. Subsequent passes will each be rescaled by 2 bits following the butterfly operations. Use the following settings: **CR1[5]=1, CR1[4:3]=10**.

Using the TMC2310 with 17-bit Inputs

For non-FFT applications the device can support 17-bit wide inputs while returning valid results. For convolution operation (i.e., MPY-ACC and FIR modes) the user must be careful not to exceed the accumulator width of the device. Input data can be placed into $RE_{16\text{-}0}$ and $IM_{16\text{-}0}$ of the two data ports. $RE_{18\text{-}17}$ are sign extensions of RE_{16} and $IM_{16\text{-}0}$ of the two data ports. $RE_{18\text{-}17}$ and $IM_{18\text{-}17}$ are sign extensions of RE_{16} and IM_{16} of the initial inputs. The data in the real and imaginary memory can also be interfaced to allow an initial shift of the inputs within the device prior to performing the desired operation. If the real and imaginary data are stored with the MSBs at RE_{17} and IM_{17}, sign extension will be supported internally in the device following the 2-bit shift, **CR1[4:3]=10**.

Generating a Write Pulse

The high-speed operation of the TMC2310 requires the use of fast random access memory. The TMC2310 provides a write enable pin for use with the local real and imaginary data memories. In some circumstances, it is necessary for the user to generate this write strobe to increase the pulse width to meet system requirements. As an alternative, the user can use the RD/ output to generate this write strobe since the RD/ signal is normally LOW and goes HIGH only during write cycles. The RD/Signal should be gated with the system clock to create an active LOW write (enable) strobe. If the device is to be used to implement Unwindowed or Real Windowed FFTs exclusively, then this method should achieve better system timing and performance.

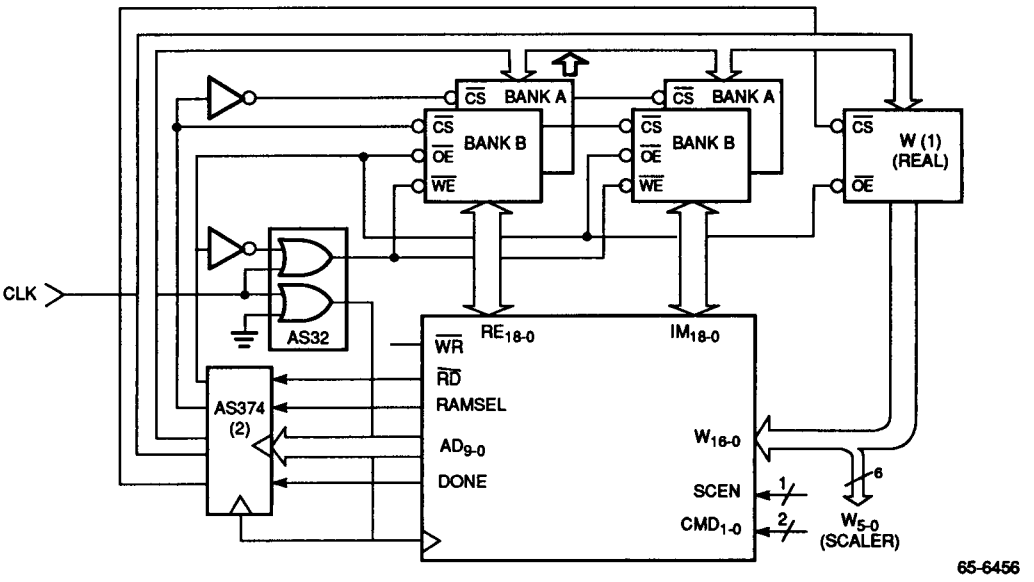


Figure 1. Memory Interface for FFT Systems

Generating a Write Pulse (continued)

More general applications, particularly those that require (2) window coefficient memories (i.e., Complex MPY, RE/IM MPY-ACC etc.), require an alternative circuit for Write strobe generation. The TMC2310 contains an option in CR2 that changes the operation of the RD/ signal. Under normal operations **CR2[4]=0** the RD/ signal will not be activated until the first valid result appears at the real and imaginary data ports, after which RD/ will toggle on successive cycles. If activated, the RD/ signal will toggle following application of the START command so that W_R and W_I inputs can be synchronized with the falling and rising edge of the RD/, respectively. If it is necessary for the write strobe to be generated for these modes (including FFT/IFFT with Complex MPY) then an alternate circuit must be used. Specifically, if CR2[4]=1 RD/ will toggle every cycle and if the write strobe is created by gating RD/ with CLK then the device will incorrectly generate (4) write pulses during the first four read cycles writing over unprocessed data. The following circuit eliminates this situation by setting **CR2[4]=0**:

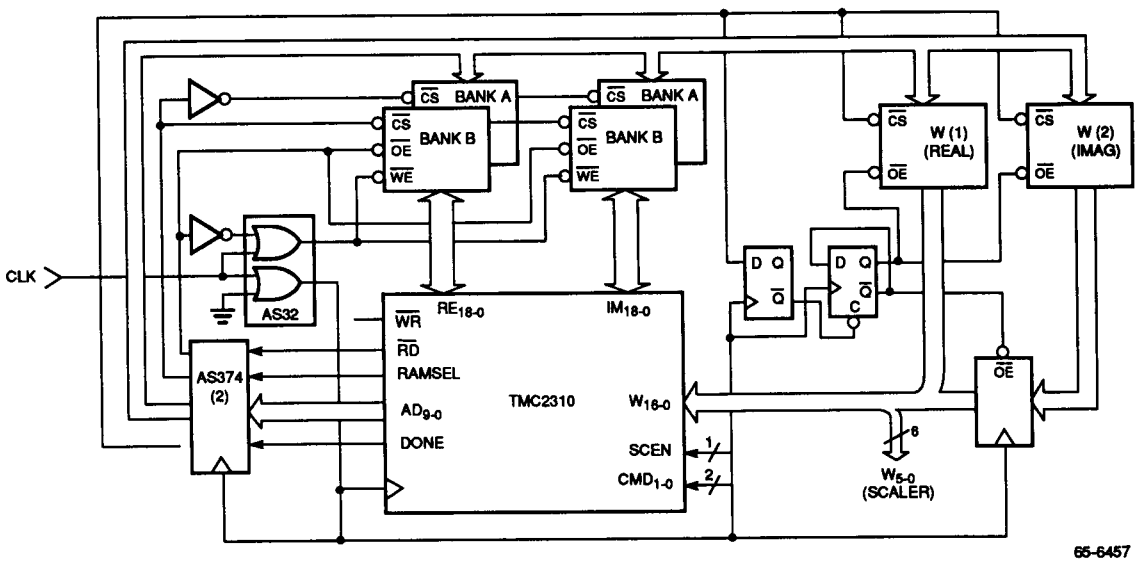


Figure 2. Memory Interface for General Systems

Bit-Reverse Addressing Details

The radix – 2, Decimation – In – Time (DIT) FFT/IFFT algorithm performed by the TMC2310 requires data scrambling during the first butterfly pass (Refs. [2],[3]). The scrambling amounts to a bitwise reversal of the address index during the first pass of the FFT. A flow diagram for a general, radix – 2, 16 – point FFT is shown in Figure 21. By a close examination of the figure, it can be seen that the first butterfly is performed on data points X(0) and X(8) with results stored in X(0) and X(1). It is apparent that results must be written to a secondary memory to prevent the loss of the unused data point X(1).

The TMC2310 allows several addressing options for transforms. While these modes have no effect on speed or processing time, they do affect system memory requirements. If the input data samples are stored in memory in sequential order, then the TMC2310 must perform the bit – reversed addressing (CR1[7:6] = 01) during the first butterfly pass. To accomodate the data scrambling and prevent overwriting of unused data, the user must provide additional "scratch pad" memory for intermediate storage during this pass. The RAMSEL output is used to toggle between the two banks during reads and writes of the first pass. RAMSEL must be connected either to the "chip enables" of separate memories or to an additional address line (for a paged memory system). At the completion of the transform, data will be in memory in sequential (frequency or time) order.

A transform can be done without the scratch pad memory by initially storing the data in scrambled order. This is accomplished by a simple reverse ordering of the address lines between the host system address generator (counters, etc.) and the data memory (Figure 22). The transform is then performed "in – place" (no bit – reverse, CR1[7:6] = 00). Since the input data has been "pre – scrambled", the TMC2310 will read and write data to memory addresses in a sequence that requires no additional memory. Final results will be available in sequential, frequency bin order. In either case, if windowing is performed, the user must store the window function either in sequential or scrambled order to match that of the input data.

Figure 21. 16 – Point FFT

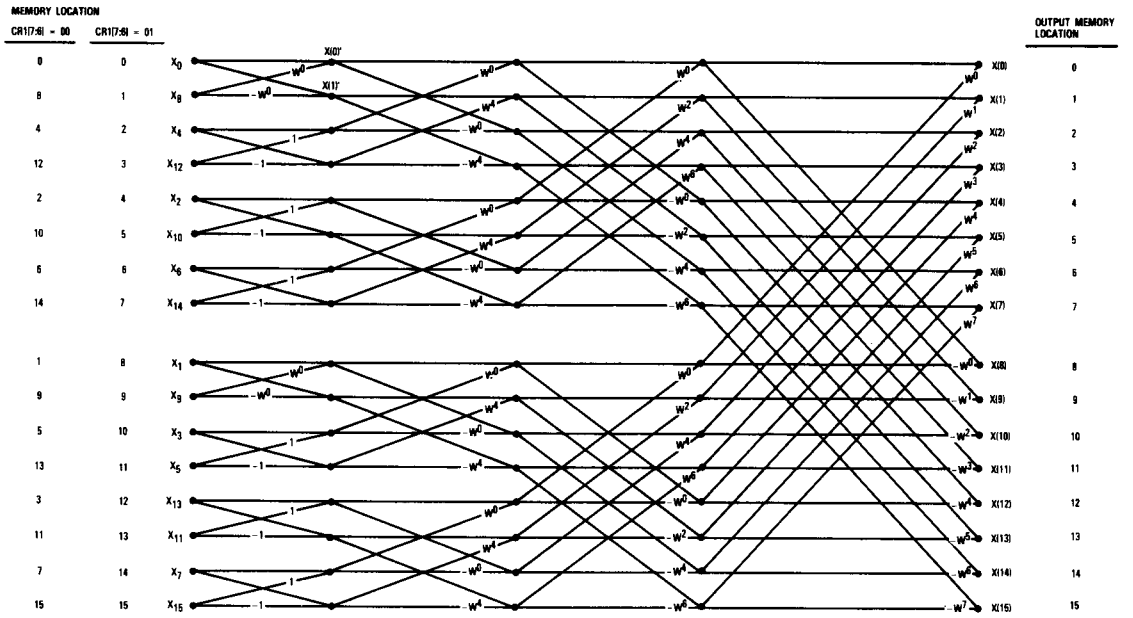
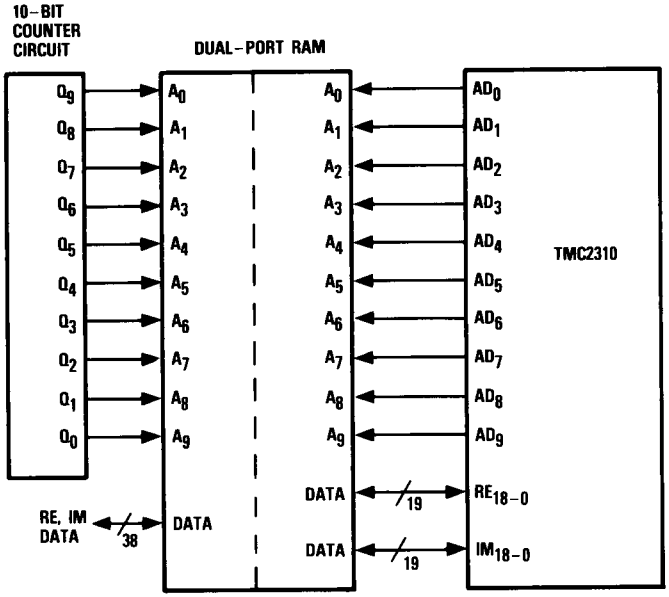


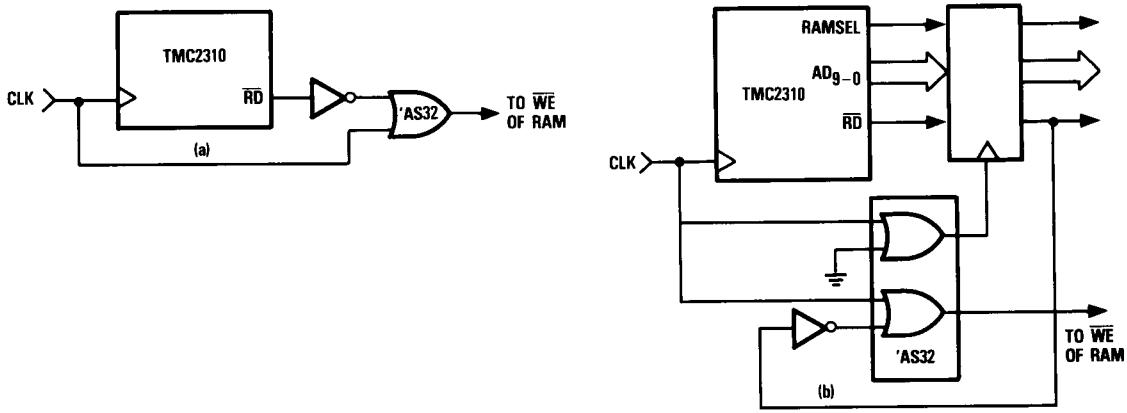
Figure 22. Bit-Reversed Input Data for 1024-Point Transform



Alternate Method For Write Strobe Generation

The high-speed operation of the TMC2310 requires the use of fast random addess memory. In some instances, the pulse-width and timing of the TMC2310's $\overline{WR}$ may not meet the system requirements. As an alternative, the user can use the $\overline{RD}$ output used to generate a write strobe for memory. Since $\overline{RD}$ is normally LOW and goes HIGH only during write cycles, the user can gate $\overline{RD}$ with the system clock to create an active LOW write (enable) strobe. Implementing the write strobe in this method may give better system timing and performance. The strobe will be the LOW portion of the system clock. *Figure 23, part (a)* shows external generation of a write strobe in non-pipelined addressing systems, and *part (b)* for pipelined systems utilizing the external address registers. The external register (74AS821) is clocked by a delayed system clock (through the AS32) to guarantee a valid memory address until WE goes HIGH.

Figure 23. Generating a Write Strobe



Scale Factor (W_{3-0})

In the inverse FFT, the final exponent read at this port will be the true binary exponent for the emerging real and imaginary data. In the forward FFT, this value will exceed the true exponent by N, where the total number of transform points is 2^N. The format for this exponent is 4-bit unsigned integer.

References

[1] Harris, F.J., "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform," Proceedings of the IEEE, Vol. 66, No. 1, January, 1978, pp 51-83.

[2] Oppenheim, A.V., Schafer, R.W., "Digital Signal Processing," Prentice-Hall, Inc., 1975.

[3] Rabiner, L.R., Gold, B., "Theory and Applications of Digital Signal Processing," Prentice-Hall, Inc., Copyright-Bell Laboratories.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2310G5V	EXT–T_C = –55°C to 125°C	MIL-STD-883, 15MHz	88 Pin Ceramic Pin Grid Array	2310G5V
TMC2310G5V1	EXT–T_C = –55°C to 125°C	MIL-STD-883, 20MHz	88 Pin Ceramic Pin Grid Array	2310G5V1
TMC2310H7C	STD–T_A = 0°C to 70°C	Commercial, 20MHz	89 Pin Plastic Pin Grid Array	2310H7C
TMC2310L4V	EXT–T_C = –55°C to 125°C	MIL-STD-883, 15MHz	100 Leaded Ceramic Chip Carrier	2310L4V
TMC2310L4V1	EXT–T_C = –55°C to 125°C	MIL-STD-883, 20MHz	100 Leaded Ceramic Chip Carrier	2310L4V1
TMC2310L6V	EXT–T_C = –55°C to 125°C	MIL-STD-883, 15MHz	132 Leaded CERQUAD	2310L6V
TMC2310L6V1	EXT–T_C = –55°C to 125°C	MIL-STD-883, 20MHz	132 Leaded CERQUAD	2310L6V1

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