32Mb F-die SLC NOR Specification

Document Title

32M Bit (2M x16) Muxed Burst / Multi Bank NOR Flash Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial issue	Nov. 18, 2007	Target
1.0	Specification is finalized.	April 17, 2008	Final
1.1	**H** : FBGA(Lead Free, OSP, Halogen Free) package code is added	October 07, 2008	Final
1.2	tCES in AC Parameter table is changed from Min. 4.0ns to Min. 4.5ns.	October 22, 2008	Final

Note : For more detailed features and specifications including FAQ, please refer to Samsung's web site.
http://samsungelectronics.com/semiconductors/products/products_index.html

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1.0 FEATURES

- Single Voltage, 1.7V to 1.95V for Read and Write operations
- Organization
  - 2,097,152 x 16 bit (Word Mode Only)
- Multiplexed Data and Address for reduction of interconnections
  - A/DQ0 ~ A/DQ15
- Read While Program/Erase Operation
- Multiple Bank Architecture
  - 16 Banks (2Mb Partition)
- OTP Block : Extra 256word block
- Read Access Time (@ C_L=30pF)
  - Asynchronous Random Access Time : 70ns
  - Synchronous Random Access Time : 70ns
  - Burst Access Time :
    14.5ns (54MHz) / 11ns (66MHz) / 9ns (83Mhz) / 7ns (108Mhz)
- Burst Length :
  - Continuous Linear Burst
  - Linear Burst : 8-word & 16-word with Wrap
- Block Architecture
  - Eight 4Kword blocks and sixty three 32Kword blocks
  - Bank 0 contains eight 4 Kword blocks and three 32Kword blocks
  - Bank 1~Bank 15 contain sixty 32Kword blocks
- Reduce program time using the V_{PP}
- Support Single & Quad word accelerate program
- Power Consumption (Typical value, C_L=30pF)
  - Burst Access Current : 24mA
  - Program/Erase Current : 15mA
  - Read While Program/Erase Current : 40mA
  - Standby Mode/Auto Sleep Mode : 15uA
- Block Protection/Unprotection
  - Using the software command sequence
  - Last two boot blocks are protected by $\overline{WP}$=V_{IL}
  - All blocks are protected by V_{PP}=V_{IL}
- Handshaking Feature
  - Provides host system with minimum latency by monitoring RDY
- Erase Suspend/Resume
- Program Suspend/Resume
- Unlock Bypass Program/Erase
- Hardware Reset ($\overline{RESET}$)
- Data Polling and Toggle Bits
  - Provides a software method of detecting the status of program or erase completion
- Endurance
  - 100K Program/Erase Cycles Minimum
- Extended Temperature : -25°C ~ 85°C
- Support Common Flash Memory Interface
- Low Vcc Write Inhibit
- Package : Package : 44-ball FBGA Type, 7.5 x 5mm
  0.5 mm ball pitch
  1.0 mm (Max.) Thickness

2.0 GENERAL DESCRIPTION

The K8S3215E featuring single 1.8V power supply is 32Mbit Synchronous Burst Multi Bank Flash Memory organized as 2Mx16. The memory architecture of the device is designed to divide its memory arrays into 71 blocks with independent hardware protection. This block architecture provides highly flexible erase and program capability. The K8S3215E NOR Flash consists of sixteen banks. This device is capable of reading data from one bank while programming or erasing in the other bank.

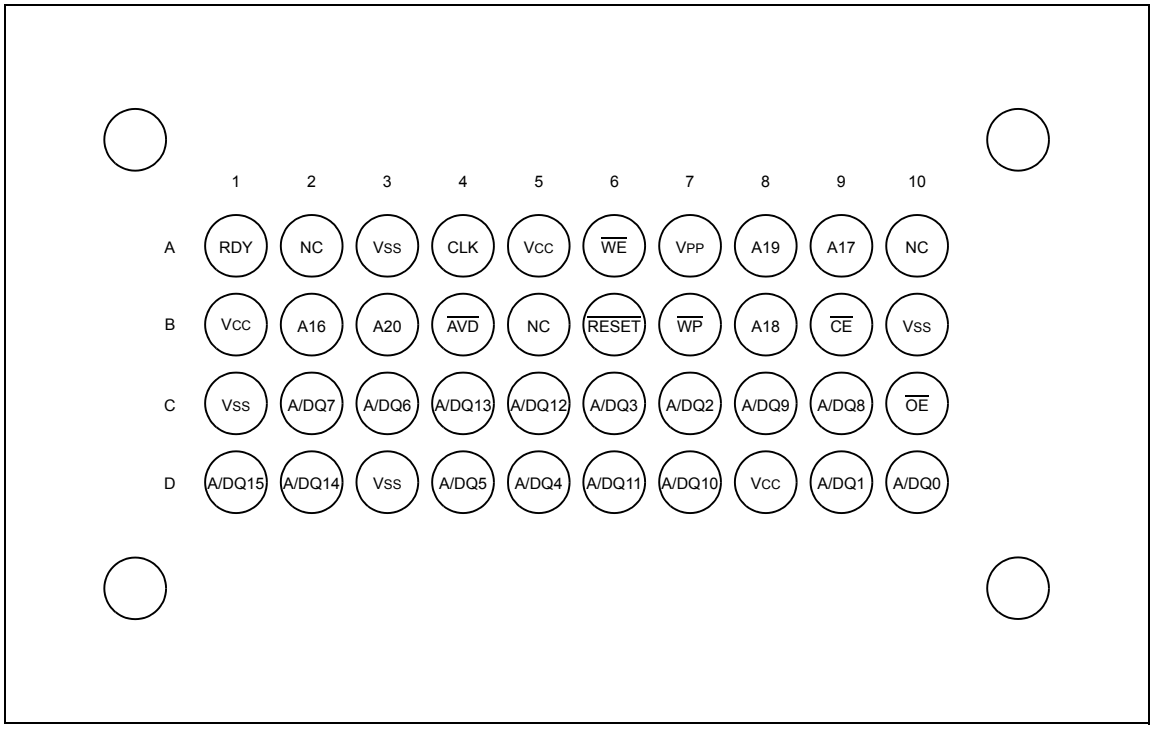
Regarding read access time, the K8S3215E provides an 14.5ns burst access time and an 70ns initial access time at 54MHz. At 66MHz, the K8S3215E provides an 11ns burst access time and 70ns initial access time. At 83MHz, the K8S3215E provides an 9ns burst access time and 70ns initial access time. At 108MHz, the K8S3215E provides an 7ns burst access time and 70ns initial access time. The device performs a program operation in units of 16bits (Word) and an erase operation in units of a block. Single or multiple blocks can be erased. The block erase operation is completed within typically 0.7sec. The device requires 15mA as program/erase current in the extended temperature ranges.

The K8S3215E NOR Flash Memory is created by using Samsung's advanced CMOS process technology.

3.0 PIN DESCRIPTION

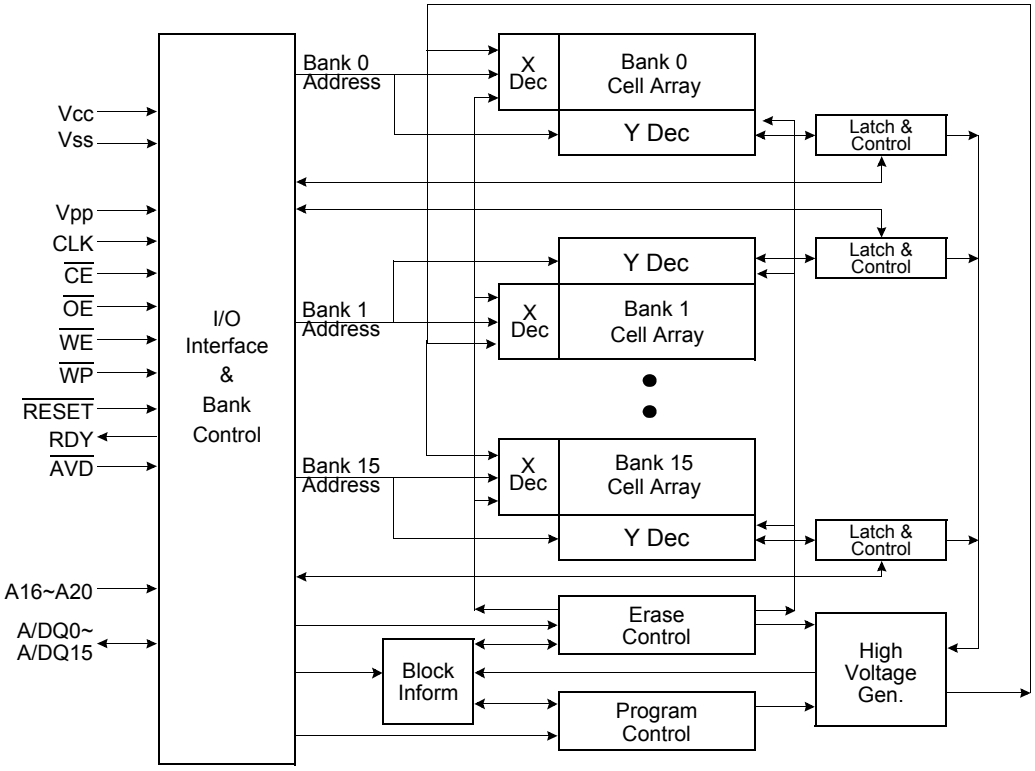
Pin Name	Pin Function
A16 - A20	Address Inputs
A/DQ0 - A/DQ15	Multiplexed Address/Data input/output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{RESET}$	Hardware Reset Pin
VPP	Accelerates Programming
$\overline{WE}$	Write Enable
$\overline{WP}$	Hardware Write Protection Input
CLK	Clock
RDY	Ready Output
$\overline{AVD}$	Address Valid Input
VCC	Power Supply
VSS	Ground

4.0 PIN CONFIGURATION

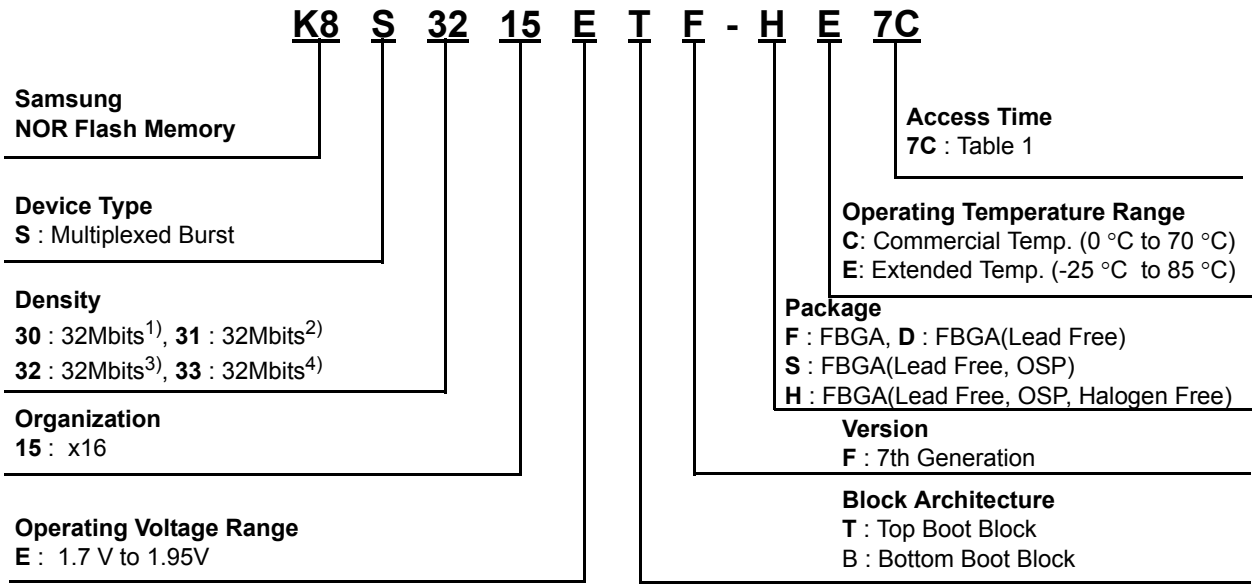


44Ball FBGA TOP VIEW (BALL DOWN)

5.0 FUNCTIONAL BLOCK DIAGRAM



6.0 ORDERING INFORMATION



NOTE :
Density : (1) 30 : 32Mb with the Sync MRS option (Extended Configuration Register)
(2) 31 : 32Mb with Enhanced block protection option
(3) 32 : 32Mb with no option
(4) 33 : 32Mb with the Sync MRS (Extended Configuration Register) and Enhanced block protection option

Table 1: PRODUCT LINE-UP

K8S3215E						
	Mode	**Speed Option**	**7B (54MHz)**	**7C (66MHz)**	**7D (83MHz)**	**7E (108Mhz)**
V_{CC}=1.7V-1.95V	Synchronous/Burst	Max. Initial Access Time (t_{IAA}, ns)	70	70	70	70
		Max. Burst Access Time (t_{BA}, ns)	14.5	11	9	7
	Asynchronous	Max. Access Time (t_{AA}, ns)	70	70	70	70
		Max. $\overline{CE}$ Access Time (t_{CE}, ns)	70	70	70	70
		Max. $\overline{OE}$ Access Time (t_{OE}, ns)	20	20	20	20

Table 2: K8S3215E DEVICE BANK DIVISIONS

Bank 0		Bank 1 ~ Bank 15	
Mbit	**Block Sizes**	**Mbit**	**Block Sizes**
2 Mbit	Eight 4Kwords, Three 32Kwords	30 Mbit	Sixty 32Kwords

Table 3: K8S3215ETF DEVICE BANK DIVISIONS

Bank	Quantity of Blocks	Block Size
0	8	4 Kwords
	3	32 Kwords
1	4	32 Kwords
2	4	32 Kwords
3	4	32 Kwords
4	4	32 Kwords
5	4	32 Kwords
6	4	32 Kwords
7	4	32 Kwords
8	4	32 Kwords
9	4	32 Kwords
10	4	32 Kwords
11	4	32 Kwords
12	4	32 Kwords
13	4	32 Kwords
14	4	32 Kwords
15	4	32 Kwords

Table 4: K8S3215EBF DEVICE BANK DIVISIONS

Bank	Quantity of Blocks	Block Size
15	4	32 Kwords
14	4	32 Kwords
13	4	32 Kwords
12	4	32 Kwords
11	4	32 Kwords
10	4	32 Kwords
9	4	32 Kwords
8	4	32 Kwords
7	4	32 Kwords
6	4	32 Kwords
5	4	32 Kwords
4	4	32 Kwords
3	4	32 Kwords
2	4	32 Kwords
1	4	32 Kwords
0	3	32 Kwords
	8	4 Kwords

7.0 PRODUCT INTRODUCTION

The K8S3215E is a 32Mbit (33,554,432 bits) NOR-type Burst Flash memory. The device features 1.8V single voltage power supply operating within the range of 1.7V to 1.95V. The device is programmed by using the Channel Hot Electron (CHE) injection mechanism which is used to program EPROMs. The device is erased electrically by using Fowler-Nordheim tunneling mechanism. To provide highly flexible erase and program capability, the device adapts a block memory architecture that divides its memory array into 71 blocks (32-Kword x 63, 4-Kword x 8). Programming is done in units of 16 bits (Word). All bits of data in one or multiple blocks can be erased when the device executes the erase operation. To prevent the device from accidental erasing or over-writing the programmed data, 71 memory blocks can be hardware protected.Regarding read access time, at 54MHz, the K8S3215E provides a burst access of 14.5ns with initial access times of 70ns at 30pF. At 66MHz, the K8S3215E provides a burst access of 11ns with initial access times of 70ns at 30pF. At 83MHz, the K8S3215E provides a burst access of 9ns with initial access times of 70ns at 30pF. At 108MHz, the K8S3215E provides a burst access of 9ns with initial access times of 70ns at 30pF. The command set of K8S3215E is compatible with standard Flash devices. The device uses Chip Enable ($\overline{CE}$), Write Enable ($\overline{WE}$), Address Valid($\overline{AVD}$) and Output Enable ($\overline{OE}$) to control asynchronous read and write operation. For burst operations, the device additionally requires Ready (RDY) and Clock (CLK). Device operations are executed by selective command codes. The command codes to be combined with addresses and data are sequentially written to the command registers using microprocessor write timing. The command codes serve as inputs to an internal state machine which controls the program/erase circuitry. Register contents also internally latch addresses and data necessary to execute the program and erase operations. The K8S3215E is implemented with Internal Program/Erase Routines to execute the program/erase operations. The Internal Program/Erase Routines are invoked by program/erase command sequences. The Internal Program Routine automatically programs and verifies data at specified address. The Internal Erase Routine automatically pre-programs the memory cell which is not programmed and then executes the erase operation. The K8S3215E has means to indicate the status of completion of program/erase operations. The status can be indicated via Data polling of DQ7, or the Toggle bit (DQ6). Once the operations have been completed, the device automatically resets itself to the read mode. The device requires 24mA burst read current and 15mA for program/erase operations.

Table 5: Device Bus Operations

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A16-20	A/DQ0-15	$\overline{RESET}$	CLK	$\overline{AVD}$
Asynchronous Read Operation	L	L	H	Add In	Add In/DOUT	H	L	
Write	L	H	L	Add In	Add In / DIN	H	L	
Standby	H	X	X	X	High-Z	H	X	X
Hardware Reset	X	X	X	X	High-Z	L	X	X
Load Initial Burst Address	L	H	H	Add In	Add In	H		
Burst Read Operation	L	L	H	X	Burst DOUT	H		H
Terminate Burst Read Cycle via $\overline{CE}$	H	X	X	X	High-Z	H	X	X
Terminate Burst Read Cycle via $\overline{RESET}$	X	X	X	X	High-Z	L	X	X
Terminate Current Burst Read Cycle and Start New Burst Read Cycle	L	H	H	Add In	Add In	H		

NOTE : L=VIL (Low), H=VIH (High), X=Don't Care.

8.0 COMMAND DEFINITIONS

The K8S3215E operates by selecting and executing its operational modes. Each operational mode has its own command set. In order to select a certain mode, a proper command with specific address and data sequences must be written into the command register. Writing incorrect information which include address and data or writing an improper command will reset the device to the read mode. The defined valid register command sequences are stated in Table 5.

Table 6: Command Sequences

Command Definitions		Cycle	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
Asynchronous Read	Add	1	RA					
	Data		RD					
Reset[5)]	Add	1	XXXH					
	Data		F0H					
Autoselect Manufacturer ID[6)]	Add	4	555H	2AAH	(DA)555H	(DA)X00H		
	Data		AAH	55H	90H	ECH		
Autoselect Device ID[6)]	Add	4	555H	2AAH	(DA)555H	(DA)X01H		
	Data		AAH	55H	90H	Table 10		
Autoselect Block Protection Verify [7)]	Add	4	555H	2AAH	(BA)555H	(BA)X02H		
	Data		AAH	55H	90H	00H/01H		
Autoselect Handshaking [16)]	Add	4	555H	2AAH	(DA)555H	(DA)X03H		
	Data		AAH	55H	90H	0H/1H		
Program	Add	4	555H	2AAH	555H	PA		
	Data		AAH	55H	A0H	PD		
Unlock Bypass	Add	3	555H	2AAH	555H			
	Data		AAH	55H	20H			
Unlock Bypass Program [8)]	Add	2	XXX	PA				
	Data		A0H	PD				
Unlock Bypass Block Erase [8)]	Add	2	XXX	BA				
	Data		80H	30H				
Unlock Bypass Chip Erase [8)]	Add	2	XXXH	XXXH				
	Data		80H	10H				
Unlock Bypass Reset	Add	2	XXXH	XXXH				
	Data		90H	00H				
Quadruple word Accelerated Program [9)]	Add	5	XXX	PA1	PA2	PA3	PA4	
	Data		A5H	PD1	PD2	PD3	PD4	
Chip Erase	Add	6	555H	2AAH	555H	555H	2AAH	555H
	Data		AAH	55H	80H	AAH	55H	10H
Block Erase	Add	6	555H	2AAH	555H	555H	2AAH	BA
	Data		AAH	55H	80H	AAH	55H	30H
Erase Suspend [10)]	Add	1	(DA)XXXH					
	Data		B0H					
Erase Resume [11)]	Add	1	(DA)XXXH					
	Data		30H					
Program Suspend [12)]	Add	1	(DA)XXXH					
	Data		B0H					
Program Resume [11)]	Add	1	(DA)XXXH					
	Data		30H					

Table 6 : Command Sequences (Continued)

Command Definitions		Cycle	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
Block Protection/Unprotection [13]	Add	3	XXX	XXX	ABP			
	Data		60H	60H	60H			
CFI Query [14]	Add	1	(DA)X55H					
	Data		98H					
Set Burst Mode Configuration Register [15]	Add	3	555H	2AAH	(CR)555H			
	Data		AAH	55H	C0H			
Set Extended Configuration Register[17]	Add	3	555H	2AAH	(CR)555H			
	Data		AAH	55H	C5H			
Enter OTP Block Region	Addr	3	555H	2AAH	555H			
	Data		AAH	55H	70H			
Exit OTP Block Region	Addr	4	555H	2AAH	555H	XXX		
	Data		AAH	55H	75H	00H		

NOTE :

1) RA : Read Address , PA : Program Address, RD : Read Data, PD : Program Data , BA : Block Address (A20 ~ A12)
DA : Bank Address (A20 ~ A17) , ABP : Address of the block to be protected or unprotected , DI :Die revision ID, CR : Configuration Register Setting
2) The 4th cycle data of autoselect mode and RD are output data. The others are input data.
3) Data bits DQ15–DQ8 are don't care in command sequences, except for RD, PD and Device ID.
4) Unless otherwise noted, address bits A20 ~ A11 are don't cares.
5) The reset command is required to return to read mode.
If a bank entered the autoselect mode during the erase suspend mode, writing the reset command returns that bank to the erase suspend mode.
If a bank entered the autoselect mode during the program suspend mode, writing the reset command returns that bank to the program suspend mode.
If DQ5 goes high during the program or erase operation, writing the reset command returns that bank to read mode or erase suspend mode if that bank was in erase suspend mode.
6) The 3rd and 4th cycle bank address of autoselect mode must be same.
7) Normal Block Protection Verify : 00H for an unprotected block and 01H for a protected block.
OTP Block Protect verify (with OTP Block Address after Entering OTP Block) : 00H for unlocked, and 01H for locked.
For OTP Block Protection Verify, 3rd command cycle is (DA)555H/90H. DA(Bank address) should be invoked instead of BA(Block address).
8) The unlock bypass command sequence is required prior to this command sequence.
9) Quadruple word accelerated program is invoked only at Vpp=V_{ID} ,Vpp setup is required prior to this command sequence.
PA1, PA2, PA3, PA4 have the same A20~A2 address.
10) The system may read and program in non-erasing blocks when in the erase suspend mode.
The system may enter the autoselect mode when in the erase suspend mode.
The erase suspend command is valid only during a block erase operation, and requires the bank address.
11) The erase/program resume command is valid only during the erase/program suspend mode, and requires the bank address.
12) This mode is used only to enable Data Read by suspending the Program operation.
13) Set block address(BA) as either A6 = VIH, A1 = VIH and A0 = VIL for unprotected or A6 = VIL, A1 = VIH and A0 = VIL for protected.
14) Command is valid when the device is in Read mode or Autoselect mode.
15) See "Set Burst Mode Configuration Register" for details.
On the third cycle, the data should be "C0h" and address bits A20-A12 set the code to be latched.
16) 0H for handshaking, 1H for non-handshaking
17) **CR is XXXA12 + 555h In Extended Configuration Register**

9.0 DEVICE OPERATION

The device has I/Os that accept both address and data information. To write a command or command sequence (which includes programming data to the device and erasing blocks of memory), the system must drive CLK, $\overline{AVD}$ and $\overline{CE}$ to V_{IL} and $\overline{OE}$ to V_{IH} when providing an address to the device, and drive CLK, $\overline{WE}$ and $\overline{CE}$ to V_{IL} and $\overline{OE}$ to V_{IH} when writing commands or data.
The device provide the unlock bypass mode to save its program time for program operation. Unlike the standard program command sequence which is comprised of four bus cycles, only two program cycles are required to program a word in the unlock bypass mode. One block, multiple blocks, or the entire device can be erased. Table 3 indicates the address space that each block occupies. The device's address space is divided into sixteen banks: Bank 0 contains the boot/parameter blocks, and the other banks(from Bank 1 to 15) consist of uniform blocks. A "bank address" is the address bits required to uniquely select a bank. Similarly, a "block address" is the address bits required to uniquely select a block. I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

9.1 Read Mode

The device automatically enters to asynchronous read mode after device power-up. No commands are required to retrieve data in asynchronous mode. After completing an Internal Program/Erase Routine, each bank is ready to read array data. The reset command is required to return a bank to the read(or erase-suspend-read)mode if DQ5 goes high during an active program/erase operation, or if the bank is in the autoselect mode.
The synchronous(burst) mode will ***automatically*** start on the last rising edge of the CLK input while $\overline{AVD}$ is held low. That means device enters burst read mode from asynchronous read mode to burst read mode using CLK and $\overline{AVD}$ signal. When the burst read is finished(or terminated), the device return to asynchronous read mode automatically.

9.1.1 Asynchronous Read Mode

For the asynchronous read mode a valid address should be asserted on A/DQ0-A/DQ15 and A16-A20, while driving $\overline{AVD}$ and $\overline{CE}$ to V_{IL}. $\overline{WE}$ should remain at V_{IH}. Note that CLK must remain low for asynchronous read mode. The address is latched at the rising edge of $\overline{AVD}$, and then the system can drive $\overline{OE}$ to V_{IL}. The data will appear on A/DQ0-A/DQ15. Since the memory array is divided into sixteen banks, each bank remains enabled for read access until the command register contents are altered.
Address access time (t_{AA}) is equal to the delay from valid addresses to valid output data. The chip enable access time(t_{CE}) is the delay from the falling edge of $\overline{CE}$ to valid data at the outputs. The output enable access time(t_{OE}) is the delay from the falling edge of $\overline{OE}$ to valid data at the output. The asynchronous access time is measured from a valid address, falling edge of $\overline{AVD}$ or falling edge of $\overline{CE}$ whichever occurs last. To prevent the memory content from spurious altering during power transition, the initial state machine is set for reading array data upon device power-up, or after a hardware reset.

9.1.2 Synchronous (Burst) Read Mode

The device is capable of continuous linear burst operation and linear burst operation of a preset length. For the burst mode, the system should determine how many clock cycles are desired for the initial word(t_{IAA}) of each burst access and what mode of burst operation is desired using "Burst Mode Configuration Register" command sequences. See "Set Burst Mode Configuration" for further details. The status data also can be read during burst read mode by using $\overline{AVD}$ signal with a bank address. To initiate the synchronous read again, a new address and $\overline{AVD}$ pulse is needed after the host has completed status reads or the device has completed the program or erase operation.

Continuous Linear Burst Read
The synchronous(burst) mode will *automatically* start on the rising edge of the CLK input while $\overline{AVD}$ is held low. If several CLKs exist in $\overline{AVD}$ low, the last rising edge is valid CLK. Note that the device is enabled for asynchronous mode when it first powers up. The initial word is output t_{IAA} after the rising edge of the last CLK cycle. Subsequent words are output t_{BA} after the rising edge of each successive clock cycle, which automatically increments the internal address counter. Note that the device has internal address boundary that occurs every 16 words. When the device is crossing the first word boundary, additional clock cycles are needed before data appears for the next address. The number of additional clock cycle can vary from zero to seven cycles, and the exact number of additional clock cycle depends on the starting address of burst read. The RDY output indicates this condition to the system by pulsing low. The device will continue to output sequential burst data, wrapping around to address 000000h after it reaches the highest addressable memory location until the system asserts $\overline{CE}$ high, $\overline{RESET}$ low or $\overline{AVD}$ low in conjunction with a new address.(See Table 5.) The reset command does not terminate the burst read operation. When it accessed the bank is programming or erasing , continuous burst read mode will output status data. And status data will be sustained until the system asserts $\overline{CE}$ high or $\overline{RESET}$ low or $\overline{AVD}$ low in conjunction with a new address. **Note that at least 10ns is needed to start next burst read operation from terminating previous burst read operation in the case of asserting $\overline{CE}$ high.**

8-,16-Word Linear Burst Read
As well as the Continuous Linear Burst Mode, there are two(8 & 16 word) linear wrap, in which a fixed number of words are read from consecutive addresses. In these modes, the addresses for burst read are determined by the group within which the starting address falls. The groups are sized according to the number of words read in a single burst sequence for a given mode.(See Table. 7)

Table 7: Burst Address Groups(Wrap mode only)

Burst Mode	Group Size	Group Address Ranges
8 word	8 words	0-7h, 8-Fh, 10-17h, ...
16 word	16 words	0-Fh, 10-1Fh, 20-2Fh, ...

As an example:
In wrap mode case, if the starting address in the 8-word mode is 2h, the address range to be read would be 0-7h, and the wrap burst sequence would be 2-3-4-5-6-7-0-1h. The burst sequence begins with the starting address written to the device, but wraps back to the first address in the selected group. In a similar manner, 16-word wrap mode begin their burst sequence on the starting address written to the device, and then wrap back to the first address in the selected address group.

9.2 Output Driver Setting

The device supports four kinds of output driver setting for matching the system chracteristics. The users can tune the output driver impedance of the data and RDY outputs by address bits A20-A19. (See Configuration Register Table) The users can set the output driver strength independently for precise system characteristic matching. Table 8 shows which output driver would be tuned and the strength according to A20-A19. Upon power-up or reset, the register will revert to the default setting.

9.3 Programmable Wait State

The programmable wait state feature indicates to the device the number of additional clock cycles that must elapse after $\overline{AVD}$ is driven active for burst read mode. Upon power up, the number of total initial access cycles defaults to eight.

9.4 Handshaking

The handshaking feature allows the host system to simply monitor the RDY signal from the device to determine when the initial word of burst data is ready to be read. To set the number of initial cycle for optimal burst mode, the host should use the programmable wait state configuration.(See "Set Burst Mode Configuration Register" for details.) The rising edge of RDY after $\overline{OE}$ goes low indicates the initial word of valid burst data. Using the autoselect command sequence the handshaking feature may be verified in the device.

9.5 Set Burst Mode Configuration Register

The device uses a configuration register to set the various burst parameters : the number of initial cycles for burst and burst read mode. The burst mode configuration register must be set before the device enters burst mode.
The burst mode configuration register is loaded with a three-cycle command sequences. On the third cycle, the data should be C0h, address bits A11-A0 should be 555h, and address bits A20-A12 set the code to be latched. The device will power up or after a hardware reset with the default setting.

Table 8: Burst Mode Configuration Register Table

Address Bit	Function	Settings(Binary)
A20	Output Driver Control	00 = Driver Multiplier : 1/3 01 = Driver Multiplier : 1/2 10 = Driver Multiplier : 1 (Default) 11 = Driver Multiplier : 1.5
A19		
A18	RDY Active	1 = RDY active one clock cycle before data 0 = RDY active with data(default)
A17	Burst Read Mode	000 = Continuous(default) 001 = 8-word linear with wrap 010 = 16-word linear with wrap 011 ~ 111 = Reserve
A16		
A15		
A14	Programmable Wait State	000 = Data is valid on the 4th active CLK edge after AVD transition to VIH (50/54Mhz) 001 = Data is valid on the 5th active CLK edge after AVD transition to VIH (60/66/70Mhz) 010 = Data is valid on the 6th active CLK edge after AVD transition to VIH (80/83Mhz) 011 = Data is valid on the 7th active CLK edge after AVD transition to VIH (90/100Mhz) 100 = Data is valid on the 8th active CLK edge after AVD transition to VIH (108Mhz,default) 101 = Reserve 110 = Reserve 111 = Reserve
A13		
A12		

NOTE :
Initial wait state should be set according to it's clock frequency. Table 8 recommends the program wait state for each clock frequencies. Not 100% tested

9.5.1 Extended Configuration Register (option : K8S3015ET(B)F, K8S3315ET(B)F only)

The synchronous(burst) mode will start on the last rising edge of the CLK input while $\overline{AVD}$ is held low after Extended Mode Register Setting to A12=1.

Table 9: Extended Configuration Register table

Address Bit	Function	Settings(Binary)
A12	Read Mode	0 = Asynchronous Read Mode(default) 1 = Synchronous Burst Read Mode

9.5.2 Programmable Wait State Configuration

This feature informs the device of the number of clock cycles that must elapse after AVD# is driven active before data will be available. This value is determined by the input frequency of the device. Address bits A14-A12 determine the setting. (See Burst Mode Configuration Register Table)
The Programmable wait state setting instructs the device to set a particular number of clock cycles for the initial access in burst mode. Note that hardware reset will set the wait state to the default setting, that is 8 initial cycles.

9.5.3 Burst Read Mode Setting

The device supports three different burst read modes : continuous linear mode, 8 and 16 word linear burst modes with wrap

9.5.4 RDY Configuration

By default, the RDY pin will be high whenever there is valid data on the output. The device can be set so that RDY goes active one data cycle before active data. Address bit A18 determine this setting. Note that RDY always go high with valid data in case of word boundary crossing.

Table 10: Burst Address Sequences

	Start Addr.	Burst Address Sequence		
		Continuous Burst	8-word Burst	16-word Burst
Wrap	0	0-1-2-3-4-5-6...	0-1-2-3-4-5-6-7	0-1-2-3-4-....-D-E-F
	1	1-2-3-4-5-6-7...	1-2-3-4-5-6-7-0	1-2-3-4-5-....-E-F-0
	2	2-3-4-5-6-7-8...	2-3-4-5-6-7-0-1	2-3-4-5-6-....-F-0-1
	. .	. .	. .	. .

9.6 Autoselect Mode

By writing the autoselect command sequences to the system, the device enters the autoselect mode. This mode can be read only by asynchronous read mode. The system can then read autoselect codes from the internal register(which is separate from the memory array). Standard asynchronous read cycle timings apply in this mode. The device offers the Autoselect mode to identify manufacturer and device type by reading a binary code. In addition, this mode allows the host system to verify the block protection or unprotection. Table 10 shows the address and data requirements. The autoselect command sequence may be written to an address within a bank that is in the read mode, erase-suspend-read mode or program-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the device. The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the address and the autoselect command. Note that the block address is needed for the verification of block protection. The system may read at any address within the same bank any number of times without initiating another autoselect command sequence. And the burst read should be prohibited during Autoselect Mode. To terminate the autoselect operation, write Reset command(F0H) into the command register.

Table 11: Autoselect Mode Description

Description	Address	Read Data
Manufacturer ID	(DA) + 00H	ECH
Device ID	(DA) + 01H	2606H(Top), 2607H(Bottom)
Block Protection/Unprotection	(BA) + 02H	01H (protected), 00H (unprotected)
Handshaking	(DA) + 03H	0H : handshaking, 1H : non-handshaking

9.7 Standby Mode

When the $\overline{CE}$ and $\overline{RESET}$ inputs are both held at $V_{CC} \pm 0.2V$ or the system is not reading or writing, the device enters Stand-by mode to minimize the power consumption. In this mode, the device outputs are placed in the high impedence state, independent of the $\overline{OE}$ input. When the device is in either of these standby modes, the device requires standard access time (tCE) for read access before it is ready to read data. If the device is deselected during erasure or programming, the device draws active current until the operation is completed. I_{CC5} in the DC Characteristics table represents the standby current specification.

9.8 Automatic Sleep Mode

The device features Automatic Sleep Mode to minimize the device power consumption during both asynchronous and burst mode. When addresses remain stable for t_{AA}+60ns, the device automatically enables this mode. The automatic sleep mode is independent of the $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ control signals. In a sleep mode, output data is latched and always available to the system. When addresses are changed, the device provides new data without wait time. Automatic sleep mode current is equal to standby mode current.

9.9 Output Disable Mode

When the $\overline{OE}$ input is at V_{IH} , output from the device is disabled. The outputs are placed in the high impedance state.

9.10 Block Protection & Unprotection

To protect the block from accidental writes, the block protection/unprotection command sequence is used. On power up, all blocks in the device are protected. To unprotect a block, the system must write the block protection/unprotection command sequence. The first two cycles are written: addresses are don't care and data is 60h. Using the third cycle, the block address (ABP) and command (60h) is written, while specifying with addresses A6, A1 and A0 whether that block should be protected (A6 = V_{IL}, A1 = V_{IH}, A0 = V_{IL}) or unprotected (A6 = V_{IH}, A1 = V_{IH}, A0 = V_{IL}). After the third cycle, the system can continue to protect or unprotect additional cycles, or exit the sequence by writing F0h (reset command).

The device offers three types of data protection at the block level:

- The block protection/unprotection command sequence disables or re-enables both program and erase operations in any block.
- When $\overline{WP}$ is at V_{IL}, the two outermost blocks are protected.
- When V_{PP} is at V_{IL}, all blocks are protected.

Note that user never float the Vpp and $\overline{WP}$, that is, Vpp is always connected with V_{IH}, V_{IL} or V_{ID} and $\overline{WP}$ is V_{IH} or V_{IL}.

9.10.1 Enhanced Block Protection (option : K8S3115ET(B)F, K8S3315ET(B)F only)

Table 12: Enhanced Block Protection Schemes

DYB	PPB	PPB Lock	Block State
0	0	0	Unprotected-PPB and DYB are changeable
0	0	1	Unprotected-PPB not changeable and DYB are changeable
0	1	0	Protected-PPB and DYB are changeable
1	0	0	
1	1	0	
0	1	1	Protected-PPB not changeable, DYB is changeable
1	0	1	
1	1	1	

The K8S3215E features several levels of block protection, which can disable both the program and erase operations in certain blocks or block groups:

Persistent Block Protection
A command block protection method that replaces the old 12V controlled protection method.

Password Block Protection
A highly sophisticated protection method that requires a password before changes to certain blocks or block groups are permitted.

Selecting a Block Protection Mode

All parts default to operate in the Persistent Block Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which block protectionmethod will be used. If the Persistent Block Protection method is desired, programming the Persistent Block Protection Mode Locking Bit permanently sets the device to the Persistent Block Protection mode. If the Password Block Protection method is desired, programming the Password Mode Locking Bit permanently sets the device to the Password Block Protection mode.

It is not possible to switch between the two protection modes once a locking bit has been set. One of the two modes must be selected when the device is first programmed. This prevents a program or virus from later setting the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Block Protection Mode into the Password Protection Mode.

The device is shipped with all blocks protected(default). Also all blocks can be unprotected by another option. (DYB can be unprotected at power-up : Please contact the local sales office.)

Persistent Block Protection

The Persistent Block Protection method replaces the 12V controlled protection method in previous flash devices. This new method provides three different block protection states:

Persistently Locked - The block is protected and cannot be changed.
Dynamically Locked - The block is protected and can be changed by a simple command.
Unlocked - The block is unprotected and can be changed by a simple command.

To achieve these states, three types of "bits" are used:

Persistent Protection Bit
Persistent Protection Bit Lock
Persistent Block Protection Mode Locking Bit

Persistent Protection Bit (PPB)

A single Persistent (non-volatile) Protection Bit is assigned to each block. Each PPB is individually modifiable through the PPB Write Command. The device erases all PPBs in parallel. If any PPB requires erasure, the device must be instructed to preprogram all of the block PPBs prior to PPB erasure. Otherwise, a previously erased block PPBs can potentially be over-erased. The flash device does not have a built-in means of preventing block PPBs over-erasure.

PPB program/erase can be checked by DQ6 toggle bit. When device is in busy state, DQ6 will toggle. Toggling DQ6 will stop after the device completes its Internal Routine.

Persistent Protection Bit Lock (PPB Lock)

The Persistent Protection Bit Lock (PPB Lock) is a global volatile bit. When set to "1", the PPBs cannot be changed. When cleared "0", the PPBs are changeable. There is only one PPB Lock bit per device. The PPB Lock is cleared after power-up or hardware reset. There is no command sequence to unlock the PPB Lock.

Dynamic Protection Bit (DYB)

A volatile protection bit is assigned for each block. After power-up, the contents of all DYBs is "1". Each DYB is individually modifiable through the DYB Write Command.

When the parts are first shipped, the PPBs are cleared, the DYBs is set("1"), and PPB Lock is defaulted to power up in the cleared state - meaning the PPBs are changeable. When the device is first powered on the DYBs power up set (blocks protected). The Protection State for each sector is determined by the logical OR of the PPB and the DYB related to that block. For the blocks that have the PPBs cleared, the DYBs control whether or not the block is protected or unprotected.

By issuing the DYB Write command sequences, the DYBs will be set or cleared, thus placing each block in the protected or unprotected state. These are the so-called Dynamic Locked or Unlocked states. They are called dynamic states because it is very easy to switch back and forth between the protected and unprotected conditions. This allows software to easily protect blocks against inadvertent changes yet does not prevent the easy removal of protection when changes are needed. The DYBs maybe set or cleared as often as needed.

The PPBs allow for a more static, and difficult to change, level of protection. The PPBs retain their state across power cycles because they are non-volatile. Individual PPBs are set with a command but must all be cleared as a group through a complex sequence of program and erasing commands. The PPBs are also limited to 100 erase cycles.

The PPB Lock bit adds an additional level of protection. Once all PPBs are programmed to the desired settings, the PPB Lock may be set to "1". Setting the PPB Lock disables all program and erase commands to the non-volatile PPBs. In effect, the PPB Lock Bit locks the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle. System boot code can determine if any changes to the PPB are needed; for example, to allow new system code to be downloaded. If no changes are needed then the boot code can set the PPB Lock to disable any further changes to the PPBs during system operation.

The WP#/ACC write protect pin adds a final level of hardware protection to blocks BA0 and BA1. (When $\overline{WP}$ is at V_{IL}, the two outermost blocks are protected) When this pin is low it is not possible to change the contents of these blocks. These blocks generally hold system boot code. The WP#/ACC pin can prevent any changes to the boot code that could override the choices made while setting up block protection during system initialization.

For customers who are concerned about malicious viruses there is another level of security - the persistently locked state. To persistently pro-

tect a given block or block group, the PPBs associated with that block need to be set to "1". Once all PPBs are programmed to the desired settings, the PPB Lock should be set to "1". Setting the PPB Lock automatically disables all program and erase commands to the Non-Volatile PPBs. In effect, the PPB Lock "freezes" the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle.

It is possible to have blocks that have been persistently locked, and blocks that are left in the dynamic state. The blocks in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DYB Write command sequence is all that is necessary. The DYB write command for the dynamic blocks switch the DYBs to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked blocks, a few more steps are required. First, the PPB Lock bit must be disabled by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB lock bit once again will lock the PPBs, and the device operates normally again.

The best protection is achieved by executing the PPB lock bit set command early in the boot code, and protect the boot code by holding WP#/ ACC = VIL.

Table 12 contains all possible combinations of the DYB, PPB, and PPB lock relating to the status of the block.

In summary, if the PPB is set, and the PPB lock is set, the block is protected and the protection can not be removed until the next power cycle clears the PPB lock. If the PPB is cleared, the block can be dynamically locked or unlocked. The DYB then controls whether or not the block is protected or unprotected.

If the user attempts to program or erase a protected block, the device ignores the command and returns to read mode. A program command to a protected block enables status polling for approximately 1us before the device returns to read mode without having modified the contents of the protected block. An erase command to a protected block enables status polling for approximately 100us after which the device returns to read mode without having erased the protected block.

The programming of the DYB, PPB, and PPB lock for a given block can be verified by writing a DYB/PPB/PPB lock verify command to the device.

Persistent Block Protection Mode Locking Bit
Like the password mode locking bit, a Persistent Block Protection mode locking bit exists to guarantee that the device remain in software block protection. Once set, the Persistent Block Protection locking bit prevents programming of the password protection mode locking bit. This guarantees that a hacker could not place the device in password protection mode.

Password Protection Mode

The Password Block Protection Mode method allows an even higher level of security than the Persistent Block Protection Mode. There are two main differences between the Persistent Block Protection and the Password Block Protection Mode:

When the device is first powered on, or comes out of a reset cycle, the PPB Lock bit set to the locked state, rather than cleared to the unlocked state.
The only means to clear the PPB Lock bit is by writing a unique 64-bit Password to the device.
The Password Block Protection method is otherwise identical to the Persistent Block Protection method.
A 64-bit password is the only additional tool utilized in this method.
Once the Password Mode Locking Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear the PPB Lock bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB Lock bit is cleared, and the PPBs can be altered. If they do not match, the flash device does nothing. There is a built-in 2us delay for each "password check." This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

Password and Password Mode Locking Bit
In order to select the Password block protection scheme, the customer must first program the password. The password may be correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Verify operations.

Once the desired password is programmed in, the customer must then set the Password Mode Locking Bit. This operation achieves two objectives:
Permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.
Disables all further commands to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Protection method is desired when setting the Password Mode Locking Bit. More importantly, the user must be sure that the password is correct when the Password Mode Locking Bit is set. Due to the fact that read operations are disabled, there is no means to verify what the password is afterwards. If the password is lost after setting the Password Mode Locking Bit, there will be no way to clear the PPB Lock bit.

The Password Mode Locking Bit, once set, prevents reading the 64-bit password on the DQ bus and further password programming. The

Password Mode Locking Bit is not erasable. Once Password Mode Locking Bit is programmed, the Persistent Block Protection Locking Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

64-bit Password

The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Verify commands (see "Password Verify Command"). The password function works in conjunction with the Password Mode Locking Bit, which when set, prevents the Password Verify command from reading the contents of the password on the pins of the device.

Write Protect (WP#)

If the system asserts VIL on the WP#/ACC pin, the device disables program and erase functions in the two outermost 4 Kword blocks on the flash array independent of whether it was previously protected or unprotected.
If the system asserts VIH on the WP#/ACC pin, the device reverts the two blocks to whether they were last set to be protected or unprotected.

Persistent Protection Bit Lock

The Persistent Protection Bit (PPB) Lock is a volatile bit that reflects the state of the Password Mode Locking Bit after power-up reset. If the Password Mode Lock Bit is also set after a hardware reset (RESET# asserted) or a power-up reset, the ONLY means for clearing the PPB Lock Bit in Password Protection Mode is to issue the Password Unlock command. Successful execution of the Password Unlock command clears the PPB Lock Bit, allowing for block PPBs modifications. Asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit to a "1" when the Password Mode Lock Bit is not set.

If the Password Mode Locking Bit is not set, including Persistent Protection Mode, the PPB Lock Bit is cleared after power-up or hardware reset. The PPB Lock Bit is set by issuing the PPB Lock Bit Set command. Once set the only means for clearing the PPB Lock Bit is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Protection Mode.

Master locking bit set

This Master locking bit can ensure that protected blocks be permanently unalterable.
Master locking bit is non-volatile bit. Master locking bit controls protection status of the protected blocks.
The usage of the master locking bit command sequence is absolutely required to ensure full protection of data from future alterations. If master locking bit is set ("1"), the protected blocks are permanently protected. They are not changed and altered by any future lock/unlock commands.
Anyone who uses this fuction needs much attention. Because there is no way to return to unlock status. Default status of master locking bit is unlock status("0").
If Master locking bit sets on unprotected block, the block still are remaining in status of unprotected block.
The unprotected block can be protected by protection command.

Table 13: Block Protection Command Sequences

Command Sequence		Cycle	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle	7th Cycle
Password Program(1,2)	Addr	4	555H	2AAH	555H	XX[0-3]H			
	Data		AAH	55H	38H	PD[0-3]			
Password Verify(2,4,5)	Addr	4	555H	2AAH	555H	PWA[0-3]			
	Data		AAH	55H	C8H	PWD[0-3]			
Password Unlock(3,6,7)	Addr	7	555H	2AAH	555H	PWA[0]	PWA[1]	PWA[2]	PWA[3]
	Data		AAH	55H	28H	PWD[0]	PWD[1]	PWD[2]	PWD[3]
PPB Program(1,2,8)	Addr	6	555H	2AAH	555H	(BA)WP	(BA)WP	(BA)WP	
	Data		AAH	55H	60H	68H	48H	RD(0)	
Master locking bit Set	Addr	3	555H	2AAH	555H				
	Data		AAH	55H	F1H				
PPB Status	Addr	4	555H	2AAH	555H	(BA)WP			
	Data		AAH	55H	90H	RD(0)			
All PPB Erase(1,2,9,10)	Addr	6	555H	2AAH	555H	WP	(BA)	(BA)WP	
	Data		AAH	55H	60H	60H	40H	RD(0)	
PPB Lock Bit Set	Addr	3	555H	2AAH	555H				
	Data		AAH	55H	78H				
PPB Lock Bit Status(11)	Addr	4	555H	2AAH	555H	BA			
	Data		AAH	55H	58H	RD(1)			

DYB Write(3)	Addr	4	555H	2AAH	555H	BA			
	Data		AAH	55H	48H	X1H			
DYB Erase(3)	Addr	4	555H	2AAH	555H	BA			
	Data		AAH	55H	48H	X0H			
DYB Status(2)	Addr	4	555H	2AAH	(DA)555H	BA			
	Data		AAH	55H	58H	RD(0)			
PPMLB Program(1,2,8)	Addr	6	555H	2AAH	555H	PL	PL	PL	
	Data		AAH	55H	60H	68H	48H	RD(0)	
PPMLB Status(1)	Addr	5	555H	2AAH	555H	PL	PL		
	Data		AAH	55H	60H	48H	RD(0)		
SPMLB Program(1,2,8)	Addr	6	555H	2AAH	555H	BL	BL	BL	
	Data		AAH	55H	60H	68	48	RD(0)	
SPMLB Status(1)	Addr	5	555H	2AAH	555H	BL	BL		
	Data		AAH	55H	60H	48	RD(0)		
OTP Protection bit Program(1,2)	Addr	6	555H	2AAH	555H	OW	OW	OW	
	Data		AAH	55H	60H	68H	48H	RD(0)	
OTP Protection bit Status	Addr	5	555H	2AAH	555H	OW	OW		
	Data		AAH	55H	60H	48H	RD(0)		

DYB = Dynamic Protection Bit
OW = Address (A7:A0) is (00011010)
PD[3:0] = Password Data (1 of 4 portions)
PPB = Persistent Protection Bit
PWA = Password Address. A1:A0 selects portion of password.
PWD = Password Data being verified.
PL = Password Protection Mode Lock Address (A7:A0) is (00001010)
RD(0) = Read Data DQ0 for protection indicator bit.
RD(1) = Read Data DQ1 for PPB Lock status.
BA = Block Address where security command applies. Address bits Amax:A12 uniquely select any block.
BL = Persistent Protection Mode Lock Address (A7:A0) is (00010010)
WP = PPB Address (A7:A0) is (00000010)
X = Don't care
PPMLB = Password Protection Mode Locking Bit
SPMLB = Persistent Protection Mode Locking Bit

Notes:
- See the description of bus operations.
- All values are in hexadecimal.
- Shaded cells in table denote read cycles. All other cycles are write operations.
- During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.

To return to read mode in 'password verify', 'password unlock', 'DYB status', 'PPB lock bit status', 'PPB lock bit set' mode Exit OTP Block Region command is needed.

1. The reset command returns device to reading array.
2. Cycle 4 programs the addressed locking bit. Cycles 5 and 6 validate bit has been fully programmed when DQ0 = 1. If DQ0 = 0 in cycle 6, program command must be issued and verified again.
3. Data is latched on the rising edge of WE#.
4. Entire command sequence must be entered for each portion of password.
5. Command sequence returns FFh if PPMLB is set.
6. The password is written over four consecutive cycles, at addresses 0-3.
7. A 2us timeout is required between any two portions of password.
8. A 100us timeout is required between cycles 4 and 5.
9. A 1.2 ms timeout is required between cycles 4 and 5.
10. Cycle 4 erases all PPBs. Cycles 5 and 6 validate bits have been fully erased when DQ0 = 0. If DQ0 = 1 in cycle 6, erase command must be issued and verified again. Before issuing erase command, all PPBs should be programmed to prevent PPB overerasure.
11. DQ1 = 1 if PPB locked, 0 if unlocked.

9.11 Hardware Reset

The device features a hardware method of resetting the device by the $\overline{\text{RESET}}$ input. When the $\overline{\text{RESET}}$ pin is held low(V_{IL}) for at least a period of tRP, the device immediately terminates any operation in progress, tristates all outputs, and ignores all read/write commands for the duration of the $\overline{\text{RESET}}$ pulse. The device also resets the internal state machine to asynchronous read mode. To ensure data integrity, the interrupted operation should be reinitiated once the device is ready to accept another command sequence. As previously noted, when $\overline{\text{RESET}}$ is held at $V_{SS} \pm 0.2V$, the device enters standby mode. The $\overline{\text{RESET}}$ pin may be tied to the system reset pin. If a system reset occurs during the Internal Program or Erase Routine, the device will be automatically reset to the asynchronous read mode; this will enable the systems microprocessor to read the boot-up firmware from the Flash memory. If $\overline{\text{RESET}}$ is asserted during a program or erase operation, the device requires a time of tREADY (during Internal Routines) before the device is ready to read data again. If $\overline{\text{RESET}}$ is asserted when a program or erase operation is not executing, the reset operation is completed within a time of tREADY (not during Internal Routines). tRH is needed to read data after $\overline{\text{RESET}}$ returns to V_{IH}. Refer to the AC Characteristics tables for $\overline{\text{RESET}}$ parameters and to Figure 12 for the timing diagram.

9.12 Software Reset

The reset command provides that the bank is reseted to read mode, erase-suspend-read mode or program-suspend-read mode. The addresses are in Don't Care state. The reset command may be written between the sequence cycles in an erase command sequence before erasing begins, or in an program command sequence before programming begins. If the device begins erasure or programming, the reset command is ignored until the operation is completed. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. The reset command valid between the sequence cycles in an autoselect command sequence. In an autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Also, if a bank entered the autoselect mode while in the Program Suspend mode, writing the reset command returns that bank to the program-suspend-read mode. If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode. (or erase-suspend-read mode if the bank was in Erase Suspend)

9.13 Program

The K8S3215E can be programmed in units of a word. Programming is writing 0's into the memory array by executing the Internal Program Routine. In order to perform the Internal Program Routine, a four-cycle command sequence is necessary. The first two cycles are unlock cycles. The third cycle is assigned for the program setup command. In the last cycle, the address of the memory location and the data to be programmed at that location are written. The device automatically generates adequate program pulses and verifies the programmed cell margin by the Internal Program Routine. During the execution of the Routine, the system is not required to provide further controls or timings. During the Internal Program Routine, commands written to the device will be ignored.
Note that a hardware reset during a program operation will cause data corruption at the corresponding location.

9.14 Accelerated Program Operation

The device provides Single/Quadruple word accelerated program operations through the Vpp input. Using this mode, faster manufacturing throughput at the factory is possible. When V_{ID} is asserted on the Vpp input, the device automatically enters the Unlock Bypass mode, temporarily unprotects any protected blocks, and uses the higher voltage on the input to reduce the time required for program operations. By removing V_{ID} returns the device to normal operation mode.
Note that Read while Accelerated Programm and Program suspend mode are not guaranteed

Single word accelerated program operation

The system would use two-cycle program sequence (One-cycle (XXX - A0H) is for single word program command, and Next one-cycle (PA - PD) is for program address and data).

Quadruple word accelerated program operation

As well as Single word accelerated program, the system would use five-cycle program sequence (One-cycle (XXX - A5H) is for quadruple word program command, and four cycles are for program address and data).

- Only four words programming is possible
- Each program address must have the same A20~A2 address
- The device automatically generates adequate program pulses and ignores other command after program command
- Program/Erase cycling must be limited below 100cycles for optimum performance.
- Read while Write mode is not guaranteed

Requirements : Ambient temperature : T_A=30°C±10°C

9.15 Unlock Bypass

The K8S3215E provides the unlock bypass mode to save its operation time. This mode is possible for program, block erase and chip erase operation. There are two methods to enter the unlock bypass mode. The mode is invoked by the unlock bypass command sequence or the assertion of V_{ID} on V_{PP} pin. Unlike the standard program/erase command sequence that contains four bus cycles, the unlock bypass program/erase command sequence comprises only two bus cycles. The unlock bypass mode is engaged by issuing the unlock bypass command sequence which is comprised of three bus cycles. Writing first two unlock cycles is followed by a third cycle containing the unlock bypass command (20H). Once the device is in the unlock bypass mode, the unlock bypass program/erase command sequence is necessary. The unlock bypass program command sequence is comprised of only two bus cycles; writing the unlock bypass program command (A0H) is followed by the program address and data. This command sequence is the only valid one for programming the device in the unlock bypass mode. Also, The unlock bypass erase command sequence is comprised of two bus cycles; writing the unlock bypass block erase command(80H-30H) or writing the unlock bypass chip erase command(80H-10H). This command sequences are the only valid ones for erasing the device in the unlock bypass mode. The unlock bypass reset command sequence is the only valid command sequence to exit the unlock bypass mode. The unlock bypass reset command sequence consists of two bus cycles. The first cycle must contain the data (90H). The second cycle contains only the data (00H). Then, the device returns to the read mode.

To enter the unlock bypass mode in hardware level, the V_{ID} also can be used. By assertion V_{ID} on the V_{PP} pin, the device enters the unlock bypass mode. Also, the all blocks are temporarily unprotected when the device using the V_{ID} for unlock bypass mode. To exit the unlock bypass mode, just remove the asserted V_{ID} from the V_{PP} pin.(Note that user never float the Vpp, that is, Vpp is always connected with V_{IH}, V_{IL} or V_{ID}.).

9.16 Chip Erase

To erase a chip is to write 1′s into the entire memory array by executing the Internal Erase Routine. The Chip Erase requires six bus cycles to write the command sequence. The erase set-up command is written after first two "unlock" cycles. Then, there are two more write cycles prior to writing the chip erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory for an all zero data pattern prior to erasing. The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when DQ7 is "1". After that the device returns to the read mode.

9.17 Block Erase

To erase a block is to write 1′s into the desired memory block by executing the Internal Erase Routine. The Block Erase requires six bus cycles to write the command sequence shown in Table 6. After the first two "unlock" cycles, the erase setup command (80H) is written at the third cycle. Then there are two more "unlock" cycles followed by the Block Erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory prior to erasing it. The block address is latched on the rising edge of $\overline{AVD}$, while the Block Erase command is latched on the rising edge of $\overline{WE}$. Multiple blocks can be erased sequentially by writing the sixth bus-cycle. Upon completion of the last cycle for the Block Erase, additional block address and the Block Erase command (30H) can be written to perform the Multi-Block Erase. For the Multi-Block Erase, only sixth cycle(block address and 30H) is needed.(Similarly, only second cycle is needed in unlock bypass block erase.) An 50us (typical) "time window" is required between the Block Erase command writes. The Block Erase command must be written within the 50us "time window", otherwise the Block Erase command will be ignored. The 50us "time window" is reset when the falling edge of the $\overline{WE}$ occurs within the 50us of "time window" to latch the Block Erase command. During the 50us of "time window", any command other than the Block Erase or the Erase Suspend command written to the device will reset the device to read mode. After the 50 us of "time window", the Block Erase command will initiate the Internal Erase Routine to erase the selected blocks. Any Block Erase address and command following the exceeded "time window" may or may not be accepted. No other commands will be recognized except the Erase Suspend command during Block Erase operation.

The device provides accelerated erase operations through the Vpp input. When V_{ID} is asserted on the Vpp input, the device automatically enters the Unlock Bypass mode, temporarily unprotects any protected blocks, and uses the higher voltage on the input to reduce the time required for erase. By removing V_{ID} returns the device to normal operation mode

9.18 Erase Suspend / Resume

The Erase Suspend command interrupts the Block Erase to read or program data in a block that is not being erased. Also, it is possible to protect or unprotect of the block that is not being erased in erase suspend mode. The Erase Suspend command is only valid during the Block Erase operation including the time window of 50us. The Erase Suspend command is not valid while the Chip Erase or the Internal Program Routine sequence is running. When the Erase Suspend command is written during a Block Erase operation, the device requires a maximum of 20us(recovery time) to suspend the erase operation. Therefore system must wait for 20us(recovery time) to read the data from the bank which include the block being erased. Otherwise, system can read the data immediately from a bank which don't include the block being erased without recovery time(max. 20us) after Erase Suspend command. And, after the maximum 20us recovery time, the device is availble for programming data in a block that is not being erased. But, when the Erase Suspend command is written during the block erase time window (50us), the device immediately terminates the block erase time window and suspends the erase operation. The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. When the Erase Resume command is executed, the Block Erase operation will resume. When the Erase Suspend or Erase Resume command is executed, the addresses are in Don't Care state. In erase suspend followed by resume operation, min. 200ns is needed for checking the busy status.

In the program suspend mode, protect/unprotect command is prohibited.

While erase can be suspended and resumed multiple times, a minimum 30us is required from resume to the next suspend.

9.19 Program Suspend / Resume

The device provides the Program Suspend/Resume mode. This mode is used to enable Data Read by suspending the Program operation. The device accepts a Program Suspend command in Program mode(including Program operations performed during Erase Suspend) but other commands are ignored. After input of the Program Suspend command, 2us is needed to enter the Program Suspend Read mode. Therefore system must wait for 2us(recovery time) to read the data from the bank which include the block being programmed. Othwewise, system can read the data immediately from a bank which don't include block being programmed without recovery time(max. 2us) after Program Suspend command. Like an Erase Suspend mode, the device can be returned to Program mode by using a Program Resume command. In program suspend followed by resume operation, min. 200ns is needed for checking the busy status.

While program operation can be suspended and resumed multiple times, a minimum 30us is required from resume to the next suspend.

9.20 Read While Write Operation

The device is capable of reading data from one bank while writing in the other banks. This is so called the Read While Write operation. An erase operation may also be suspended to read from or program to another location within the same bank(except the block being erased). The Read While Write operation is prohibited during the chip erase operation. Figure 19 shows how read and write cycles may be initiated for simultaneous operation with zero latency. Refer to the DC Characteristics table for read-while-write current specifications.

9.21 OTP Block Region

The OTP Block feature provides a 256-word Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The OTP Block is customer lockable and shipped with itself unlocked, allowing customers to untilize the that block in any manner they choose. The customer-lockable OTP Block has the Protection Verify Bit (DQ0) set to a "0" for Unlocked state or a "1" for Locked state. The system accesses the OTP Block through a command sequence (see "Enter OTP Block / Exit OTP Block Command sequence" at Table 6). After the system has written the "Enter OTP Block" Command sequence, it may read the OTP Block by using the address (1FFF00h~1FFFFFh, in top boot device), (000000h~0000FFh, in bottom boot device) normally and may check the Protection Verify Bit (DQ0) by using the "Autoselect Block Protection Verify" Command sequence with OTP Block address. This mode of operation continues until the system issues the "Exit OTP Block" Command suquence, a hardware reset or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to main blocks. Note that the Accelerated function and unlock bypass modes are not available when the OTP Block is enabled.

Customer Lockable

In a Customer lockable device, The OTP Block is one-time programmable and can be locked only once. Note that the Accelerated programming and Unlock bypass functions are not available when programming the OTP Block. Locking operation to the OTP Block is started by writing the "Enter OTP Block" Command sequence, and then the "Block Protection" Command sqeunce (Table 6) with an OTP Block address. Hardware reset terminates Locking operation, and then makes exiting from OTP Block. The Locking operation has to be above 100us. (After 3rd cycle of protection command invoked, at least 100us wait time is required.) "Exit OTP Block" command sequence and Hardware reset makes locking operation finished and then exiting from OTP Block after 30us.

The OTP Block Lock operation must be used with caution since, once locked, there is no procedure available for unlocking and none of the bits in the OTP Block space can be modified in any way.

Suspend and resume operation are not supported during OTP protect, nor is OTP protect supported during any suspend operations.

Write Pulse “Glitch” Protection

Noise pulses of less than 5ns (typical) on $\overline{OE}$, $\overline{CE}$, $\overline{AVD}$ or $\overline{WE}$ do not initiate a write cycle.

9.22 Low Vcc Write Inhibit

To avoid initiation of a write cycle during Vcc power-up and power-down, a write cycle is locked out for Vcc less than V_{LKO}. If the Vcc < V_{LKO} (Lock-Out Voltage), the command register and all internal program/erase circuits are disabled. Under this condition the device will reset itself to the read mode.Subsequent writes will be ignored until the Vcc level is greater than V_{LKO}. It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional writes when Vcc is above V_{LKO}.

9.23 Logical Inhibit

Write cycles are inhibited by holding any one of $\overline{OE}$ = V_{IL} , $\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IH}. To initiate a write cycle, $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-up Protection

To avoid initiation of a write cycle during V_{CC} power-up, $\overline{RESET}$ low must be asserted during Power-up. After $\overline{RESET}$ goes high. the device is reset to the read mode.

10.0 FLASH MEMORY STATUS FLAGS

The K8S3215E has means to indicate its status of operation in the bank where a program or erase operation is in processes. Address must include bank address being executed internal routine operation. The status is indicated by raising the device status flag via corresponding DQ pins. The status data can be read during burst read mode by using $\overline{AVD}$ signal with a bank address. That means status read is supported in synchronous mode. If status read is performed, the data provided in the burst read is identical to the data in the initial access. To initiate the synchronous read again, a new address and $\overline{AVD}$ pulse is needed after the host has completed status reads or the device has completed the program or erase operation. The corresponding DQ pins are DQ7, DQ6, DQ5, DQ3 and DQ2.

Table 14: Hardware Sequence Flags

	Status		DQ7	DQ6	DQ5	DQ3	DQ2
In Progress	Programming		$\overline{DQ7}$	Toggle	0	0	1
	Block Erase or Chip Erase		0	Toggle	0	1	Toggle
	Erase Suspend Read	Erase Suspended Block	1	1	0	0	Toggle[1)]
	Erase Suspend Read	Non-Erase Suspended Block	Data	Data	Data	Data	Data
	Erase Suspend Program	Non-Erase Suspended Block	$\overline{DQ7}$	Toggle	0	0	1
	Program Suspend Read	Program Suspended Block	DQ7	1	0	0	Toggle[1)]
	Program Suspend Read	Non- program Suspended Block	Data	Data	Data	Data	Data
Exceeded Time Limits	Programming		$\overline{DQ7}$	Toggle	1	0	No Toggle
	Block Erase or Chip Erase		0	Toggle	1	1	(Note 2)
	Erase Suspend Program		$\overline{DQ7}$	Toggle	1	0	No Toggle

NOTE :
1) DQ2 will toggle when the device performs successive read operations from the erase/program suspended block.
2) If DQ5 is High (exceeded timing limits), successive reads from a problem block will cause DQ2 to toggle.

DQ7 : $\overline{\text{Data}}$ Polling

When an attempt to read the device is made while executing the Internal Program, the complement of the data is written to DQ7 as an indication of the Routine in progress. When the Routine is completed an attempt to access to the device will produce the true data written to DQ7. When a user attempts to read the block being erased or bank contains the block, DQ7 will be low. If the device is placed in the Erase/Program Suspend Mode, the status can be detected via the DQ7 pin. If the system tries to read an address which belongs to a block that is being erase suspended, DQ7 will be high. And, if the system tries to read an address which belongs to a block that is being program suspended, the output will be the true data of DQ7 itself. If a non-erase-suspended or non-program-suspended block address is read, the device will produce the true data to DQ7. If an attempt is made to program a protected block, DQ7 outputs complements the data for approximately 1μs and the device then returns to the Read Mode without changing data in the block. If an attempt is made to erase a protected block, DQ7 outputs complement data in approximately 100us and the device then returns to the Read Mode without erasing the data in the block.

DQ6 : Toggle Bit

Toggle bit is another option to detect whether an Internal Routine is in progress or completed. Once the device is at a busy state, DQ6 will toggle. Toggling DQ6 will stop after the device completes its Internal Routine. If the device is in the Erase/Program Suspend Mode, an attempt to read an address that belongs to a block that is being erased or programmed will produce a high output of DQ6. If an address belongs to a block that is not being erased or programmed, toggling is halted and valid data is produced at DQ6. If an attempt is made to program a protected block, DQ6 toggles for approximately 1us and the device then returns to the Read Mode without changing the data in the block. If an attempt is made to erase a protected block, DQ6 toggles for approximately 100μs and the device then returns to the Read Mode without erasing the data in the block. #OE or #CE should be toggled in each toggle bit status read.

DQ5 : Exceed Timing Limits

If the Internal Program/Erase Routine extends beyond the timing limits, DQ5 will go High, indicating program/erase failure.

DQ3 : Block Erase Timer

The status of the multi-block erase operation can be detected via the DQ3 pin. DQ3 will go High if 50μs of the block erase time window expires. In this case, the Internal Erase Routine will initiate the erase operation.Therefore, the device will not accept further write commands until the erase operation is completed. DQ3 is Low if the block erase time window is not expired. Within the block erase time window, an additional block erase command (30H) can be accepted. To confirm that the block erase command has been accepted, the software may check the status of DQ3 following each block erase command.

DQ2 : Toggle Bit 2

The device generates a toggling pulse in DQ2 only if an Internal Erase Routine or an Erase/Program Suspend is in progress. When the device executes the Internal Erase Routine, DQ2 toggles if the bank including an erasing block is read. Although the Internal Erase Routine is in the Exceeded Time Limits, DQ2 toggles if an erasing block in the Exceeded Time Limits is read. When the device is in the Erase/Program Suspend mode, DQ2 toggles only if an address in the erasing or programming block is read. If a non-erasing or non-programmed block address is read during the Erase/Program Suspend mode, then DQ2 will produce valid data. DQ2 will go High if the user tries to program a non-erase suspend block while the device is in the Erase Suspend mode. #OE or #CE should be toggled in each toggle bit status read.

RDY: Ready

Normally the RDY signal is used to indicate if new burst data is available at the rising edge of the clock cycle or not. If RDY is low state, data is not valid at expected time, and if high state, data is valid. Note that, if $\overline{CE}$ is low and $\overline{OE}$ is high, the RDY is high state.

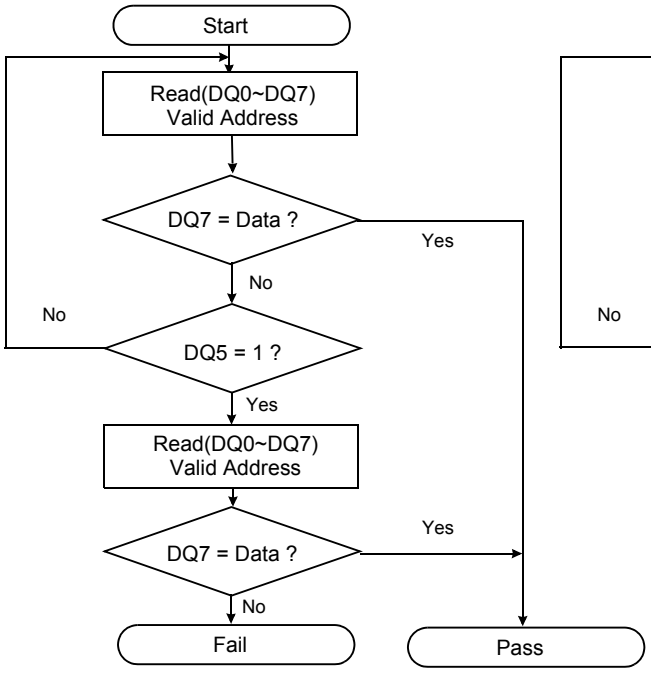


Figure 1: Data Polling Algorithms

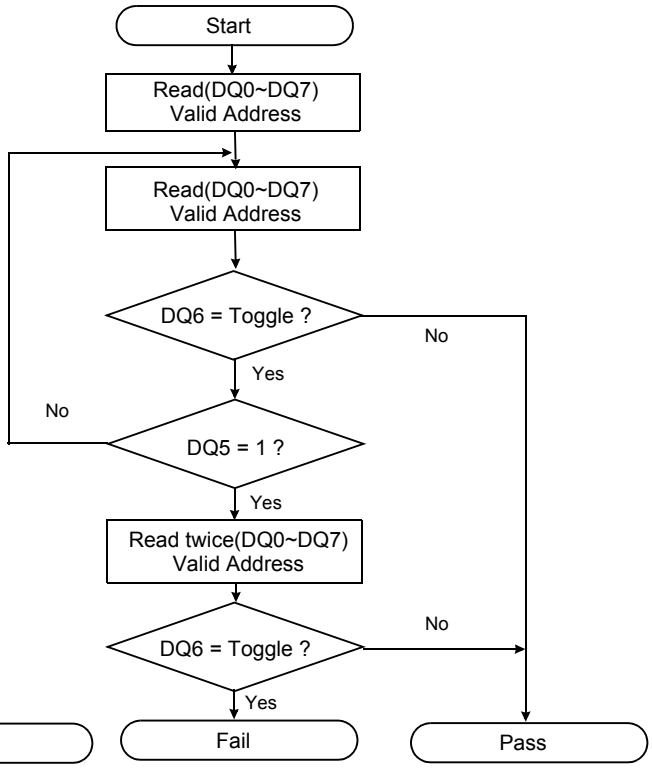


Figure 2: Toggle Bit Alogrithms

11.0 Commom Flash Memory Interface

Common Flash Momory Interface is contrived to increase the compatibility of host system software. It provides the specific information of the device, such as memory size and electrical features. Once this information has been obtained, the system software will know which command sets to use to enable flash writes, block erases, and control the flash component.
When the system writes the CFI command(98H) to address 55H , the device enters the CFI mode. And then if the system writes the address shown in Table 12, the system can read the CFI data. Query data are always presented on the lowest-order data outputs(DQ0-7) only. In word(x16) mode, the upper data outputs(DQ8-15) is 00h. To terminate this operation, the system must write the reset command.

Table 15: Common Flash Memory Interface Code

Description	Addresses (Word Mode)	Data
Query Unique ASCII string "QRY"	10H 11H 12H	0051H 0052H 0059H
Primary OEM Command Set	13H 14H	0002H 0000H
Address for Primary Extended Table	15H 16H	0040H 0000H
Alternate OEM Command Set (00h = none exists)	17H 18H	0000H 0000H
Address for Alternate OEM Extended Table (00h = none exists)	19H 1AH	0000H 0000H
Vcc Min. (write/erase) D7-D4: volt, D3-D0: 100 millivolt	1BH	0017H
Vcc Max. (write/erase) D7-D4: volt, D3-D0: 100 millivolt	1CH	0019H
Vpp(Acceleration Program) Supply Minimum 00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV	1DH	0085H
Vpp(Acceleration Program) Supply Maximum 00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV	1EH	0095H
Typical timeout per single word write 2^N us	1FH	0004H
Typical timeout for Min. size buffer write 2^N us(00H = not supported)	20H	0000H
Typical timeout per individual block erase 2^N ms	21H	000AH
Typical timeout for full chip erase 2^N ms(00H = not supported)	22H	0010H
Max. timeout for word write 2^N times typical	23H	0005H
Max. timeout for buffer write 2^N times typical	24H	0000H
Max. timeout per individual block erase 2^N times typical	25H	0004H
Max. timeout for full chip erase 2^N times typical(00H = not supported)	26H	0000H
Device Size = 2^N byte	27H	0016H
Flash Device Interface description	28H 29H	0000H 0000H
Max. number of byte in multi-byte write = 2^N	2AH 2BH	0000H 0000H
Number of Erase Block Regions within device	2CH	0002H

Table 12 : Common Flash Memory Interface Code (Continued)

Description	Addresses (Word Mode)	Data
Erase Block Region 1 Information Bits 0~15: y+1=block number Bits 16~31: block size= z x 256bytes	2DH 2EH 2FH 30H	0007H 0000H 0020H 0000H
Erase Block Region 2 Information	31H 32H 33H 34H	003EH 0000H 0000H 0001H
Erase Block Region 3 Information	35H 36H 37H 38H	0000H 0000H 0000H 0000H
Erase Block Region 4 Information	39H 3AH 3BH 3CH	0000H 0000H 0000H 0000H
Query-unique ASCII string "PRI"	40H 41H 42H	0050H 0052H 0049H
Major version number, ASCII	43H	0036H
Minor version number, ASCII	44H	0030H
Address Sensitive Unlock(Bits 1-0) 0 = Required, 1= Not Required Silcon Revision Number(Bits 7-2)	45H	0000H
Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write	46H	0002H
Block Protect 00 = Not Supported, 01 = Supported	47H	0001H
Block Temporary Unprotect 00 = Not Supported, 01 = Supported	48H	0000H
Block Protect/Unprotect scheme 00 = Not Supported, 01 = Supported	49H	0001H
Simultaneous Operation 00 = Not Supported, 01 = Supported	4AH	0001H
Burst Mode Type 00 = Not Supported, 01 = Supported	4BH	0001H
Page Mode Type 00 = Not Supported, 01 = 4 Word Page 02 = 8 Word Page	4CH	0000H
Top/Bottom Boot Block Flag 02H = Bottom Boot Device, 03H = Top Boot Device	4DH	0003H
Max. Operating Clock Frequency (MHz)	4EH	006CH
RWW(Read While Write) Functionality Restriction (00H = non exists , 01H = exists)	4FH	0000H
Handshaking 00 = Not Supported at both mode, 01 = Supported at Sync. Mode 10 = Supported at Async. Mode, 11 = Supported at both Mode	50H	0001H

12.0 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{CC}	V_{CC}	-0.5 to +2.5	V
	V_{PP}	V_{IN}	-0.5 to +9.5	
	All Other Pins		-0.5 to +2.5	
Temperature Under Bias	Commercial	T_{bias}	-10 to +125	°C
	Extended		-25 to +125	
Storage Temperature		T_{stg}	-65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA
Operating Temperature		T_A (Commercial Temp.)	0 to +70	°C
		T_A (Extended Temp.)	-25 to + 85	°C

NOTE :

1) Minimum DC voltage is -0.5V on Input/ Output pins. During transitions, this level may fall to -2.0V for periods <20ns.
Maximum DC voltage is Vcc+0.6V on input / output pins which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.

2) Minimum DC input voltage is -0.5V on V_{PP} . During transitions, this level may fall to -2.0V for periods <20ns.
Maximum DC input voltage is +9.5V on V_{PP} which, during transitions, may overshoot to +12.0V for periods <20ns.

3) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

13.0 RECOMMENDED OPERATING CONDITIONS (Voltage reference to GND)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	1.7	1.8	1.95	V
Supply Voltage	V_{SS}	0	0	0	V

14.0 DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}, V_{CC}=V_{CCmax}		- 1.0	-	+ 1.0	µA
VPP Leakage Current	I_{LIP}	V_{CC}=V_{CCmax} , V_{PP}=V_{CCmax}		- 1.0	-	+ 1.0	µA
		V_{CC}=V_{CCmax} , V_{PP}=9.5V		-	-	35	µA
Output Leakage Current	I_{LO}	V_{OUT}=V_{SS} to V_{CC}, V_{CC}=V_{CCmax}, $\overline{OE}$=V_{IH}		- 1.0	-	+ 1.0	µA
Active Burst Read Current	I_{CCB1}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH} (Continuous Burst, 108Mhz)		-	24	36	mA
Active Asynchronous Read Current	I_{CC1}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}	10MHz	-	27	40	mA
Active Write Current [2]	I_{CC2}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}, $\overline{WE}$=V_{IL}, V_{PP}=V_{IH}		-	15	30	mA
Read While Write Current	I_{CC3}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}		-	40	70	mA
Accelerated Program Current	I_{CC4}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH} , V_{PP}=9.5V		-	15	30	mA
Standby Current	I_{CC5}	$\overline{CE}$= $\overline{RESET}$=V_{CC} ± 0.2V		-	15	50	µA
Standby Current During Reset	I_{CC6}	$\overline{RESET}$ = V_{SS} ± 0.2V		-	15	50	µA
Automatic Sleep Mode[3]	I_{CC7}	$\overline{CE}$=V_{SS} ± 0.2V, Other Pins=V_{IL} or V_{IH} V_{IL} = V_{SS} ± 0.2V, V_{IH} = V_{CC} ± 0.2V		-	15	50	µA
Input Low Voltage	V_{IL}			-0.5	-	0.4	V
Input High Voltage	V_{IH}			V_{CC}-0.4	-	V_{CC}+0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 100 µA , V_{CC}=V_{CCmin}		-	-	0.1	V
Output High Voltage	V_{OH}	I_{OH} = -100 µA , V_{CC}=V_{CCmin}		V_{CC}-0.1	-	-	V
Voltage for Accelerated Program	V_{ID}			8.5	9.0	9.5	V
Low V_{CC} Lock-out Voltage	V_{LKO}			-	-	1.4	V

NOTE :

1) Maximum ICC specifications are tested with VCC = VCCmax.

2) ICC active while Internal Erase or Internal Program is in progress.

3) Device enters automatic sleep mode when addresses are stable for tAA + 60ns.

Vcc Power-up

Parameter	Symbol	All Speed Options		Unit
		Min	Max	
Vcc Setup Time	tVCS	200	-	μs
Time between $\overline{\text{RESET}}$ (high) and $\overline{\text{CE}}$ (low)	tRH	200	-	ns

NOTE : Not 100% tested.

SWITCHING WAVEFORMS

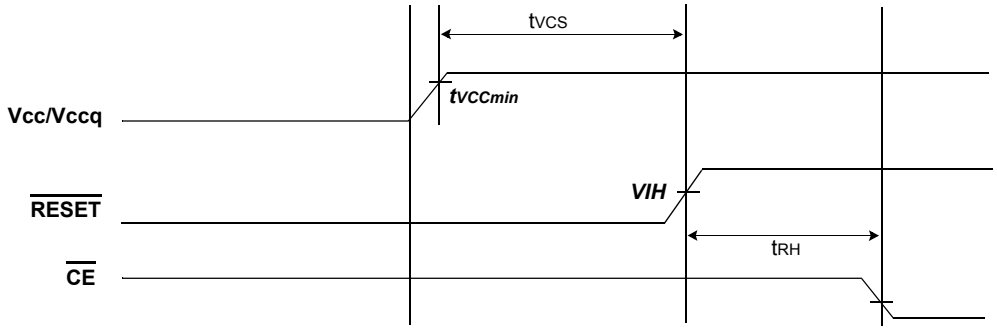


Figure 3: Vcc Power-up Diagram

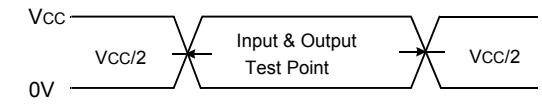
15.0 CAPACITANCE(TA = 25 °C, VCC = 1.8V, f = 1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	10	pF
Control Pin Capacitance	C_{IN2}	V_{IN}=0V	-	10	pF

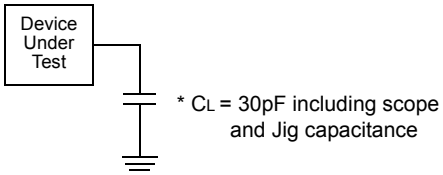
NOTE : Capacitance is periodically sampled and not 100% tested.

16.0 AC TEST CONDITION

Parameter	Value
Input Pulse Levels	0V to V_{CC}
Input Rise and Fall Times	3ns(max)@66Mhz, 2.5ns(max)@83Mhz, 1.5ns(max)@108Mhz
Input and Output Timing Levels	V_{CC}/2
Output Load	C_L = 30pF
Address to Address Skew	3ns(max)



Input Pulse and Test Point (including CLK characterization)



Output Load

17.0 AC CHARACTERISTICS

17.1 Synchronous/Burst Read

Parameter	Symbol	7B (54 MHz)		7C (66 MHz)		7D (83 MHz)		7E (108 MHz)		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Initial Access Time	t_{IAA}	-	70	-	70	-	70	-	70	ns
Burst Access Time Valid Clock to Output Delay	t_{BA}	-	14.5	-	11	-	9	-	7	ns
$\overline{AVD}$ Setup Time to CLK	t_{AVDS}	5	-	5	-	4	-	4	-	ns
$\overline{AVD}$ Hold Time from CLK	t_{AVDH}	2	-	2	-	2	-	2	-	ns
$\overline{AVD}$ High to $\overline{OE}$ Low	t_{AVDO}	0	-	0	-	0	-	0	-	ns
Address Setup Time to CLK	t_{ACS}	5	-	4	-	4	-	3.5	-	ns
Address Hold Time from CLK	t_{ACH}	7	-	6	-	5	-	2	-	ns
Data Hold Time from Next Clock Cycle	t_{BDH}	4	-	3	-	3	-	2	-	ns
Output Enable to Data	t_{OE}	-	20	-	20	-	20	-	20	ns
Output Enable to RDY valid	t_{OER}	-	14.5	-	11	-	9	-	7	ns
$\overline{CE}$ Disable to High Z	t_{CEZ}	-	15	-	15	-	11	-	8.5	ns
$\overline{OE}$ Disable to High Z	t_{OEZ}	-	9	-	9	-	9	-	9	ns
$\overline{CE}$ Setup Time to CLK	t_{CES}	6	-	6	-	4.5	-	4.5	-	ns
$\overline{CE}$ Enable to RDY active	t_{RDY}	-	7	-	7	-	7	-	7	ns
CLK to RDY Setup Time	t_{RDYA}	-	14.5	-	11	-	9	-	7	ns
RDY Setup Time to CLK	t_{RDYS}	4	-	3	-	3	-	2	-	ns
CLK period	t_{CLK}	18.5	-	15.1	-	12.05	-	9.26	-	ns
CLK High or Low Time	$t_{CLKH/L}$	0.4x t_{CLK}	0.6x t_{CLK}	0.4x t_{CLK}	0.6x t_{CLK}	0.4x t_{CLK}	0.6x t_{CLK}	0.4x t_{CLK}	0.6x t_{CLK}	ns
CLK Fall or Rise Time	t_{CLKHCL}	-	3	-	3	-	2.5	-	1.5	ns

SWITCHING WAVEFORMS

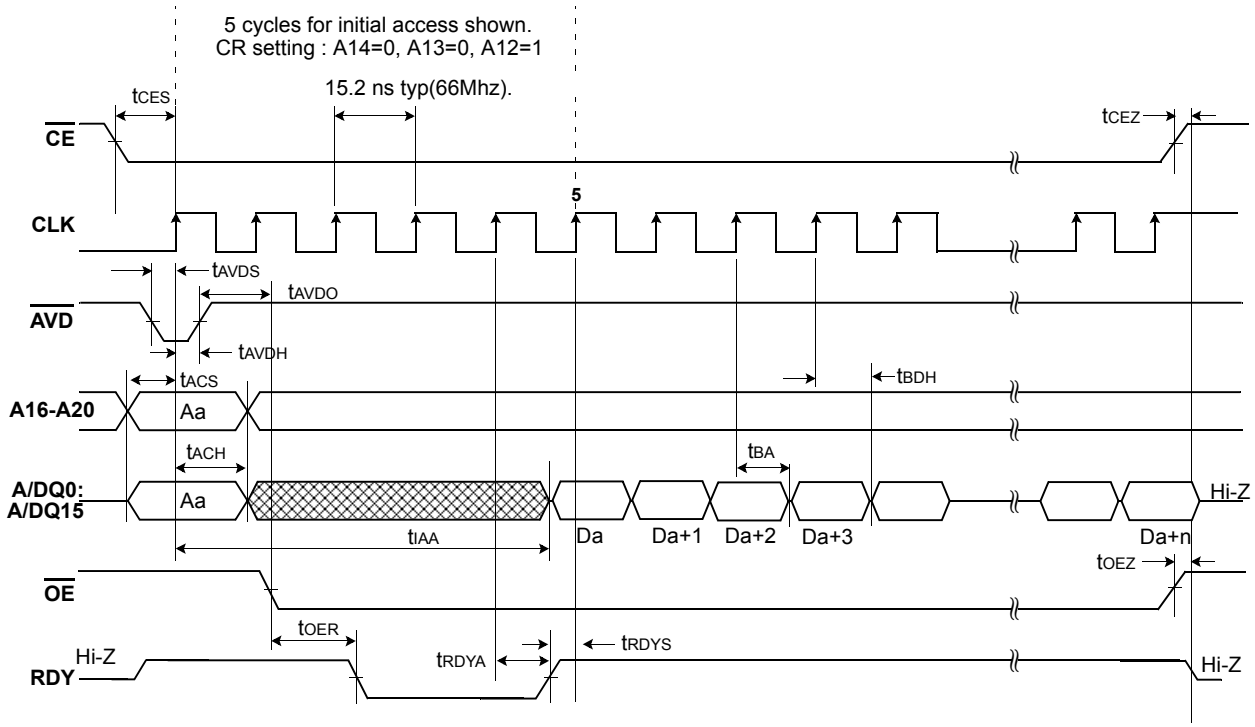


Figure 4: Continuous Burst Mode Read (66MHz)

NOTE : In order to avoid a bus conflict the $\overline{OE}$ signal is enabled on the next rising edge after $\overline{AVD}$ is going high.

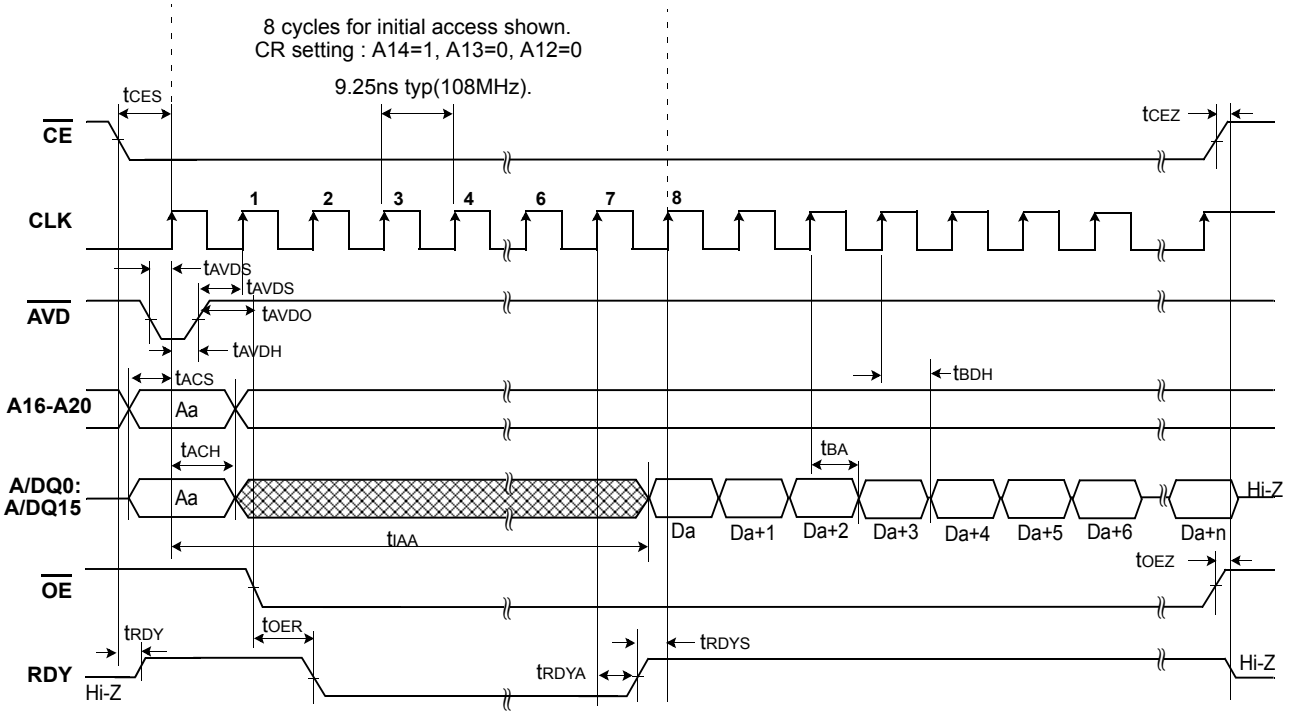


Figure 5: Continuous Burst Mode Read (108MHz)

NOTE: In order to avoid a bus conflict the $\overline{OE}$ signal is enabled on the next rising edge after $\overline{AVD}$ is going high.

SWITCHING WAVEFORMS

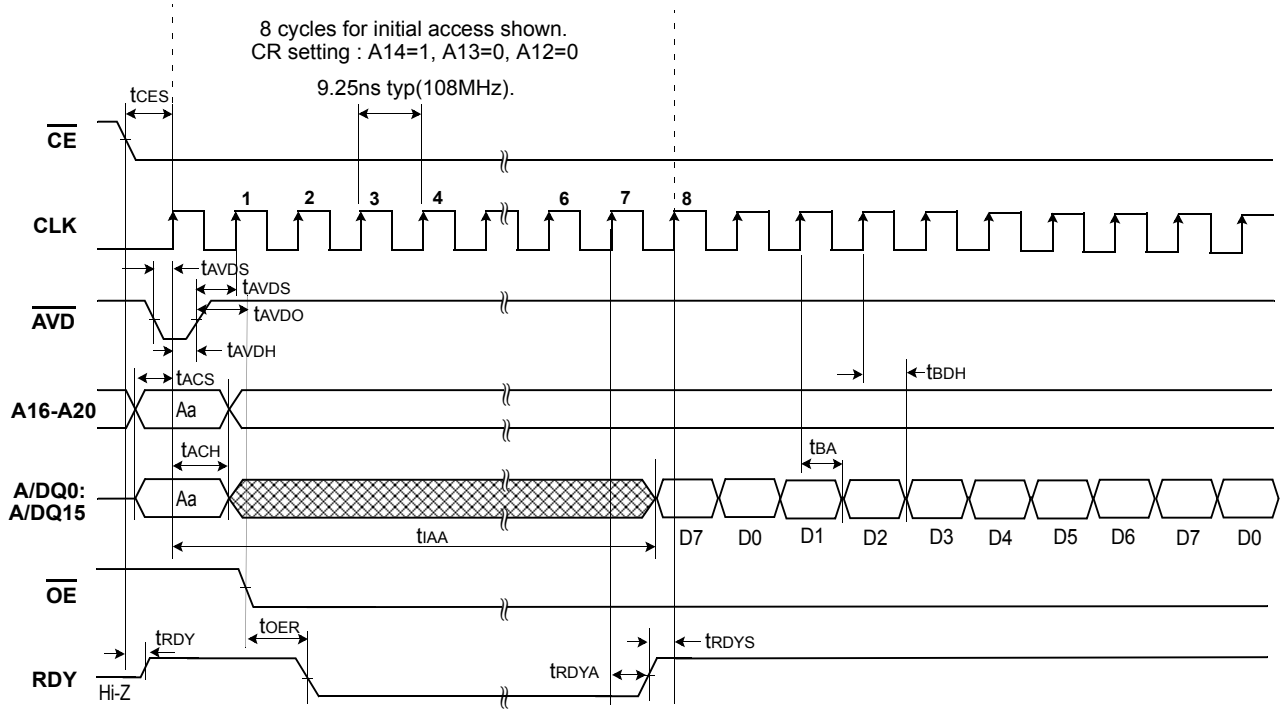


Figure 6: 8 word Linear Burst Mode with Wrap Around (108MHz)

NOTE: In order to avoid a bus conflict the $\overline{OE}$ signal is enabled on the next rising edge after $\overline{AVD}$ is going high.

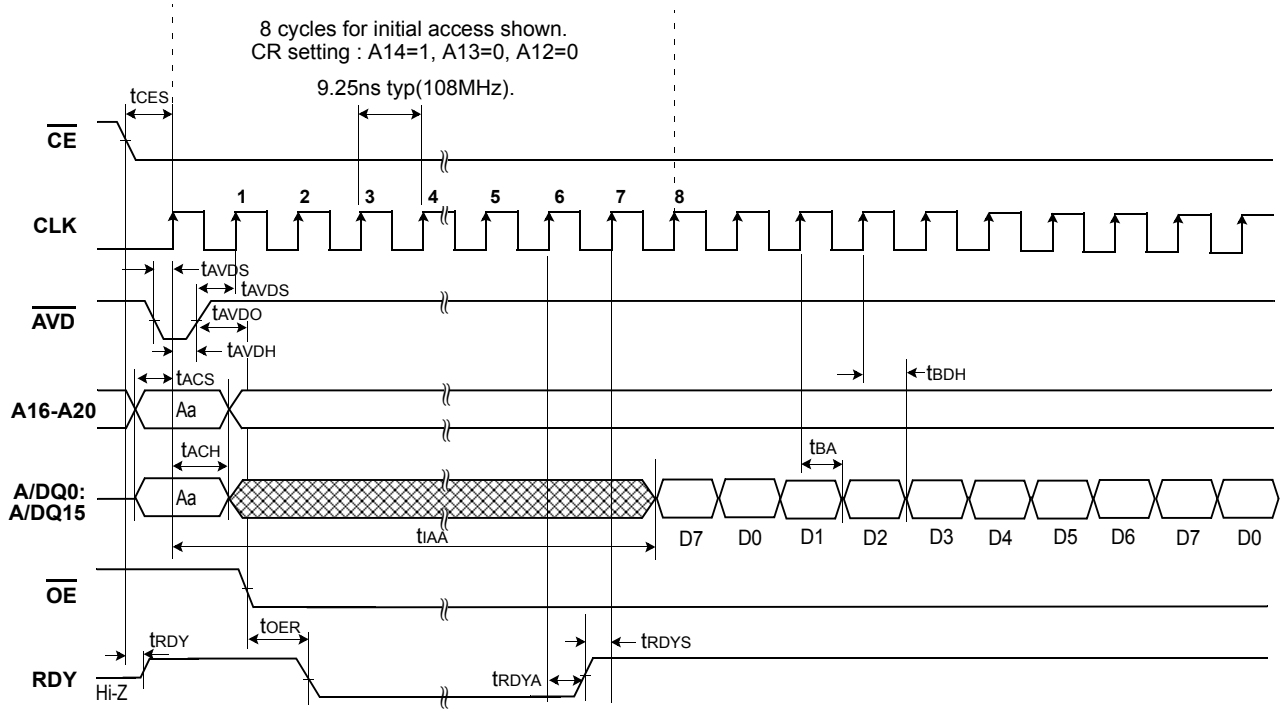


Figure 7: 8 word Linear Burst with RDY Set One Cycle Before Data (Wrap Around Mode, CR setting : A18=1)

NOTE: In order to avoid a bus conflict the $\overline{OE}$ signal is enabled on the next rising edge after $\overline{AVD}$ is going high.

SWITCHING WAVEFORMS

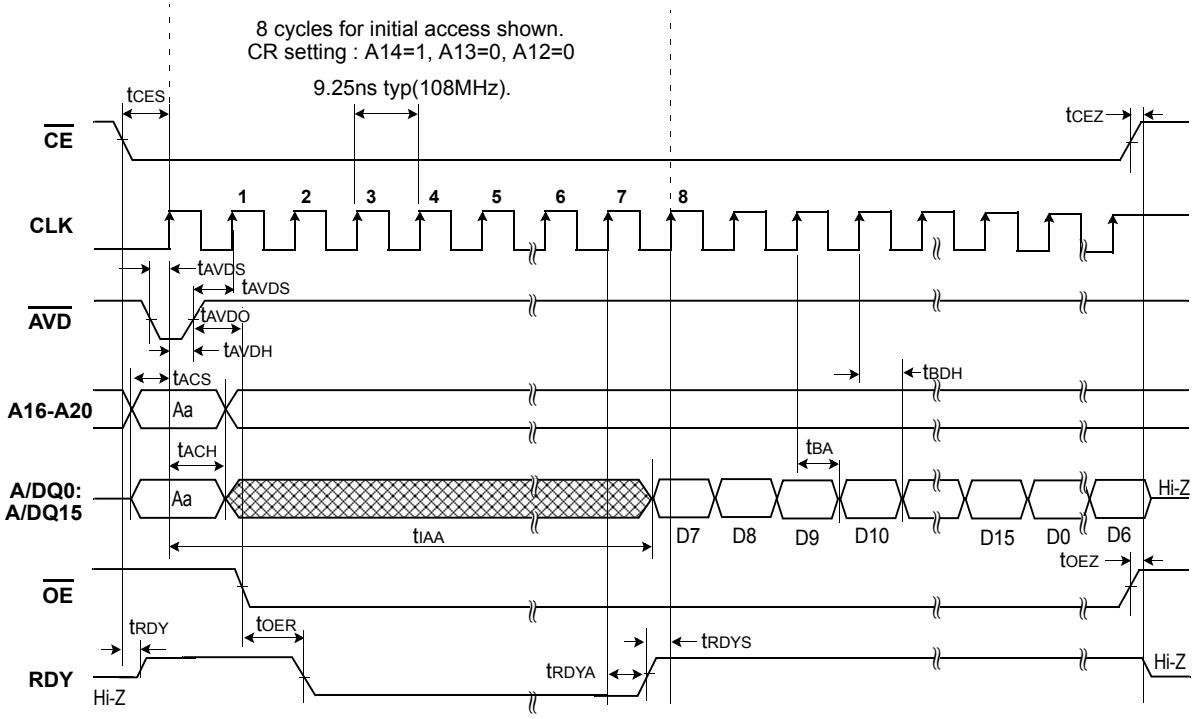


Figure 8: 16 word Linear Burst Mode with Wrap Around (108Mhz)

NOTE: In order to avoid a bus conflict the $\overline{OE}$ signal is enabled on the next rising edge after $\overline{AVD}$ is going high.

17.2 Asynchronous Read

Parameter		Symbol	All Speed option		Unit
			Min	Max	
Access Time from $\overline{CE}$ Low		tCE	-	70	ns
Asynchronous Access Time		tAA	-	70	ns
$\overline{AVD}$ Low Time		tAVDP	9	-	ns
Address Setup Time to rising Edge of AVD		tAAVDS	4	-	ns
Address Hold Time from Rising Edge of AVD		tAAVDH	6	-	ns
Output Enable to Output Valid		tOE	-	20	ns
Output Enable Hold Time	Read	tOEH	0	-	ns
	Toggle and Data Polling		10	-	ns
Output Disable to High Z[1)]		tOEZ	-	9	ns

NOTE:
1) Not 100% tested.

SWITCHING WAVEFORMS
Asynchronous Mode Read (tCE)

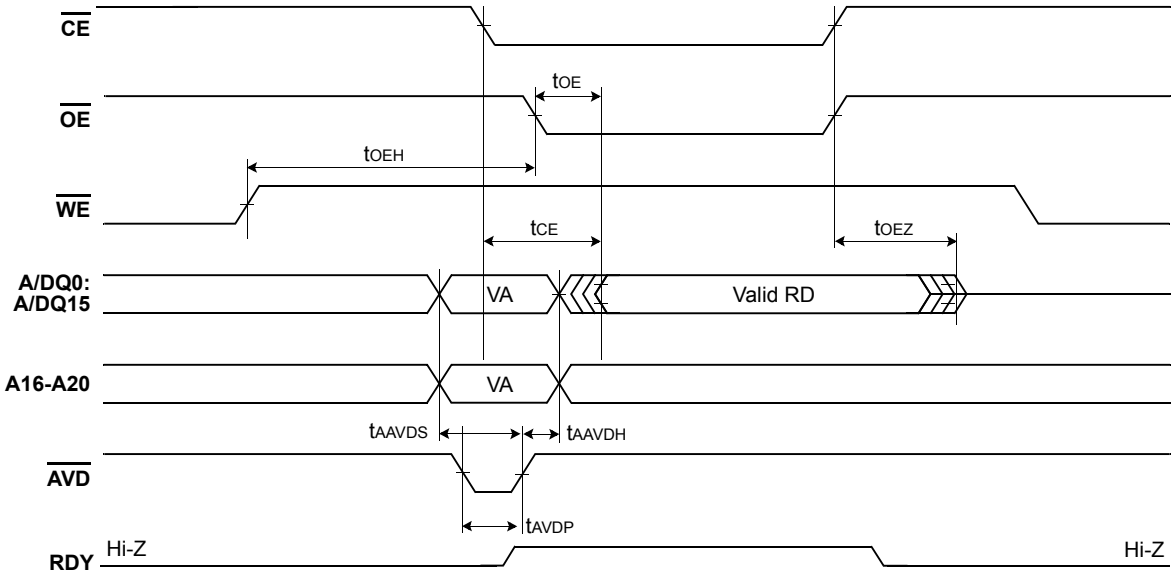


Figure 9: Asynchronous Mode Read (tCE)

Asynchronous Mode Read (tAA)

Case 1 : Valid Address Transition occurs before $\overline{AVD}$ is driven to Low

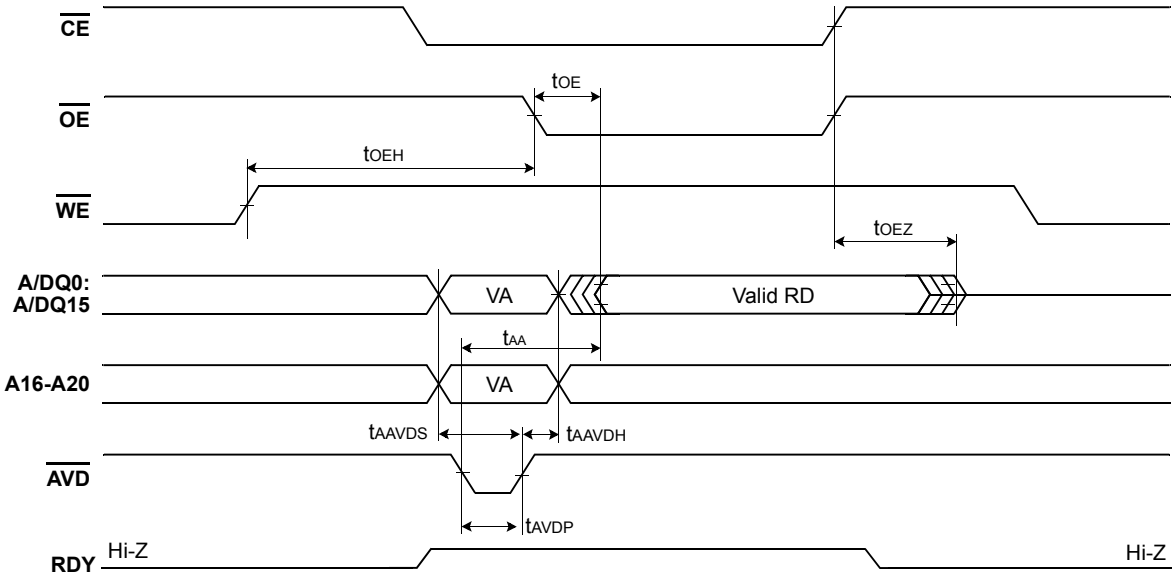


Figure 10: Asynchronous Mode Read (tAA) : Case 1

Case 2 : Valid Address Transition occurs after $\overline{AVD}$ is driven to Low

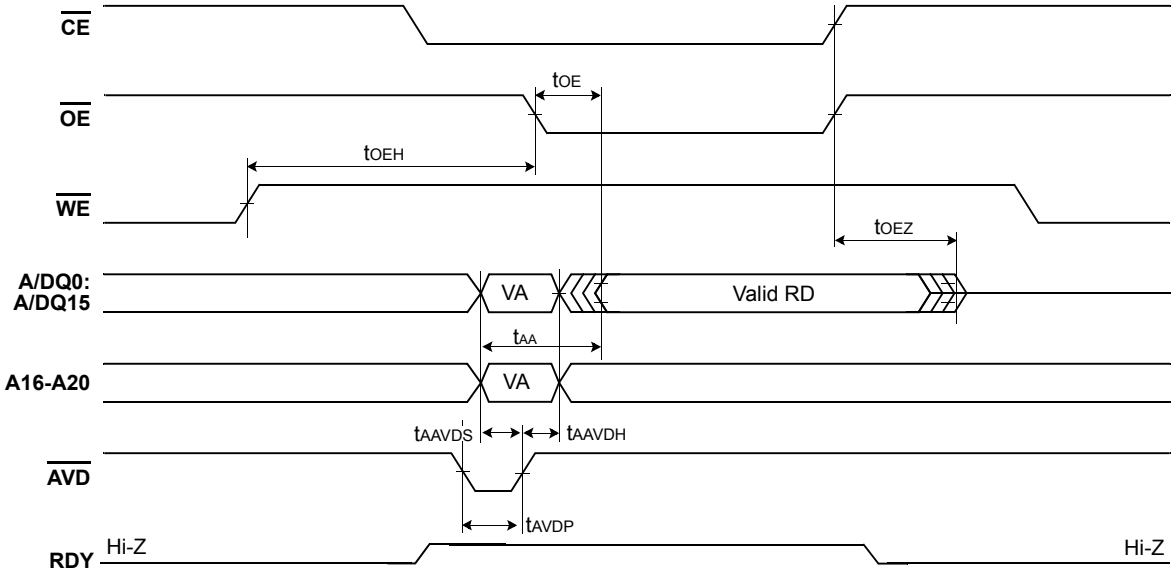


Figure 11: Asynchronous Mode Read (tAA) : Case 2

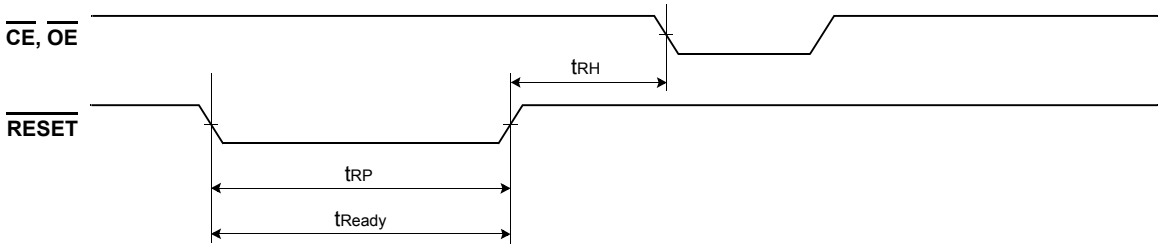
NOTE :
VA=Valid Read Address, RD=Read Data.
Asynchronous mode may not support read following four sequential invalid read condition within 200ns.

17.3 Hardware Reset($\overline{\text{RESET}}$)

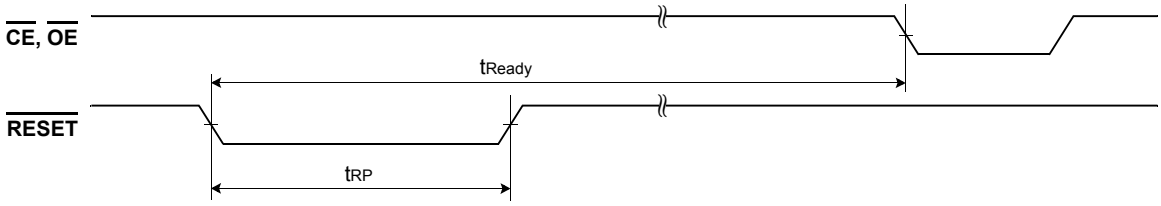
Parameter	Symbol	All Speed Options		Unit
		Min	Max	
$\overline{\text{RESET}}$ Pin Low(During Internal Routines) to Read Mode (Note)	tReady	-	20	μs
$\overline{\text{RESET}}$ Pin Low(NOT During Internal Routines) to Read Mode (Note)	tReady	-	500	ns
$\overline{\text{RESET}}$ Pulse Width*	tRP	200	-	ns
Reset High Time Before Read (Note)	tRH	200	-	ns

NOTE : Not 100% tested.

SWITCHING WAVEFORMS



Reset Timings NOT during Internal Routines



Reset Timings during Internal Routines

Figure 12: Reset Timings

17.4 Erase/Program Operation

Parameter	Symbol	All Speed Option			Unit
		Min	Typ	Max	
$\overline{WE}$ Cycle Time[1)]	tWC	60	-	-	ns
Address Setup Time	tAS	4	-	-	ns
Address Hold Time	tAH	5.5	-	-	ns
$\overline{AVD}$ Low Time	tAVDP	9	-	-	ns
Data Setup Time	tDS	30	-	-	ns
Data Hold Time	tDH	0	-	-	ns
Read Recovery Time Before Write	tGHWL	0	-	-	ns
$\overline{CE}$ Setup Time	tCS	0	-	-	ns
$\overline{CE}$ Hold Time	tCH	0	-	-	ns
$\overline{WE}$ Disable to $\overline{AVD}$ Enable	tWEA	30	-	-	ns
$\overline{WE}$ Pulse Width	tWP	30	-	-	ns
$\overline{WE}$ Pulse Width High	tWPH	30	-	-	ns
Latency Between Read and Write Operations	tSR/W	0	-	-	ns
Word Programming Operation	tPGM	-	11.5	-	µs
Accelerated Single word Programming Operation	tACCPGM	-	6.5	-	µs
Accelerated Quad word Programming Operation	tACCPGM_QUAD	-	6.5	-	µs
Main Block Erase Operation [2)]	tBERS	-	0.7	-	sec
VPP Rise and Fall Time	tVPP	500	-	-	ns
VPP Setup Time (During Accelerated Programming)	tVPS	1	-	-	µs

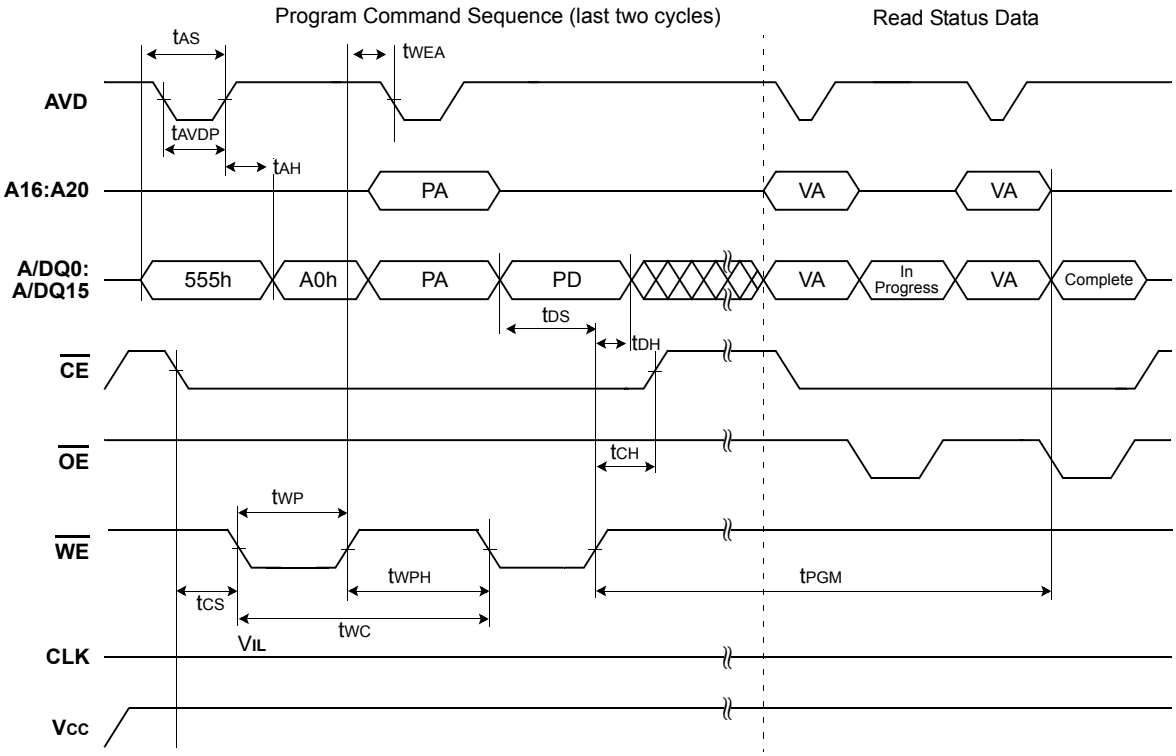
NOTE :
1) Not 100% tested.
2) Not include the preprogramming time.

17.5 FLASH Erase/Program Performance

Parameter		Limits			Unit	Comments
		Min.	Typ.	Max.		
Block Erase Time	32 Kword	-	0.7	14	sec	Includes 00h programming prior to erasure
	4 Kword	-	0.2	4		
Chip Erase Time		-	45	-		
Accelerated Chip Erase Time		-	30	-		
Word Programming Time		-	11.5	210	µs	Excludes system level overhead
Accelerated Sinlge Programming Time		-	6.5	120		
Accelerated Quad Programming Time (@word)			1.6	30	µs	
Chip Programming Time		-	23	-	sec	
Accelerated Single word Chip Programming		-	13	-		
Accelerated Quad word Chip Programming Time		-	3	-	sec	

NOTE :
1) 25°C, VCC = 1.8V, 100,000 cycles, typical pattern.
2) System-level overhead is defined as the time required to execute the two or four bus cycle command necessary to program each word. In the preprogramming step of the Internal Erase Routine, all words are programmed to 00H before erase.

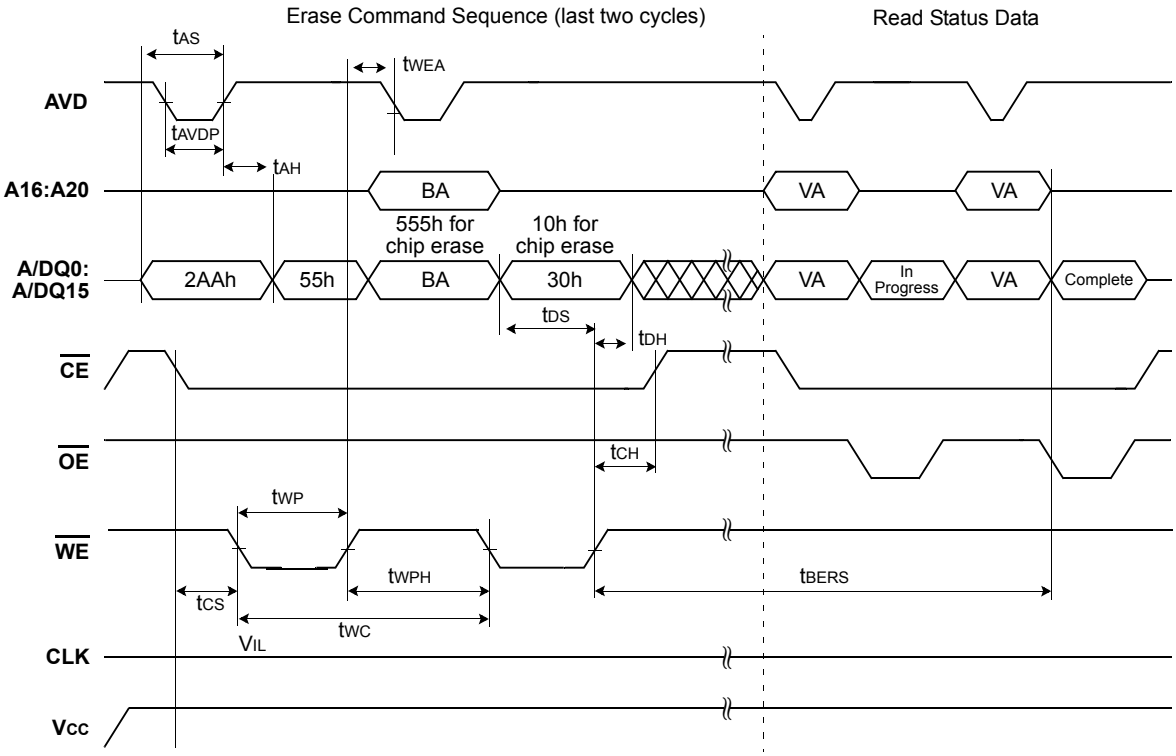
SWITCHING WAVEFORMS
Program Operations



NOTE :
1) PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.
2) “In progress” and “complete” refer to status of program operation.
3) A16–A20 are don’t care during command sequence unlock cycles.
4) Status reads in this figure is asynchronous read, but status read in synchronous mode is also supported.

Figure 13: Program Operation Timing

SWITCHING WAVEFORMS
Erase Operation



NOTE :

1) BA is the block address for Block Erase.

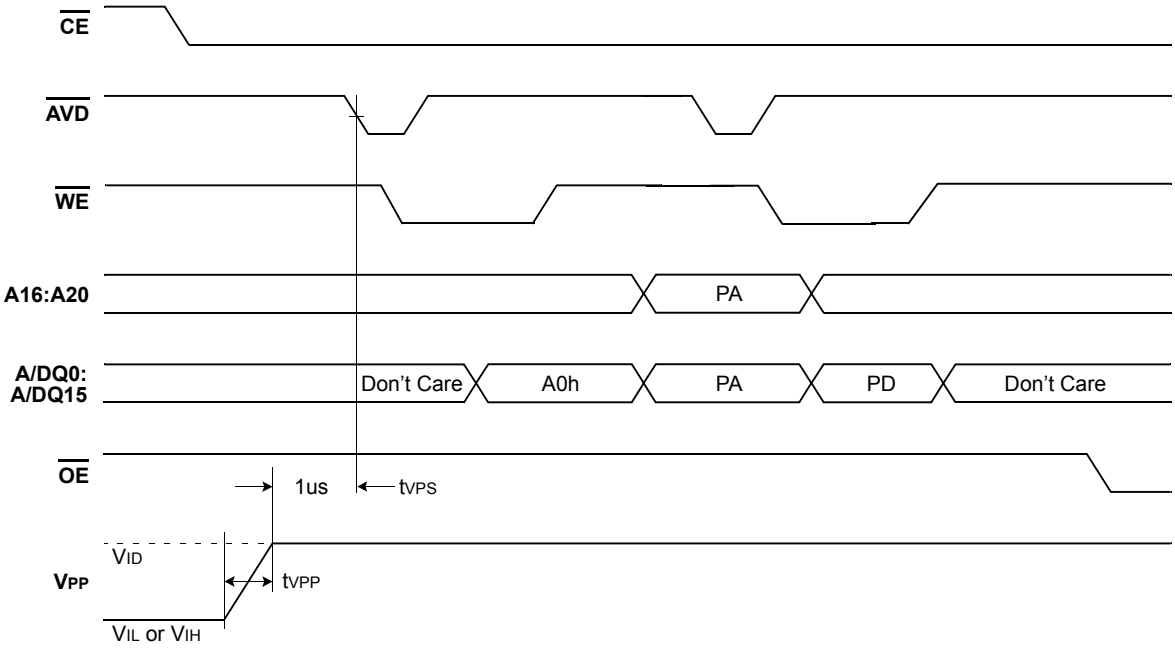
2) Address bits A16–A20 are don't cares during unlock cycles in the command sequence.

3) Status reads in this figure is asynchronous read, but status read in synchronous mode is also supported.

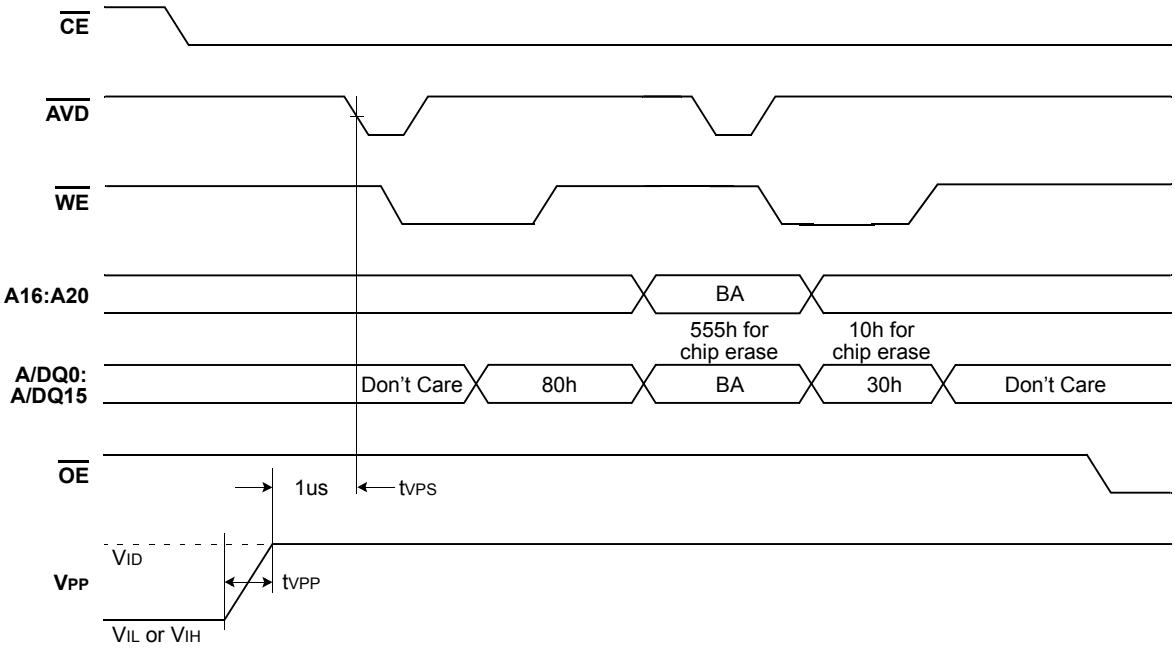
Figure 14: Chip/Block Erase Operations

SWITCHING WAVEFORMS

Unlock Bypass Program Operations(Accelerated Program)



Unlock Bypass Block Erase Operations



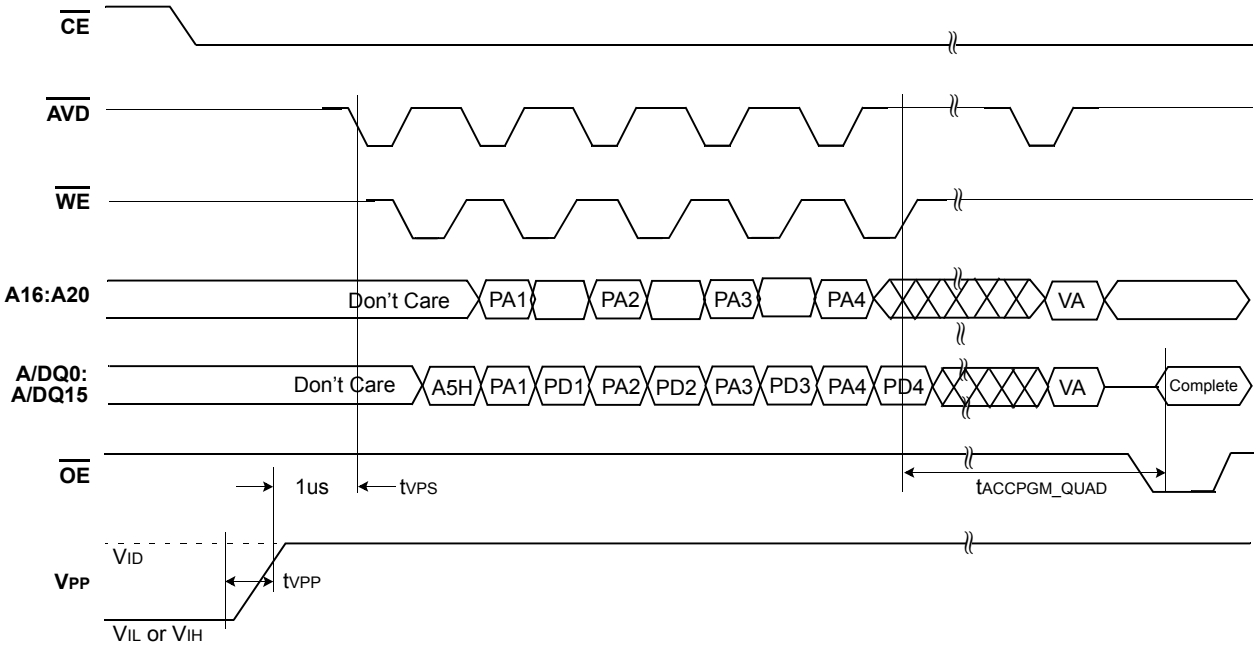
NOTE :

1) VPP can be left high for subsequent programming pulses.
2) Use setup and hold times from conventional program operations.
3) Unlock Bypass Program/Erase commands can be used when the VID is applied to Vpp.

Figure 15: Unlock Bypass Operation Timings

SWITCHING WAVEFORMS

Quad word Accelerated Program



NOTE :

1) VPP can be left high for subsequent programming pulses.

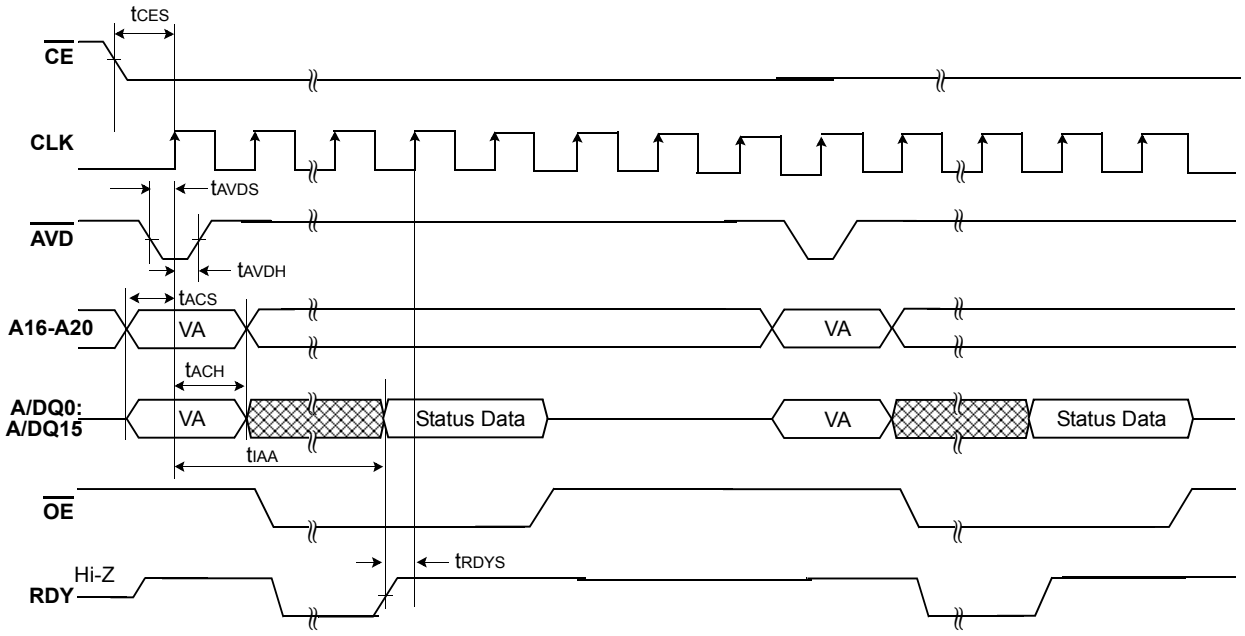
2) Use setup and hold times from conventional program operations.

3) Quad word Acelerate program commands can be used when the VID is applied to Vpp.

Figure 16: Quad word Accelerated Program Operation Timings

SWITCHING WAVEFORMS

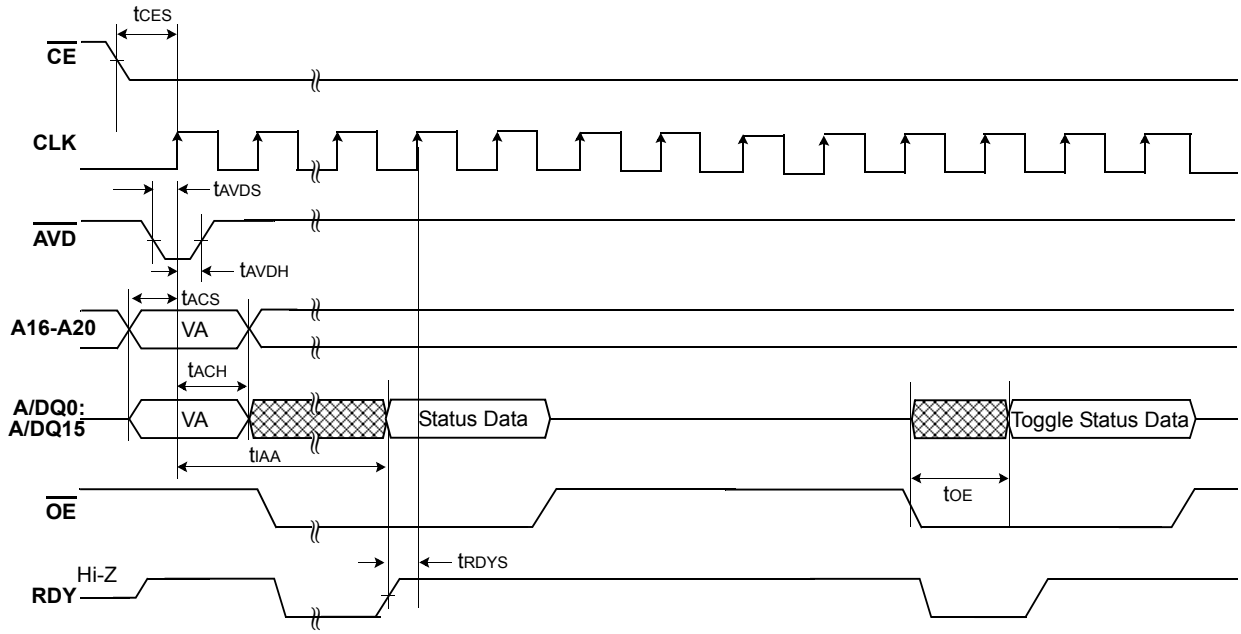
Data Polling Operations



NOTE :
1) VA = Valid Address. When the Internal Routine operation is complete, and $\overline{\text{Data}}$ Polling will output true data.

Figure 17: $\overline{\text{Data}}$ Polling Timings (During Internal Routine)

Toggle Bit Operations



NOTE :
1) VA = Valid Address. When the Internal Routine operation is complete, the toggle bits will stop toggling.

Figure 18: Toggle Bit Timings(During Internal Routine)

SWITCHING WAVEFORMS
Read While Write Operations

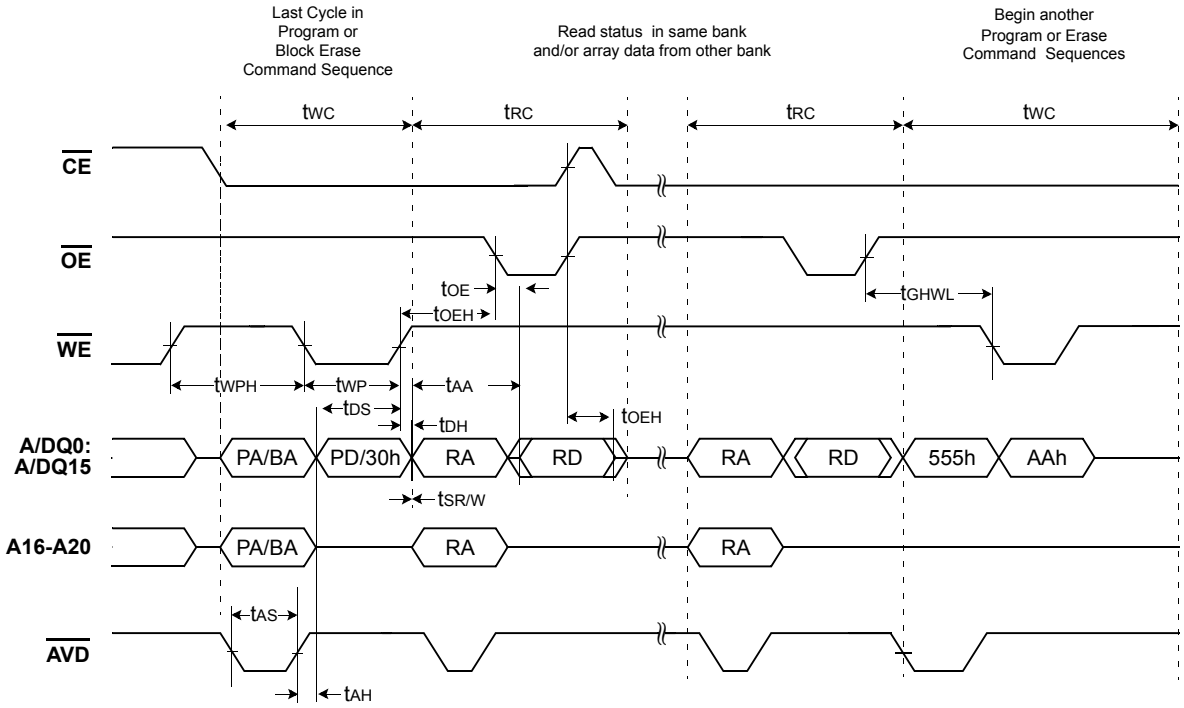


Figure 19: Read While Write Operation

NOTE :
Breakpoints in waveforms indicate that system may alternately read array data from the “non-busy bank” and checking the status of the program or erase operation in the “busy” bank.

18.0 Crossing of First Word Boundary in Burst Read Mode

The additional clock insertion for word boundary is needed only at the first crossing of word boundary. This means that no additional clock cycle is needed from 2nd word boundary crossing to the end of continuous burst read. Also, the number of additional clock cycle for the first word boundary can varies from zero to seven cycles, and the exact number of additional clock cycle depends on the starting address of burst read.

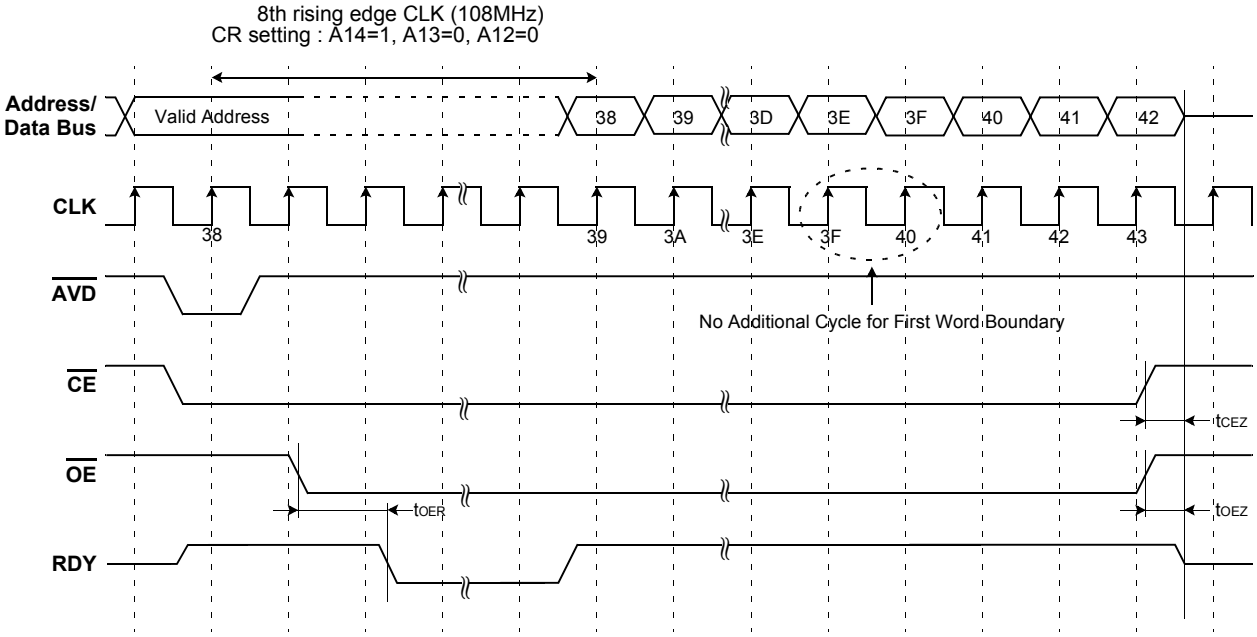
The rule to determine the additional clock cycle is as follows. All addresses can be divided into 8 groups. The applied rule is "The residue obtained when the address is divided by 8" or "three LSB bits of address". Using this rule, all address can be divided by 8 different groups as shown in below table. For simplicity of terminology, "8N" stands for the address of which the residue is "0"(or the three LSB bits are "000") and "8N+1" for the address of which the residue is "1"(or the three LSB bits are "001"), etc.

The additional clock cycles for first word boundary crossing are zero, one, two ... or seven when the burst read start from "8N" address, "8N+1" address, "8N+2" address .... or "8N+7" address respectively.

Starting Address vs. Additional Clock Cycles for first word boundary

Srarting Address Group for Burst Read	The Residue of (Address/8)	LSB Bits of Address	Additional Clock Cycles for First Word Boundary				
			A14~A12 "000" Valid data : 4th CLK	A14~A12 "001" Valid data : 5th CLK	A14~A12 "010" Valid data : 6th CLK	A14~A12 "011" Valid data : 7th CLK	A14~A12 "100" Valid data : 8th CLK
8N	0	000	0 cycle	0 cycle	0 cycle	0 cycle	0 cycle
8N+1	1	001	0 cycle	0 cycle	0 cycle	0 cycle	1 cycle
8N+2	2	010	0 cycle	0 cycle	0 cycle	1 cycle	2 cycle
8N+3	3	011	0 cycle	0 cycle	1 cycle	2 cycle	3 cycle
8N+4	4	100	0 cycle	1 cycle	2 cycle	3 cycle	4 cycle
8N+5	5	101	1 cycle	2 cycle	3 cycle	4 cycle	5 cycle
8N+6	6	110	2 cycle	3 cycle	4 cycle	5 cycle	6 cycle
8N+7	7	111	3 cycle	4 cycle	5 cycle	6 cycle	7 cycle

Case 1 : Start from "8N" address group

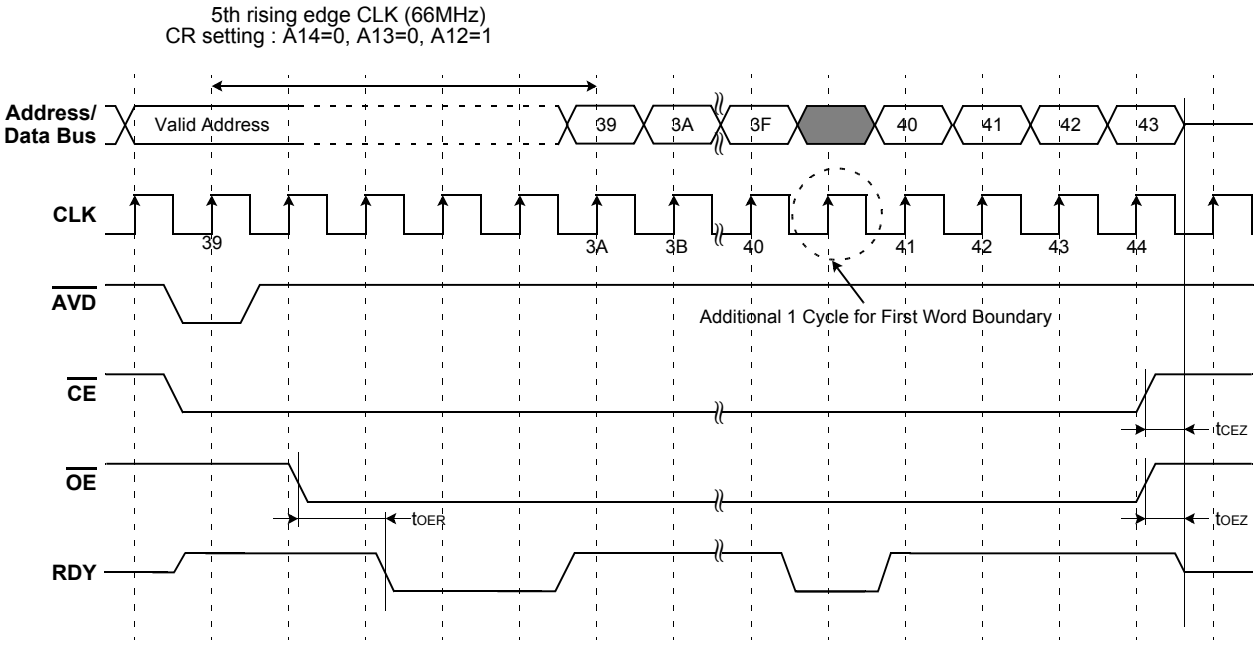


NOTE :

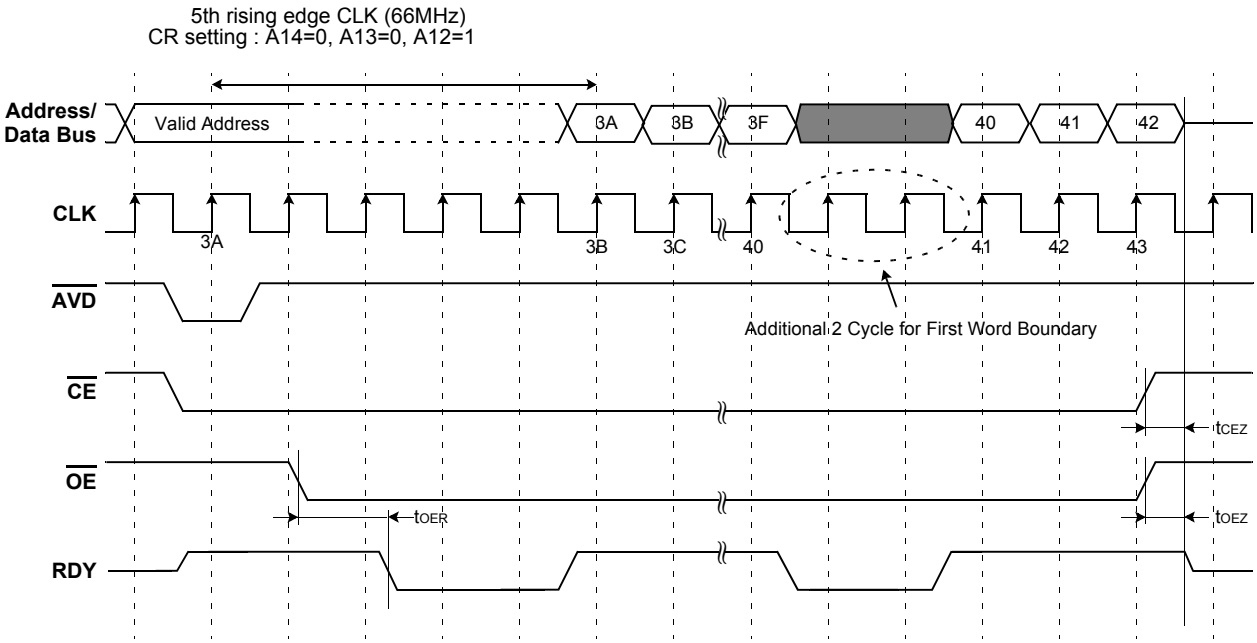
1) Address boundary occurs every 16 words beginning at address 00000FH , 00001FH , 00002FH , etc.
2) Address 000000H is also a boundary crossing.
3) No additional clock cycles are needed except for 1st boundary crossing.

Figure 20: Crossing of first word boundary in burst read mode.

Case2 : Start from "8N+4" address group



Case 3 : Start from "8N+5" address group



NOTE :

1) Address boundary occurs every 16 words beginning at address 00000FH , 00001FH , 00002FH , etc.
2) Address 000000H is also a boundary crossing.
3) No additional clock cycles are needed except for 1st boundary crossing.

Figure 21: Crossing of first word boundary in burst read mode.

Table 16: Top Boot Block Address Table

Bank	Block	Block Size	(x16) Address Range
Bank 0	BA70	4 Kwords	1FF000h-1FFFFFh
	BA69	4 Kwords	1FE000h-1FEFFFh
	BA68	4 Kwords	1FD000h-1FDFFFh
	BA67	4 Kwords	1FC000h-1FCFFFh
	BA66	4 Kwords	1FB000h-1FBFFFh
	BA65	4 Kwords	1FA000h-1FAFFFh
	BA64	4 Kwords	1F9000h-1F9FFFh
	BA63	4 Kwords	1F8000h-1F8FFFh
	BA62	32 Kwords	1F0000h-1F7FFFh
	BA61	32 Kwords	1E8000h-1EFFFFh
	BA60	32 Kwords	1E0000h-1E7FFFh
Bank 1	BA59	32 Kwords	1D8000h-1DFFFFh
	BA58	32 Kwords	1D0000h-1D7FFFh
	BA57	32 Kwords	1C8000h-1CFFFFh
	BA56	32 Kwords	1C0000h-1C7FFFh
Bank 2	BA55	32 Kwords	1B8000h-1BFFFFh
	BA54	32 Kwords	1B0000h-1B7FFFh
	BA53	32 Kwords	1A8000h-1AFFFFh
	BA52	32 Kwords	1A0000h-1A7FFFh
Bank 3	BA51	32 Kwords	198000h-19FFFFh
	BA50	32 Kwords	190000h-197FFFh
	BA49	32 Kwords	188000h-18FFFFh
	BA48	32 Kwords	180000h-187FFFh
Bank 4	BA47	32 Kwords	178000h-17FFFFh
	BA46	32 Kwords	170000h-177FFFh
	BA45	32 Kwords	168000h-16FFFFh
	BA44	32 Kwords	160000h-167FFFh
Bank 5	BA43	32 Kwords	158000h-15FFFFh
	BA42	32 Kwords	150000h-157FFFh
	BA41	32 Kwords	148000h-14FFFFh
	BA40	32 Kwords	140000h-147FFFh
Bank 6	BA39	32 Kwords	138000h-13FFFFh
	BA38	32 Kwords	130000h-137FFFh
	BA37	32 Kwords	128000h-12FFFFh
	BA36	32 Kwords	120000h-127FFFh
Bank 7	BA35	32 Kwords	118000h-11FFFFh
	BA34	32 Kwords	110000h-117FFFh
	BA33	32 Kwords	108000h-10FFFFh
	BA32	32 Kwords	100000h-107FFFh
Bank 8	BA31	32 Kwords	0F8000h-0FFFFFh
	BA30	32 Kwords	0F0000h-0F7FFFh
	BA29	32 Kwords	0E8000h-0EFFFFh
	BA28	32 Kwords	0E0000h-0E7FFFh

Table 13:Top Boot Block Address Table

Bank	Block	Block Size	(x16) Address Range
Bank 9	BA27	32 Kwords	0D8000h-0DFFFFh
	BA26	32 Kwords	0D0000h-0D7FFFh
	BA25	32 Kwords	0C8000h-0CFFFFh
	BA24	32 Kwords	0C0000h-0C7FFFh
Bank 10	BA23	32 Kwords	0B8000h-0BFFFFh
	BA22	32 Kwords	0B0000h-0B7FFFh
	BA21	32 Kwords	0A8000h-0AFFFFh
	BA20	32 Kwords	0A0000h-0A7FFFh
Bank 11	BA19	32 Kwords	098000h-09FFFFh
	BA18	32 Kwords	090000h-097FFFh
	BA17	32 Kwords	088000h-08FFFFh
	BA16	32 Kwords	080000h-087FFFh
Bank 12	BA15	32 Kwords	078000h-07FFFFh
	BA14	32 Kwords	070000h-077FFFh
	BA13	32 Kwords	068000h-06FFFFh
	BA12	32 Kwords	060000h-067FFFh
Bank 13	BA11	32 Kwords	058000h-05FFFFh
	BA10	32 Kwords	050000h-057FFFh
	BA9	32 Kwords	048000h-04FFFFh
	BA8	32 Kwords	040000h-047FFFh
Bank 14	BA7	32 Kwords	038000h-03FFFFh
	BA6	32 Kwords	030000h-037FFFh
	BA5	32 Kwords	028000h-02FFFFh
	BA4	32 Kwords	020000h-027FFFh
Bank 15	BA3	32 Kwords	018000h-01FFFFh
	BA2	32 Kwords	010000h-017FFFh
	BA1	32 Kwords	008000h-00FFFFh
	BA0	32 Kwords	000000h-007FFFh

Table 17: Top Boot Block OTP Block Addresses

OTP	Block Address A20 ~ A8	Block Size	(x16) Address Range
	1FFFh	256words	1FFF00h-1FFFFFh

After entering OTP block, any issued addresses should be in the range of OTP block address

Table 18: Bottom Boot Block Address Table

Bank	Block	Block Size	(x16) Address Range
Bank15	BA70	32 Kwords	1F8000h-1FFFFFh
	BA69	32 Kwords	1F0000h-1F7FFFh
	BA68	32 Kwords	1E8000h-1EFFFFh
	BA67	32 Kwords	1E0000h-1E7FFFh
Bank14	BA66	32 Kwords	1D8000h-1DFFFFh
	BA65	32 Kwords	1D0000h-1D7FFFh
	BA64	32 Kwords	1C8000h-1CFFFFh
	BA63	32 Kwords	1C0000h-1C7FFFh
Bank13	BA62	32 Kwords	1B8000h-1BFFFFh
	BA61	32 Kwords	1B0000h-1B7FFFh
	BA60	32 Kwords	1A8000h-1AFFFFh
	BA59	32 Kwords	1A0000h-1A7FFFh
Bank12	BA58	32 Kwords	198000h-19FFFFh
	BA57	32 Kwords	190000h-197FFFh
	BA56	32 Kwords	188000h-18FFFFh
	BA55	32 Kwords	180000h-187FFFh
Bank11	BA54	32 Kwords	178000h-17FFFFh
	BA53	32 Kwords	170000h-177FFFh
	BA52	32 Kwords	168000h-16FFFFh
	BA51	32 Kwords	160000h-167FFFh
Bank10	BA50	32 Kwords	158000h-15FFFFh
	BA49	32 Kwords	150000h-157FFFh
	BA48	32 Kwords	148000h-14FFFFh
	BA47	32 Kwords	140000h-147FFFh
Bank 9	BA46	32 Kwords	138000h-13FFFFh
	BA45	32 Kwords	130000h-137FFFh
	BA44	32 Kwords	128000h-12FFFFh
	BA43	32 Kwords	120000h-127FFFh
Bank 8	BA42	32 Kwords	118000h-11FFFFh
	BA41	32 Kwords	110000h-117FFFh
	BA40	32 Kwords	108000h-10FFFFh
	BA39	32 Kwords	100000h-107FFFh
Bank 7	BA38	32 Kwords	0F8000h-0FFFFFh
	BA37	32 Kwords	0F0000h-0F7FFFh
	BA36	32 Kwords	0E8000h-0EFFFFh
	BA35	32 Kwords	0E0000h-0E7FFFh

Table 15 : Bottom Boot Block Address Table

Bank	Block	Block Size	(x16) Address Range
Bank 6	BA34	32 Kwords	0D8000h-0DFFFFh
	BA33	32 Kwords	0D0000h-0D7FFFh
	BA32	32 Kwords	0C8000h-0CFFFFh
	BA31	32 Kwords	0C0000h-0C7FFFh
Bank 5	BA30	32 Kwords	0B8000h-0BFFFFh
	BA29	32 Kwords	0B0000h-0B7FFFh
	BA28	32 Kwords	0A8000h-0AFFFFh
	BA27	32 Kwords	0A0000h-0A7FFFh
Bank 4	BA26	32 Kwords	098000h-09FFFFh
	BA25	32 Kwords	090000h-097FFFh
	BA24	32 Kwords	088000h-08FFFFh
	BA23	32 Kwords	080000h-087FFFh
Bank 3	BA22	32 Kwords	078000h-07FFFFh
	BA21	32 Kwords	070000h-077FFFh
	BA20	32 Kwords	068000h-06FFFFh
	BA19	32 Kwords	060000h-067FFFh
Bank 2	BA18	32 Kwords	058000h-05FFFFh
	BA17	32 Kwords	050000h-057FFFh
	BA16	32 Kwords	048000h-04FFFFh
	BA15	32 Kwords	040000h-047FFFh
Bank 1	BA14	32 Kwords	038000h-03FFFFh
	BA13	32 Kwords	030000h-037FFFh
	BA12	32 Kwords	028000h-02FFFFh
	BA11	32 Kwords	020000h-027FFFh
Bank 0	BA10	32 Kwords	018000h-01FFFFh
	BA9	32 Kwords	010000h-017FFFh
	BA8	32 Kwords	008000h-00FFFFh
	BA7	4 Kwords	007000h-007FFFh
	BA6	4 Kwords	006000h-006FFFh
	BA5	4 Kwords	005000h-005FFFh
	BA4	4 Kwords	004000h-004FFFh
	BA3	4 Kwords	003000h-003FFFh
	BA2	4 Kwords	002000h-002FFFh
	BA1	4 Kwords	001000h-001FFFh
	BA0	4 Kwords	000000h-000FFFh

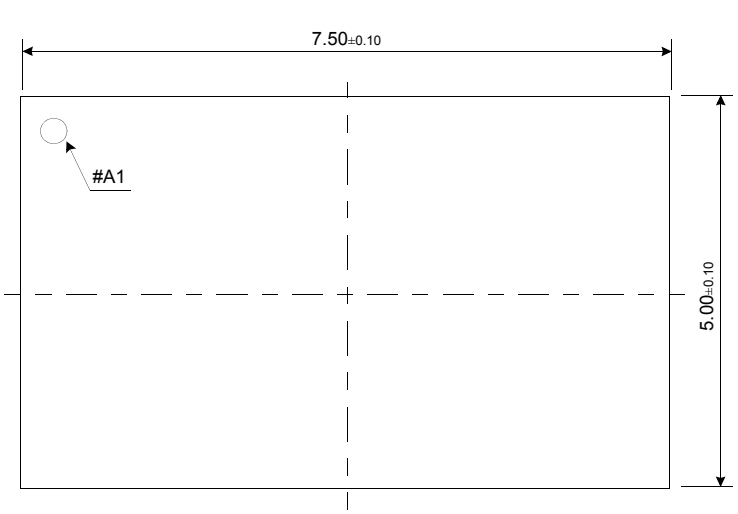
Table 19: Bottom Boot Block OTP Block Addresses

OTP	Block Address A20 ~ A8	Block Size	(x16) Address Range
	0000h	256words	000000h-0000FFh

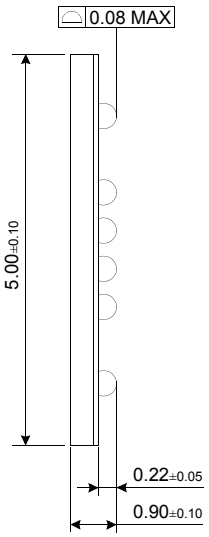
After entering OTP block, any issued addresses should be in the range of OTP block address

19.0 PACKAGE DIMENSIONS

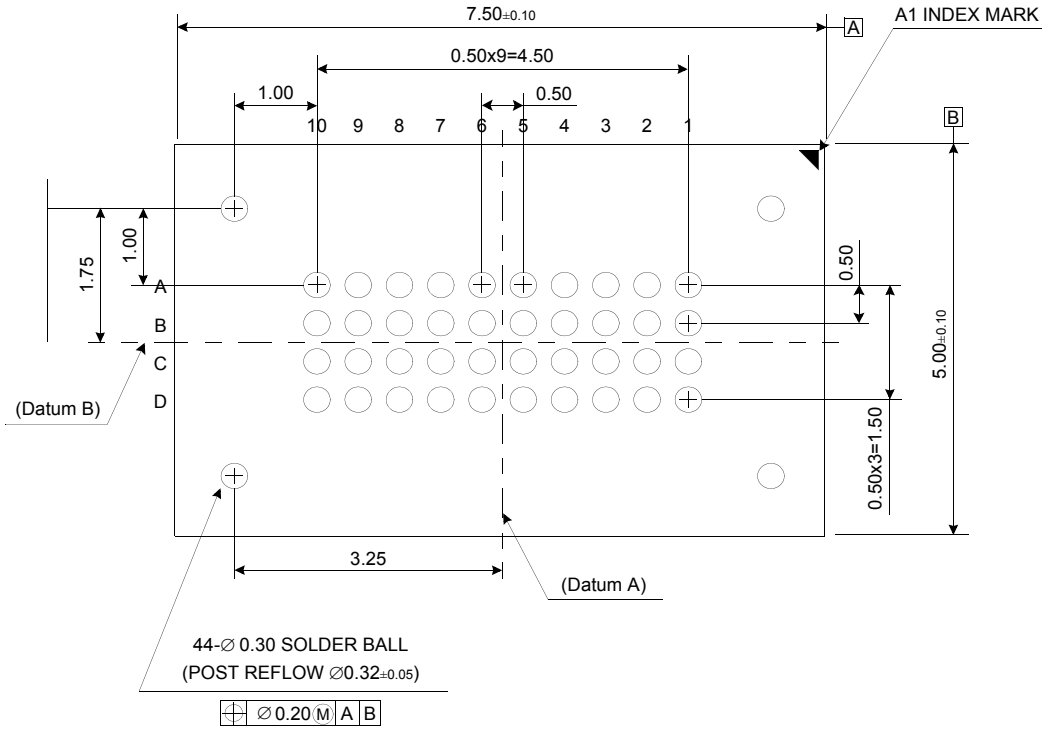
44-Ball FBGA (measured in millimeters)



Top View



Side View



Bottom View