

100-Pin TQFP
Commercial Temp
Industrial Temp

1M x 18, 512K x 36
18Mb Sync Burst SRAMs

250 MHz–133 MHz
2.5 V or 3.3 V V_{DD}
2.5 V or 3.3 V I/O

Features

- $\overline{FT}$ pin for user-configurable flow through or pipeline operation
- Dual Cycle Deselect (DCD) operation
- 2.5 V or 3.3 V +10%/–10% core power supply
- 2.5 V or 3.3 V I/O supply
- $\overline{LBO}$ pin for Linear or Interleaved Burst mode
- Internal input resistors on mode pins allow floating mode pins
- Default to Interleaved Pipeline mode
- Byte Write ($\overline{BW}$) and/or Global Write ($\overline{GW}$) operation
- Internal self-timed write cycle
- Automatic power-down for portable applications
- JEDEC-standard 100-lead TQFP package

Functional Description

Applications

The GS8160E18/32/36T is an 18,874,368-bit (16,777,216-bit for x32 version) high performance synchronous SRAM with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM applications, ranging from DSP main store to networking chip set support.

Controls

Addresses, data I/Os, chip enables ($\overline{E1}$, $\overline{E2}$, $\overline{E3}$), address burst control inputs ($\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$), and write control inputs ($\overline{Bx}$, $\overline{BW}$, $\overline{GW}$) are synchronous and are controlled by a positive-edge-triggered clock input ($\overline{CK}$). Output enable ($\overline{G}$) and power down control ($\overline{ZZ}$) are asynchronous inputs. Burst cycles can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ inputs. In Burst mode, subsequent burst addresses are generated internally and are controlled by $\overline{ADV}$. The burst address counter may be configured to count in either linear or interleave order

with the Linear Burst Order ($\overline{LBO}$) input. The Burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

Flow Through/Pipeline Reads

The function of the Data Output register can be controlled by the user via the $\overline{FT}$ mode pin (Pin 14). Holding the $\overline{FT}$ mode pin low places the RAM in Flow Through mode, causing output data to bypass the Data Output Register. Holding $\overline{FT}$ high places the RAM in Pipeline mode, activating the rising-edge-triggered Data Output Register.

DCD Pipelined Reads

The GS8160E18/32/36T is a DCD (Dual Cycle Deselect) pipelined synchronous SRAM. SCD (Single Cycle Deselect) versions are also available. DCD SRAMs pipeline disable commands to the same degree as read commands. DCD RAMs hold the deselect command for one full cycle and then begin turning off their outputs just after the second rising edge of clock.

Byte Write and Global Write

Byte write operation is performed by using Byte Write enable ($\overline{BW}$) input combined with one or more individual byte write signals ($\overline{Bx}$). In addition, Global Write ($\overline{GW}$) is available for writing all bytes at one time, regardless of the Byte Write control inputs.

Sleep Mode

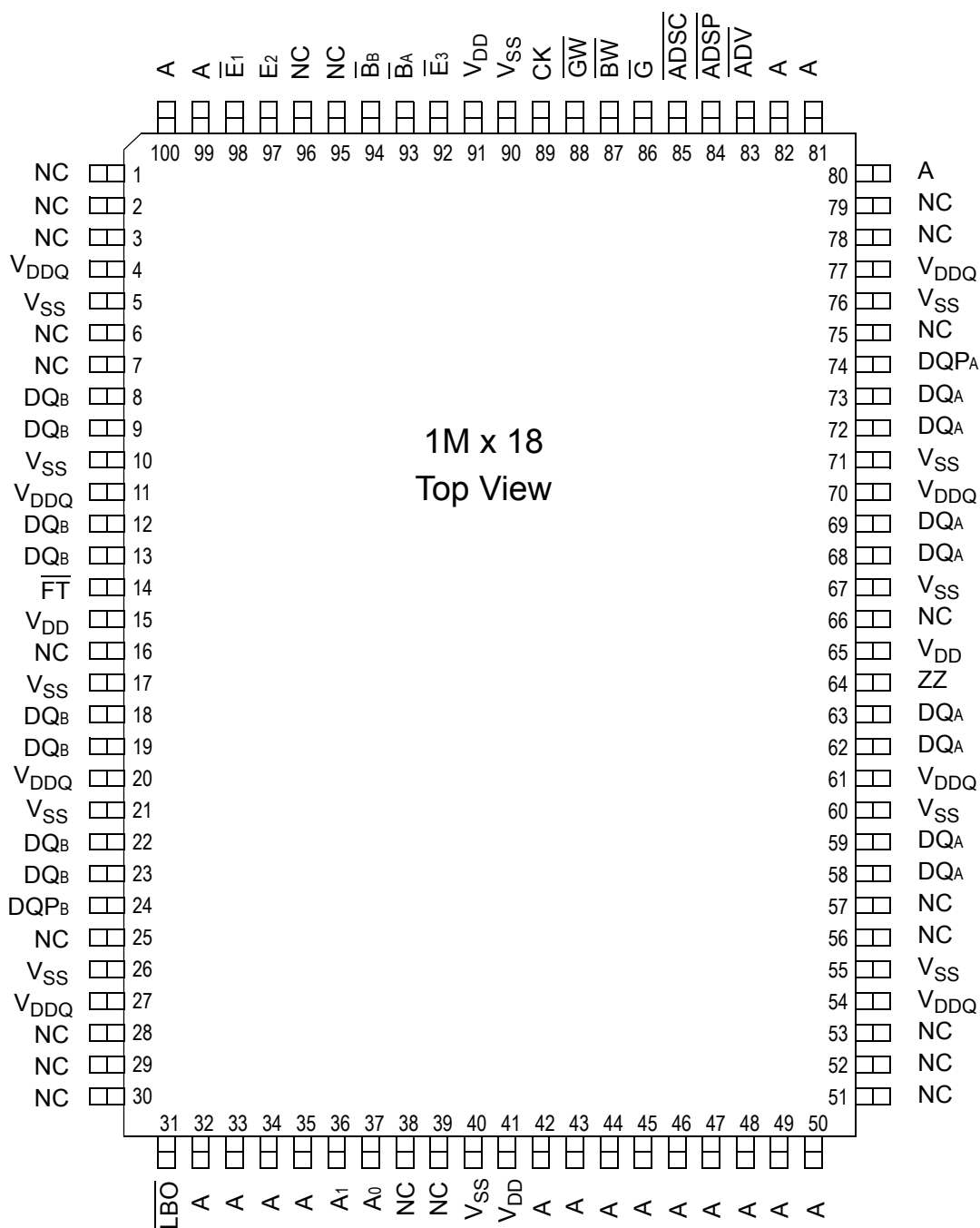
Low power (Sleep mode) is attained through the assertion (High) of the $\overline{ZZ}$ signal, or by stopping the clock ($\overline{CK}$). Memory data is retained during Sleep mode.

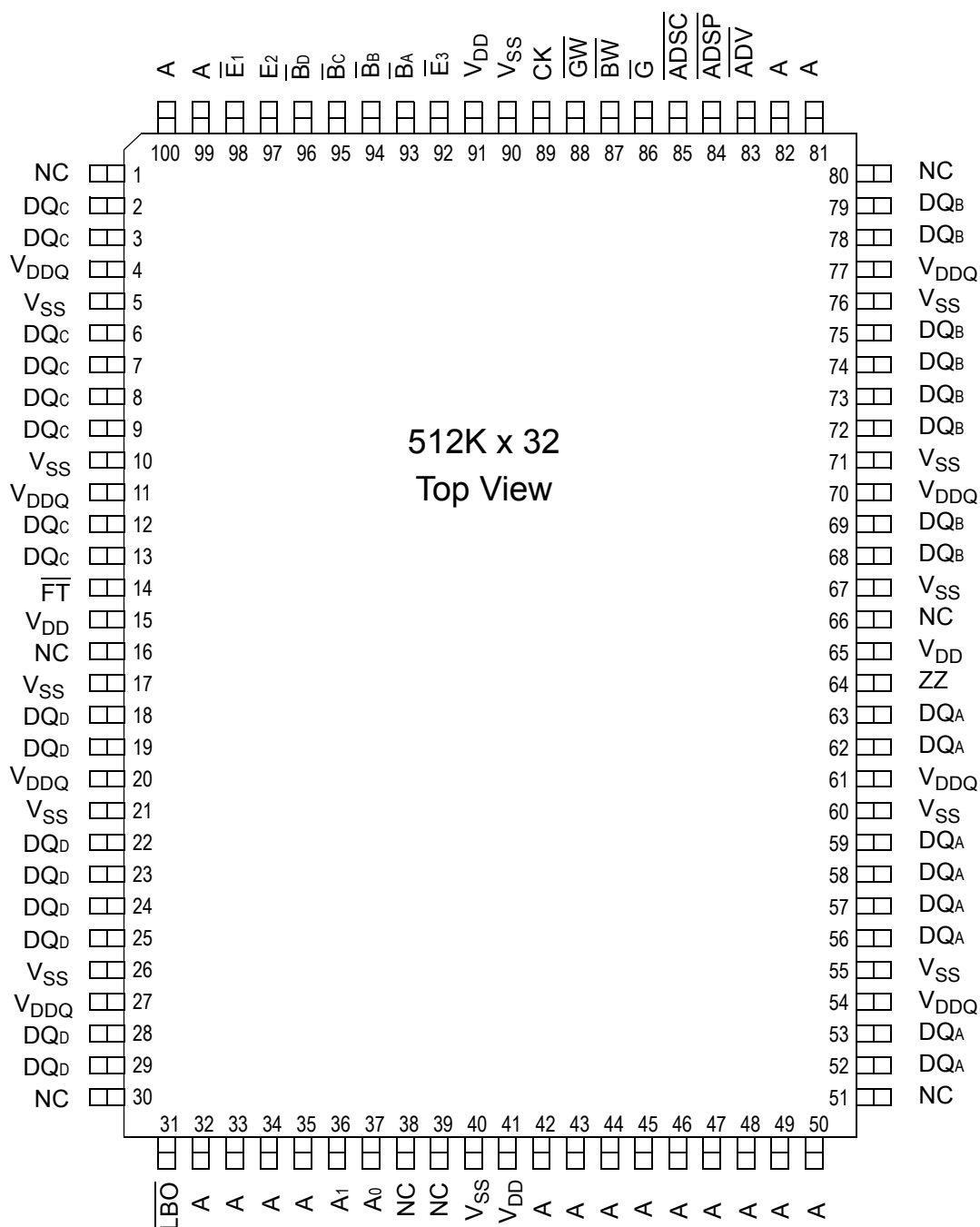
Core and Interface Voltages

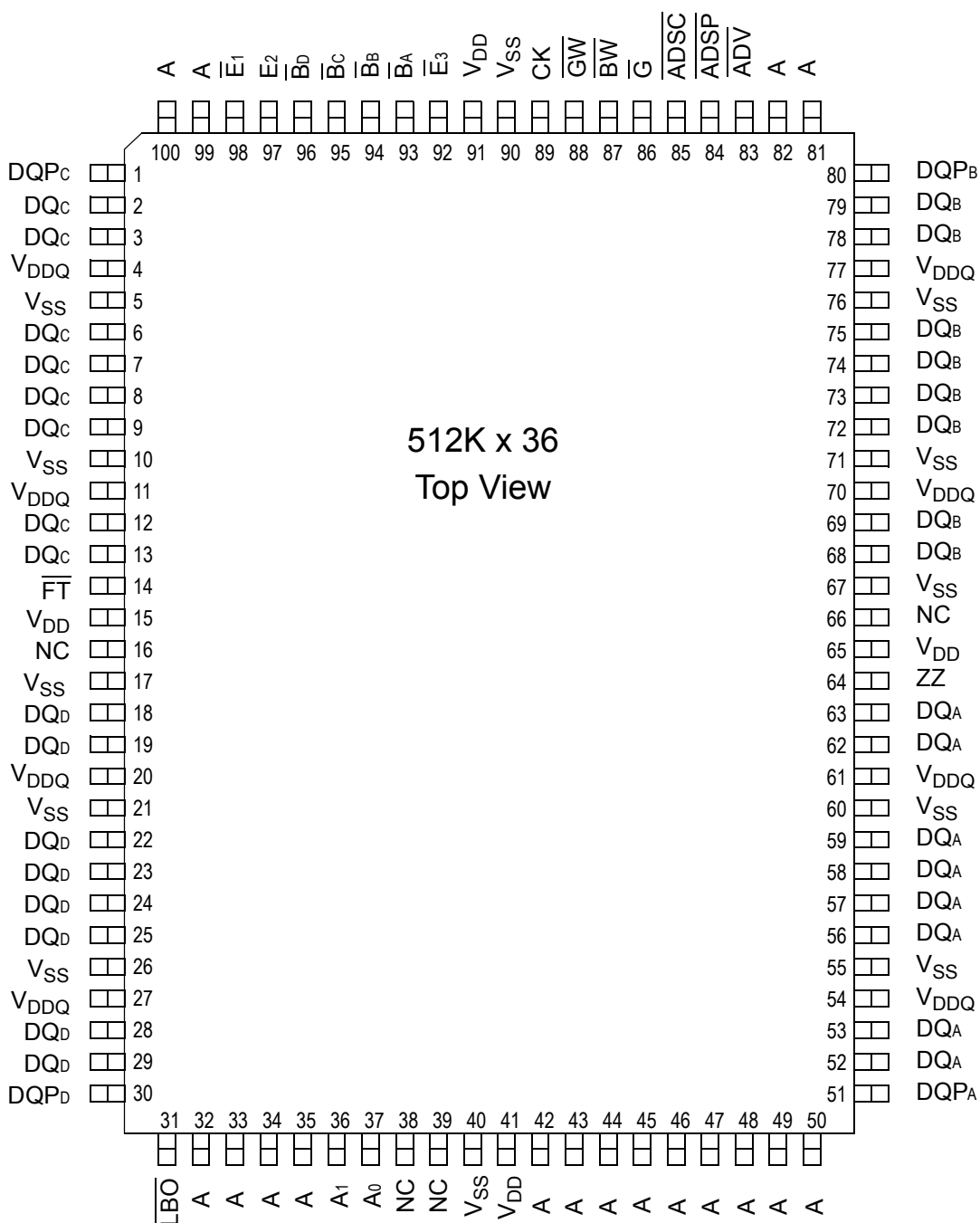
The GS8160E18/32/36T operates on a 2.5 V or 3.3 V power supply. All input are 3.3 V and 2.5 V compatible. Separate output power (V_{DDQ}) pins are used to decouple output noise from the internal circuits and are 3.3 V and 2.5 V compatible.

Parameter Synopsis

		-250	-225	-200	-166	-150	-133	Unit
Pipeline 3-1-1-1	t_{KQ}	2.5	2.7	3.0	3.4	3.8	4.0	ns
	t_{Cycle}	4.0	4.4	5.0	6.0	6.7	7.5	ns
3.3 V	Curr (x18)	280	255	230	200	185	165	mA
	Curr (x32/x36)	330	300	270	230	215	190	mA
2.5 V	Curr (x18)	275	250	230	195	180	165	mA
	Curr (x32/x36)	320	295	265	225	210	185	mA
Flow Through 2-1-1-1	t_{KQ}	5.5	6.0	6.5	7.0	7.5	8.5	ns
	t_{Cycle}	5.5	6.0	6.5	7.0	7.5	8.5	ns
3.3 V	Curr (x18)	175	165	160	150	145	135	mA
	Curr (x32/x36)	200	190	180	170	165	150	mA
2.5 V	Curr (x18)	175	165	160	150	145	135	mA
	Curr (x32/x36)	200	190	180	170	165	150	mA

GS8160E18 100-Pin TQFP Pinout (Package T)


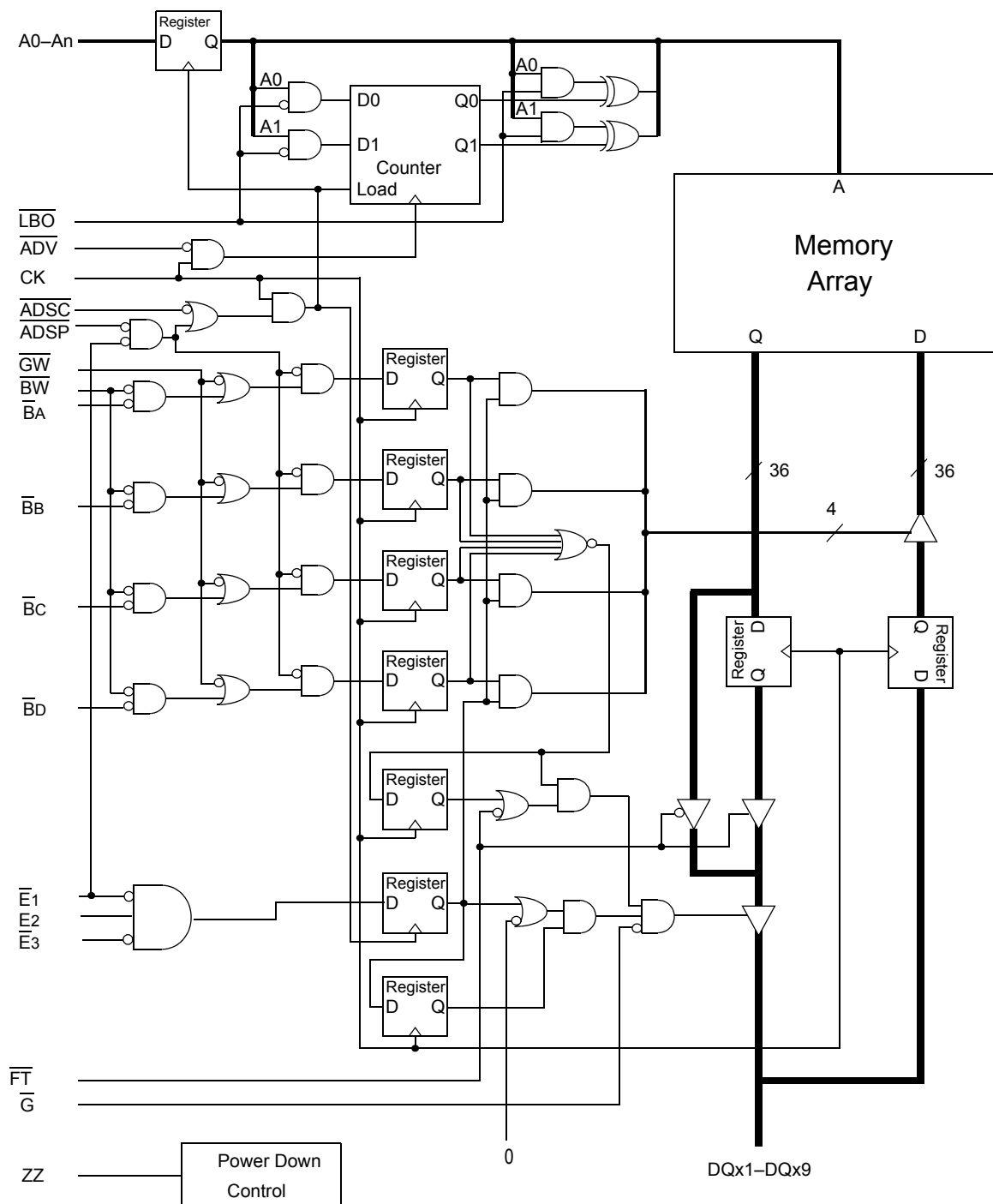
GS8160E32 100-Pin TQFP Pinout (Package T)


GS8160E36 100-Pin TQFP Pinout (Package T)


TQFP Pin Description

Symbol	Type	Description
A ₀ , A ₁	I	Address field LSBs and Address Counter preset Inputs
A	I	Address Input
DQ _A DQ _B DQ _C DQ _D	I/O	Data Input and Output pins
NC	—	No Connect
$\overline{\text{BW}}$	I	Byte Write—Writes all enabled bytes; active low
$\overline{\text{B}}_{\text{A}}$, $\overline{\text{B}}_{\text{B}}$, $\overline{\text{B}}_{\text{C}}$, $\overline{\text{B}}_{\text{D}}$	I	Byte Write Enable for DQ _A , DQ _B Data I/Os; active low
CK	I	Clock Input Signal; active high
$\overline{\text{GW}}$	I	Global Write Enable—Writes all bytes; active low
$\overline{\text{E}}_1$	I	Chip Enable; active low
E ₂	I	Chip Enable; active high
$\overline{\text{E}}_3$	I	Chip Enable; active low
$\overline{\text{G}}$	I	Output Enable; active low
ADV	I	Burst address counter advance enable; active low
$\overline{\text{ADSP}}$, $\overline{\text{ADSC}}$	I	Address Strobe (Processor, Cache Controller); active low
$\overline{\text{ZZ}}$	I	Sleep Mode control; active high
LBO	I	Linear Burst Order mode; active low
V _{DD}	I	Core power supply
V _{SS}	I	I/O and Core Ground
V _{DDQ}	I	Output driver power supply

GS8160E18/32/36 Block Diagram



Note: Only x36 version shown for simplicity.

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{\text{LBO}}$	L	Linear Burst
		H	Interleaved Burst
Output Register Control	$\overline{\text{FT}}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

Note:

There is a pull-up device on the $\overline{\text{FT}}$ pin and a pull-down device on the ZZ pin, so this input pin can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note:

The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note:

The burst counter wraps to initial state on the 5th clock.

BPR 1999.05.18

Byte Write Truth Table

Function	GW	BW	BA	BB	Bc	Bd	Notes
Read	H	H	X	X	X	X	1
Read	H	L	H	H	H	H	1
Write byte a	H	L	L	H	H	H	2, 3
Write byte b	H	L	H	L	H	H	2, 3
Write byte c	H	L	H	H	L	H	2, 3, 4
Write byte d	H	L	H	H	H	L	2, 3, 4
Write all bytes	H	L	L	L	L	L	2, 3, 4
Write all bytes	L	X	X	X	X	X	

Notes:

1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs.
2. Byte Write Enable inputs BA, BB, BC and/or BD may be used in any combination with BW to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes "C" and "D" are only available on the x32 and x36 versions.

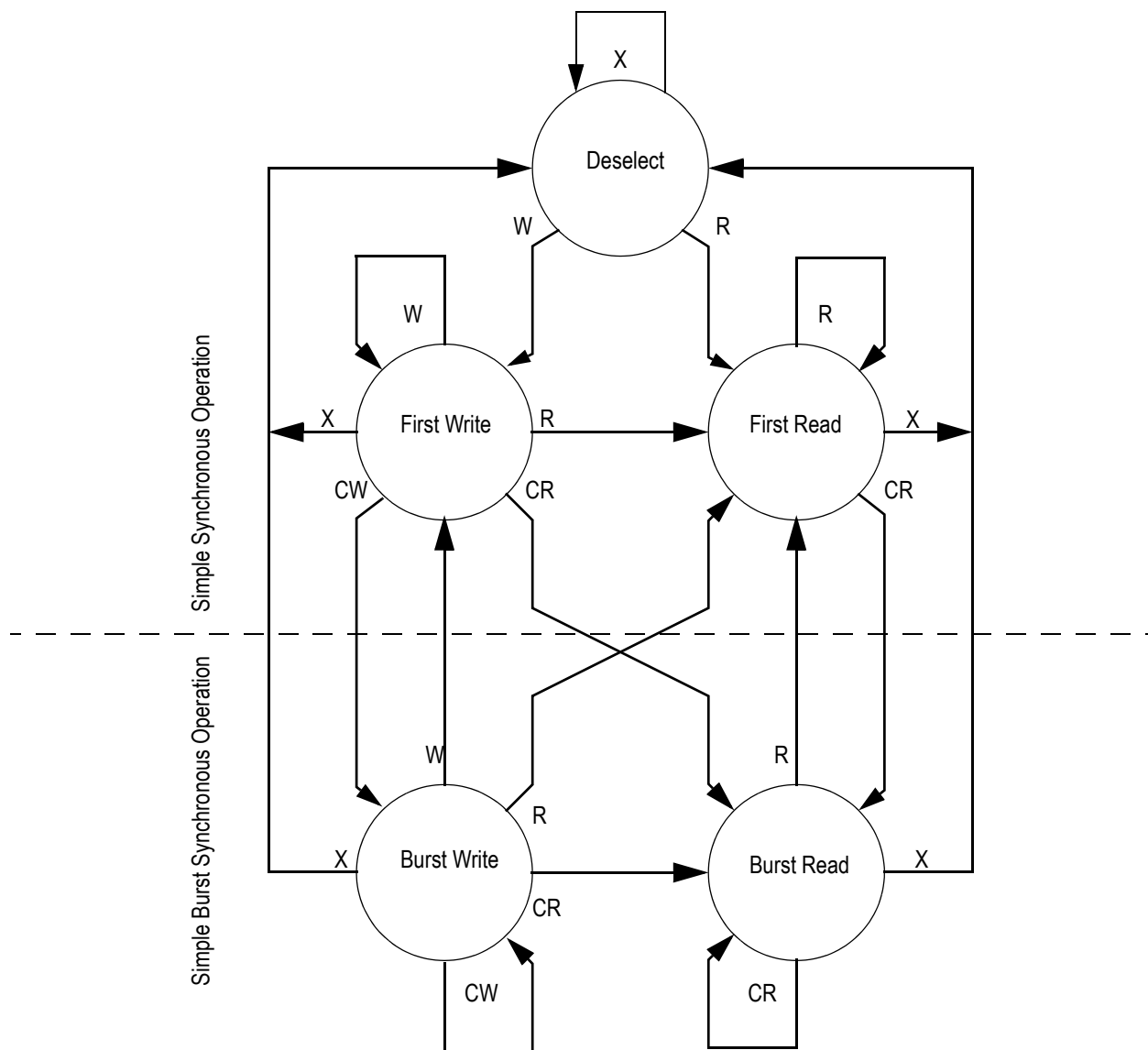
Synchronous Truth Table

Operation	Address Used	State Diagram Key ⁵	$\bar{E}_1$	E^2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\bar{W}^3$	DQ ⁴
Deselect Cycle, Power Down	None	X	H	X	X	L	X	X	High-Z
Deselect Cycle, Power Down	None	X	L	F	L	X	X	X	High-Z
Deselect Cycle, Power Down	None	X	L	F	H	L	X	X	High-Z
Read Cycle, Begin Burst	External	R	L	T	L	X	X	X	Q
Read Cycle, Begin Burst	External	R	L	T	H	L	X	F	Q
Write Cycle, Begin Burst	External	W	L	T	H	L	X	T	D
<i>Read Cycle, Continue Burst</i>	<i>Next</i>	<i>CR</i>	X	X	H	H	L	F	Q
Read Cycle, Continue Burst	Next	CR	H	X	X	H	L	F	Q
<i>Write Cycle, Continue Burst</i>	<i>Next</i>	<i>CW</i>	X	X	H	H	L	T	D
Write Cycle, Continue Burst	Next	CW	H	X	X	H	L	T	D
Read Cycle, Suspend Burst	Current		X	X	H	H	H	F	Q
Read Cycle, Suspend Burst	Current		H	X	X	H	H	F	Q
Write Cycle, Suspend Burst	Current		X	X	H	H	H	T	D
Write Cycle, Suspend Burst	Current		H	X	X	H	H	T	D

Notes:

1. X = Don't Care, H = High, L = Low
2. $E = T$ (True) if $E_2 = 1$ and $\bar{E}_3 = 0$; $E = F$ (False) if $E_2 = 0$ or $\bar{E}_3 = 1$
3. $W = T$ (True) and F (False) is defined in the Byte Write Truth Table preceding.
4. $\bar{G}$ is an asynchronous input. $\bar{G}$ can be driven high at any time to disable active output drivers. $\bar{G}$ low can only enable active drivers (shown as "Q" in the Truth Table above).
5. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
6. Tying $\overline{ADSP}$ high and $\overline{ADSC}$ low allows simple non-burst synchronous operations. See **BOLD** items above.
7. Tying $\overline{ADSP}$ high and $\overline{ADV}$ low while using $\overline{ADSC}$ to load new addresses allows simple burst operations. See *ITALIC* items above.

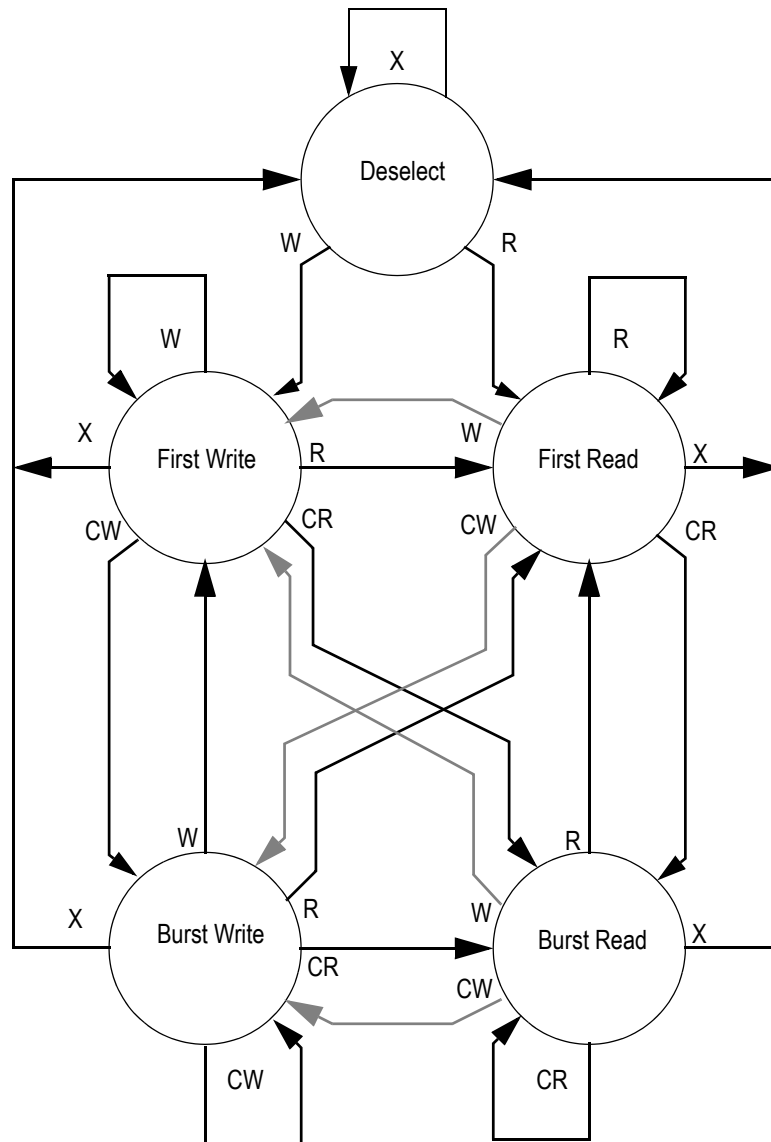
Simplified State Diagram



Notes:

1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes $\overline{G}$ is tied low.
2. The upper portion of the diagram assumes active use of only the Enable ($\overline{E1}$, $\overline{E2}$, and $\overline{E3}$) and Write ($\overline{BA}$, $\overline{BB}$, $\overline{BC}$, $\overline{BD}$, $\overline{BW}$, and $\overline{GW}$) control inputs, and that $\overline{ADSP}$ is tied high and $\overline{ADSC}$ is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write, and $\overline{ADSC}$ control inputs, and assumes $\overline{ADSP}$ is tied high and $\overline{ADV}$ is tied low.

Simplified State Diagram with $\overline{G}$



Notes:

1. The diagram shows supported (tested) synchronous state transitions plus supported transitions that depend upon the use of $\overline{G}$.
2. Use of "Dummy Reads" (Read Cycles with $\overline{G}$ High) may be used to make the transition from Read cycles to Write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal read cycles.
3. Transitions shown in gray tone assume $\overline{G}$ has been pulsed high long enough to turn the RAM's drivers off and for incoming data to meet Data Input Set Up Time.

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	-0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	-0.5 to 4.6	V
$V_{I/O}$	Voltage on I/O Pins	-0.5 to $V_{DDQ} + 0.5$ (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	-0.5 to $V_{DD} + 0.5$ (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/-20	mA
I_{OUT}	Output Current on Any I/O Pin	+/-20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	-55 to 125	°C
T_{BIAS}	Temperature Under Bias	-55 to 125	°C

Note:

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Power Supply Voltage Ranges

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
3.3 V Supply Voltage	V_{DD3}	3.0	3.3	3.6	V	
2.5 V Supply Voltage	V_{DD2}	2.3	2.5	2.7	V	
3.3 V V_{DDQ} I/O Supply Voltage	V_{DDQ3}	3.0	3.3	3.6	V	
2.5 V V_{DDQ} I/O Supply Voltage	V_{DDQ2}	2.3	2.5	2.7	V	

Notes:

- The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
- Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

V_{DDQ3} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
V _{DD} Input High Voltage	V _{IH}	2.0	—	V _{DD} + 0.3	V	1
V _{DD} Input Low Voltage	V _{IL}	−0.3	—	0.8	V	1
V _{DDQ} I/O Input High Voltage	V _{IHQ}	2.0	—	V _{DDQ} + 0.3	V	1,3
V _{DDQ} I/O Input Low Voltage	V _{ILQ}	−0.3	—	0.8	V	1,3

Notes:

1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% t_{KC}.
3. V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

V_{DDQ2} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
V _{DD} Input High Voltage	V _{IH}	0.6*V _{DD}	—	V _{DD} + 0.3	V	1
V _{DD} Input Low Voltage	V _{IL}	−0.3	—	0.3*V _{DD}	V	1
V _{DDQ} I/O Input High Voltage	V _{IHQ}	0.6*V _{DD}	—	V _{DDQ} + 0.3	V	1,3
V _{DDQ} I/O Input Low Voltage	V _{ILQ}	−0.3	—	0.3*V _{DD}	V	1,3

Notes:

1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% t_{KC}.
3. V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

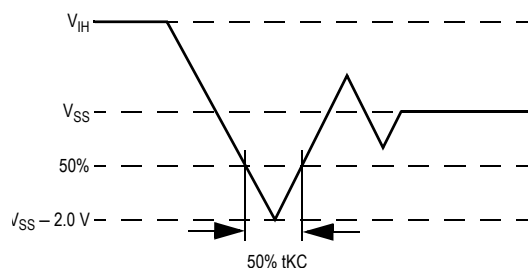
Recommended Operating Temperatures

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Temperature (Commercial Range Versions)	T _A	0	25	70	°C	2
Ambient Temperature (Industrial Range Versions)	T _A	−40	25	85	°C	2

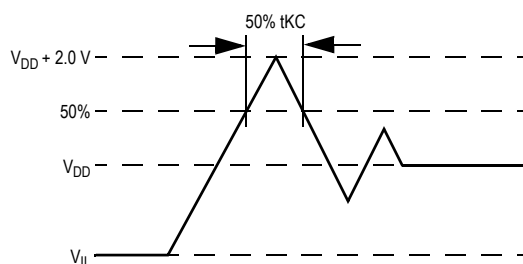
Notes:

1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% t_{KC}.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{DD} = 2.5\text{ V}$)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0\text{ V}$	4	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{OUT} = 0\text{ V}$	6	7	pF

Note:

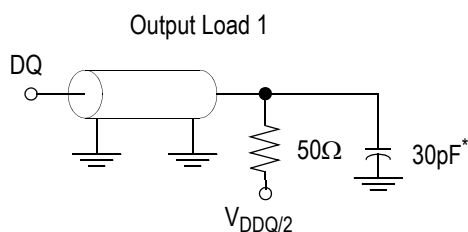
These parameters are sample tested.

AC Test Conditions

Parameter	Conditions
Input high level	$V_{DD} - 0.2\text{ V}$
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	$V_{DD}/2$
Output reference level	$V_{DDQ}/2$
Output load	Fig. 1

Notes:

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Device is deselected as defined by the Truth Table.



* Distributed Test Jig Capacitance

DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	$V_{IN} = 0 \text{ to } V_{DD}$	-1 μA	1 μA
ZZ Input Current	I_{IN1}	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0 \text{ V} \leq V_{IN} \leq V_{IH}$	-1 μA -1 μA	1 μA 100 μA
$\overline{FT}$ Input Current	I_{IN2}	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0 \text{ V} \leq V_{IN} \leq V_{IL}$	-100 μA -1 μA	1 μA 1 μA
Output Leakage Current	I_{OL}	Output Disable, $V_{OUT} = 0 \text{ to } V_{DD}$	-1 μA	1 μA
Output High Voltage	V_{OH2}	$I_{OH} = -8 \text{ mA}$, $V_{DDQ} = 2.375 \text{ V}$	1.7 V	—
Output High Voltage	V_{OH3}	$I_{OH} = -8 \text{ mA}$, $V_{DDQ} = 3.135 \text{ V}$	2.4 V	—
Output Low Voltage	V_{OL}	$I_{OL} = 8 \text{ mA}$	—	0.4 V

Operating Currents

Parameter	Test Conditions	Mode	Symbol	-250		-225		-200		-166		-150		-133		Unit
				0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	
Operating Current 3.3 V	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	(x32/ x36)	Pipeline	290	300	265	275	240	250	205	215	190	200	170	180	mA
			I _{DDQ}	40	40	35	35	30	30	25	25	25	25	20	20	
		(x18)	Flow Through	180	190	170	180	165	175	155	165	150	160	140	150	mA
			I _{DDQ}	20	20	20	20	15	15	15	15	15	15	10	10	
Operating Current 2.5 V	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	(x18)	Pipeline	260	270	235	245	215	225	185	195	170	180	155	165	mA
			I _{DDQ}	20	20	20	20	15	15	15	15	15	15	10	10	
		(x32/ x36)	Flow Through	165	175	155	165	150	160	140	150	135	145	125	135	mA
			I _{DDQ}	10	10	10	10	10	10	10	10	10	10	10	10	
Standby Current	ZZ $\geq V_{DD} - 0.2$ V	(x18)	Pipeline	260	270	235	245	215	225	185	195	170	180	155	165	mA
			I _{DDQ}	15	15	15	15	15	15	10	10	10	10	10	10	
		(x32/ x36)	Flow Through	165	175	155	165	150	160	140	150	135	145	125	135	mA
			I _{DDQ}	10	10	10	10	10	10	10	10	10	10	10	10	
Deselect Current	Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$	(x18)	Pipeline	20	30	20	30	20	30	20	30	20	30	20	30	mA
			I _{SB}													
		(x32/ x36)	Flow Through	20	30	20	30	20	30	20	30	20	30	20	30	mA
			I _{SB}													
Deselect Current	Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$	(x18)	Pipeline	85	90	80	85	75	80	64	70	60	65	50	55	mA
			I _{DD}													
		(x32/ x36)	Flow Through	60	65	60	65	50	55	50	55	50	55	45	50	mA
			I _{DD}													

Notes:

1. I_{DD} and I_{DDQ} apply to any combination of V_{DD3}, V_{DD2}, V_{DDQ3}, and V_{DDQ2} operation.
2. All parameters listed are worst case scenario.

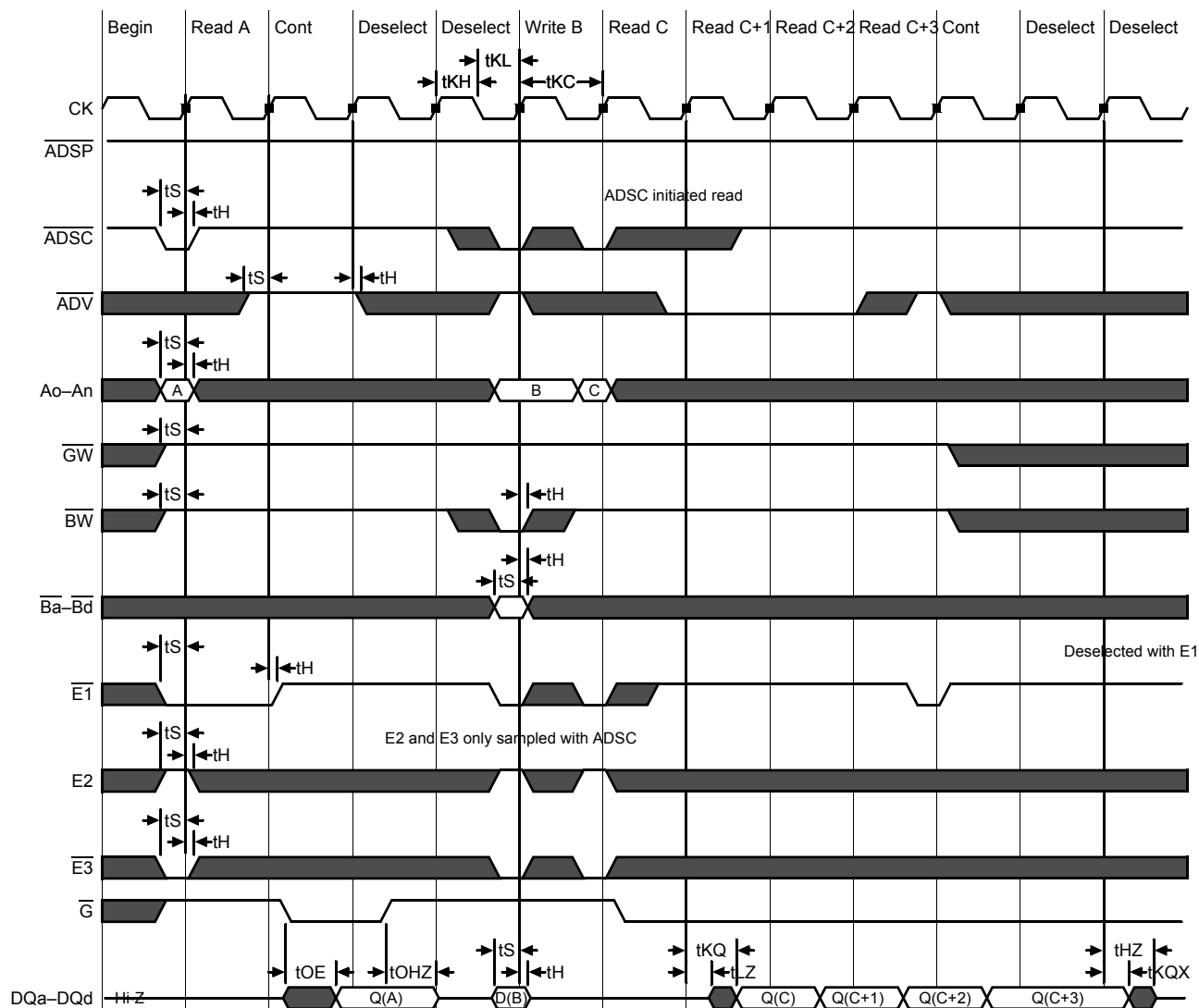
AC Electrical Characteristics

	Parameter	Symbol	-250		-225		-200		-166		-150		-133		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	t _{KC}	4.0	—	4.4	—	5.0	—	6.0	—	6.7	—	7.5	—	ns
	Clock to Output Valid	t _{KQ}	—	2.5	—	2.7	—	3.0	—	3.4	—	3.8	—	4.0	ns
	Clock to Output Invalid	t _{KQX}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	t _{LZ} ¹	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Setup time	t _S	1.2	—	1.3	—	1.4	—	1.5	—	1.5	—	1.5	—	ns
	Hold time	t _H	0.2	—	0.3	—	0.4	—	0.5	—	0.5	—	0.5	—	ns
Flow Through	Clock Cycle Time	t _{KC}	5.5	—	6.0	—	6.5	—	7.0	—	7.5	—	8.5	—	ns
	Clock to Output Valid	t _{KQ}	—	5.5	—	6.0	—	6.5	—	7.0	—	7.5	—	8.5	ns
	Clock to Output Invalid	t _{KQX}	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock to Output in Low-Z	t _{LZ} ¹	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Setup time	t _S	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Hold time	t _H	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
	Clock HIGH Time	t _{KH}	1.3	—	1.3	—	1.3	—	1.3	—	1.5	—	1.7	—	ns
	Clock LOW Time	t _{KL}	1.5	—	1.5	—	1.5	—	1.5	—	1.7	—	2	—	ns
	Clock to Output in High-Z	t _{HZ} ¹	1.5	2.3	1.5	2.5	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	ns
	$\overline{G}$ to Output Valid	t _{OE}	—	2.3	—	2.5	—	3.2	—	3.5	—	3.8	—	4.0	ns
	$\overline{G}$ to output in Low-Z	t _{OLZ} ¹	0	—	0	—	0	—	0	—	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	t _{OHZ} ¹	—	2.3	—	2.5	—	3.0	—	3.0	—	3.0	—	3.0	ns
	ZZ setup time	t _{ZZS} ²	5	—	5	—	5	—	5	—	5	—	5	—	ns
	ZZ hold time	t _{ZZH} ²	1	—	1	—	1	—	1	—	1	—	1	—	ns
	ZZ recovery	t _{ZZR}	20	—	20	—	20	—	20	—	20	—	20	—	ns

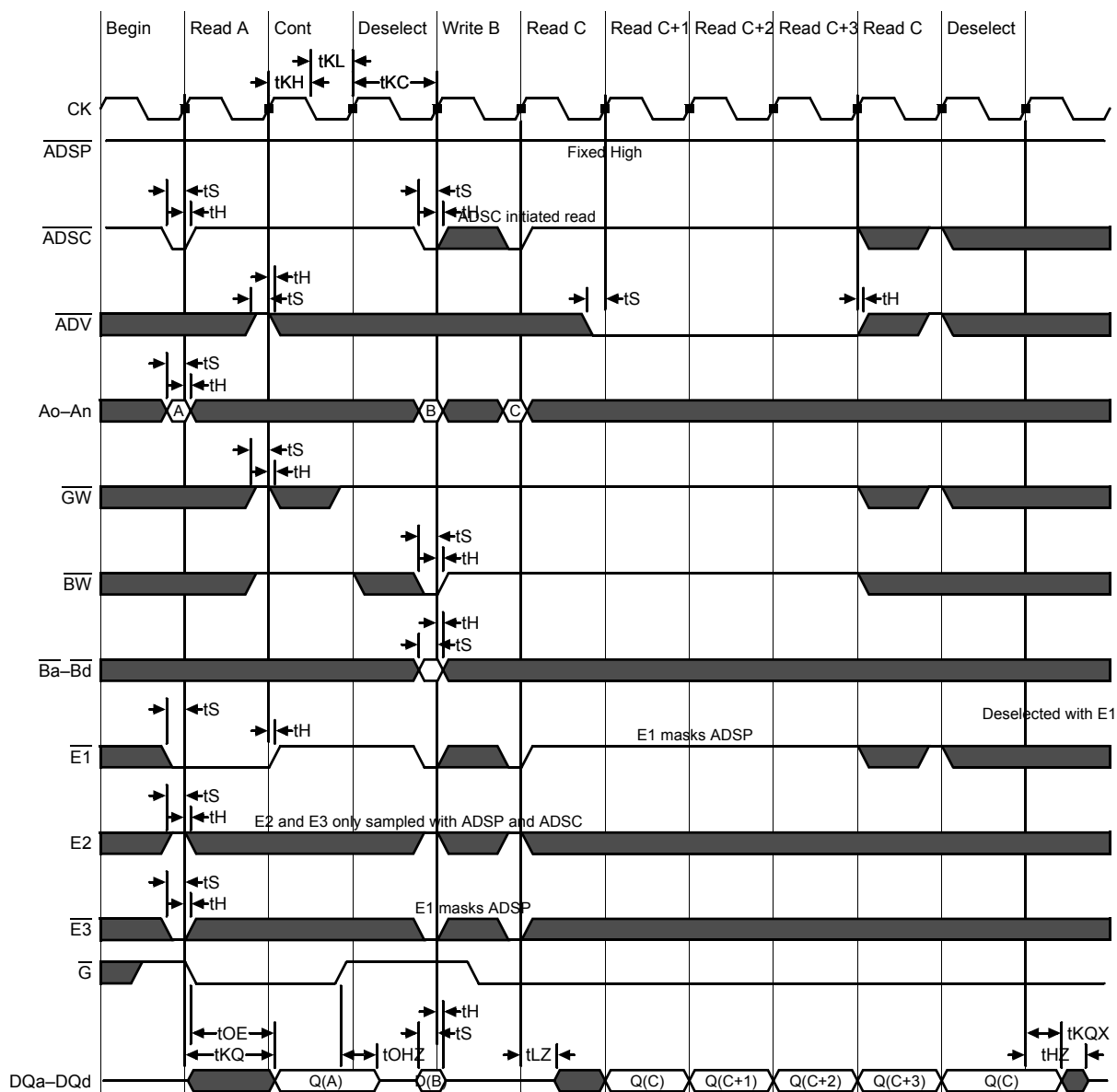
Notes:

1. These parameters are sampled and are not 100% tested.
2. ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

Pipeline Mode Timing



Flow Through Mode Timing

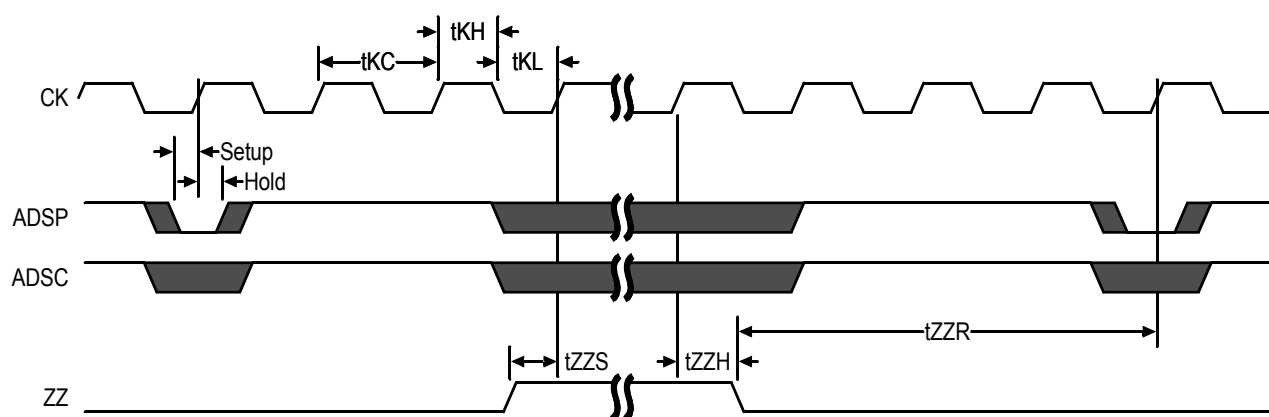


Sleep Mode

During normal operation, ZZ must be pulled low, either by the user or by its internal pull down resistor. When ZZ is pulled high, the SRAM will enter a Power Sleep mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates normally after ZZ recovery time.

Sleep mode is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2} . The duration of Sleep mode is dictated by the length of time the ZZ is in a High state. After entering Sleep mode, all inputs except ZZ become disabled and all outputs go to High-Z. The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep mode. When the ZZ pin is driven high, I_{SB2} is guaranteed after the time t_{ZZI} is met. Because ZZ is an asynchronous input, pending operations or operations in progress may not be properly completed if ZZ is asserted. Therefore, Sleep mode must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep mode during t_{ZZR} , only a Deselect or Read commands may be applied while the SRAM is recovering from Sleep mode.

Sleep Mode Timing Diagram



Application Tips

Single and Dual Cycle Deselect

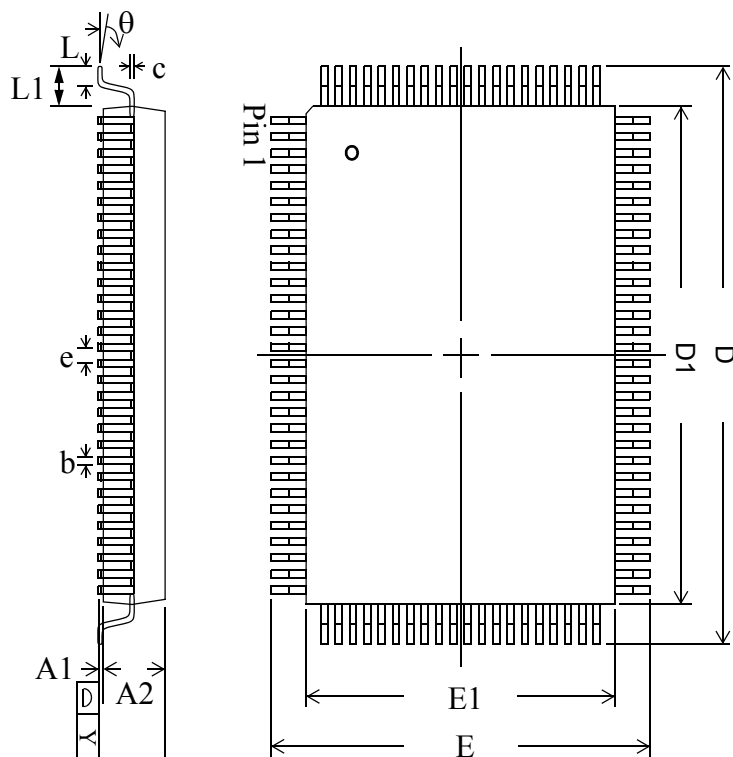
SCD devices force the use of “dummy read cycles” (read cycles that are launched normally, but that are ended with the output drivers inactive) in a fully synchronous environment. Dummy read cycles waste performance, but their use usually assures there will be no bus contention in transitions from reads to writes or between banks of RAMs. DCD SRAMs (like this one) do not waste bandwidth on dummy cycles and are logically simpler to manage in a multiple bank application (wait states need not be inserted at bank address boundary crossings), but greater care must be exercised to avoid excessive bus contention.

TQFP Package Drawing (Package T)

Symbol	Description	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15
A2	Body Thickness	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40
c	Lead Thickness	0.09	—	0.20
D	Terminal Dimension	21.9	22.0	22.1
D1	Package Body	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1
e	Lead Pitch	—	0.65	—
L	Foot Length	0.45	0.60	0.75
L1	Lead Length	—	1.00	—
Y	Coplanarity			0.10
θ	Lead Angle	0°	—	7°

Notes:

1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.



Ordering Information for GSI Synchronous Burst RAMs

Org	Part Number ¹	Type	Package	Speed ² (MHz/ns)	T _A ³	Status
1M x 18	GS8160E18T-250	DCD Pipeline/Flow Through	TQFP	250/5.5	C	
1M x 18	GS8160E18T-225	DCD Pipeline/Flow Through	TQFP	225/6	C	
1M x 18	GS8160E18T-200	DCD Pipeline/Flow Through	TQFP	200/6.5	C	
1M x 18	GS8160E18T-166	DCD Pipeline/Flow Through	TQFP	166/7	C	
1M x 18	GS8160E18T-150	DCD Pipeline/Flow Through	TQFP	150/7.5	C	
1M x 18	GS8160E18T-133	DCD Pipeline/Flow Through	TQFP	133/8.5	C	
512K x 32	GS8160E32T-250	DCD Pipeline/Flow Through	TQFP	250/5.5	C	
512K x 32	GS8160E32T-225	DCD Pipeline/Flow Through	TQFP	225/6	C	
512K x 32	GS8160E32T-200	DCD Pipeline/Flow Through	TQFP	200/6.5	C	
512K x 32	GS8160E32T-166	DCD Pipeline/Flow Through	TQFP	166/7	C	
512K x 32	GS8160E32T-150	DCD Pipeline/Flow Through	TQFP	150/7.5	C	
512K x 32	GS8160E32T-133	DCD Pipeline/Flow Through	TQFP	133/8.5	C	
512K x 36	GS8160E36T-250	DCD Pipeline/Flow Through	TQFP	250/5.5	C	
512K x 36	GS8160E36T-225	DCD Pipeline/Flow Through	TQFP	225/6	C	
512K x 36	GS8160E36T-200	DCD Pipeline/Flow Through	TQFP	200/6.5	C	
512K x 36	GS8160E36T-166	DCD Pipeline/Flow Through	TQFP	166/7	C	
512K x 36	GS8160E36T-150	DCD Pipeline/Flow Through	TQFP	150/7.5	C	
512K x 36	GS8160E36T-133	DCD Pipeline/Flow Through	TQFP	133/8.5	C	
1M x 18	GS8160E18T-250I	DCD Pipeline/Flow Through	TQFP	250/5.5	I	
1M x 18	GS8160E18T-225I	DCD Pipeline/Flow Through	TQFP	225/6	I	
1M x 18	GS8160E18T-200I	DCD Pipeline/Flow Through	TQFP	200/6.5	I	
1M x 18	GS8160E18T-166I	DCD Pipeline/Flow Through	TQFP	166/7	I	
1M x 18	GS8160E18T-150I	DCD Pipeline/Flow Through	TQFP	150/7.5	I	
1M x 18	GS8160E18T-133I	DCD Pipeline/Flow Through	TQFP	133/8.5	I	
512K x 32	GS8160E32T-250I	DCD Pipeline/Flow Through	TQFP	250/5.5	I	
512K x 32	GS8160E32T-225I	DCD Pipeline/Flow Through	TQFP	225/6	I	

Notes:

- Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS8160E18T-150IT.
- The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow through mode-selectable by the user.
- T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
- GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsistechnology.com) for a complete listing of current offerings.

Ordering Information for GSI Synchronous Burst RAMs

Org	Part Number ¹	Type	Package	Speed ² (MHz/ns)	T _A ³	Status
512K x 32	GS8160E32T-200I	DCD Pipeline/Flow Through	TQFP	200/6.5	I	
512K x 32	GS8160E32T-166I	DCD Pipeline/Flow Through	TQFP	166/7	I	
512K x 32	GS8160E32T-150I	DCD Pipeline/Flow Through	TQFP	150/7.5	I	
512K x 32	GS8160E32T-133I	DCD Pipeline/Flow Through	TQFP	133/8.5	I	
512K x 36	GS8160E36T-250I	DCD Pipeline/Flow Through	TQFP	250/5.5	I	
512K x 36	GS8160E36T-225I	DCD Pipeline/Flow Through	TQFP	225/6	I	
512K x 36	GS8160E36T-200I	DCD Pipeline/Flow Through	TQFP	200/6.5	I	
512K x 36	GS8160E36T-166I	DCD Pipeline/Flow Through	TQFP	166/7	I	
512K x 36	GS8160E36T-150I	DCD Pipeline/Flow Through	TQFP	150/7.5	I	
512K x 36	GS8160E36T-133I	DCD Pipeline/Flow Through	TQFP	133/8.5	I	

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18Mb Sync SRAM Datasheet Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
GS8160E18T-150IT 1.00 9/ 1999A;GS8160E18T-150IT 2.00 1/1999B	Content	• Converted from 0.25u 3.3V process to 0.18u 2.5V process. Master File Rev B • Added x72 Pinout. • Added GSI Logo.
GS8160E18T- 2.00 11/ 1999B;GS8160E18T 2.01 1/ 2000C	Format	• Changed Flow-Through Read-Write cycle Timing Diagram for accuracy
GS8160E18T 2.01 1/ 2000C;GS8160E18 T 2.02 1/ 2000D		• Changed pin description in TQFP to match order of pins in pinout.
GS18/362.0 1/2000DGS18/ 362.03 2/2000E		• Front page; Features - changed 2.5V I/O supply to 2.5V or 3.3V I/O supply; Core and Interface voltages - Changed paragraph to include information for 3.3V;Completeness • Absolute Maximum Ratings; Changed VDDQ - Value: From: -.05 to VDD : to : -.05 to 3.6; Completeness. • Recommended Operating Conditions;Changed: I/O Supply Voltage- Max. from VDD to 3.6; Input High Voltage- Max. from VDD +0.3 to 3.6; Same page - took out Note 1;Completeness • Electrical Characteristics - Added second Output High Voltage line to table; completeness. • Note: There was not a Rev 2.02 for the 8160Z or the 8161Z.
GS18/362.03 2/2000E; 8160E18_r2_04	Content	• Changed the value of ZZ recovery in the AC Electrical Characteristics table on page 15 from 20 ns to 100 ns
8160E18_r2_04; 8160E18_r2_05	Content/Format	• Added 225 MHz speed bin • Updated Pg. 1 table, AC Characteristics table, and Operating Currents table to match 815xxx • Updated format to comply with Technical Publications standards
8160E18_r2_05; 8160E18_r2_06	Content	• Updated Capacitance table—removed Input row and changed Output row to I/O
8160E18_r2_06; 8160E18_r2_07	Content	• Updated Features list on page 1 • Completely reworked table on page 1 • Updated Mode Pin Functions table on page 7
8160E18_r2_07; 8160E18_r2_08	Content	• Added 3.3 V references to entire document • Updated Operating Conditions table • Added Pin 56 to Pin Description table • Updated Operating Currents table and added note • Updated Application Tips paragraph • Updated table on page 1; added power numbers

18Mb Sync SRAM Datasheet Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
8160E18_r2_08; 8160E18_r2_09	Content	• Updated Operating Currents table • Updated table on page 1; updated power numbers • Updated Recommended Operating Conditions table (added V_{DDQ} references)
8160E18_r2_09; 8160E18_r2_10	Content	• Updated table on page 1 • Created recommended operating conditions tables on pages 12 and 13 • Updated AC Electrical Characteristics table • Added Sleep mode description on page 23 • Updated Ordering Information for 225 MHz part (changed from 7ns to 6.5 ns) • Added 250 MHz speed bin • Deleted 180 MHz speed bin
8160E18_r2_10; 8160E18_r2_11	Content	• Updated AC Characteristics table • Updated FT power numbers • Updated ZZ recovery time diagram • Updated Mb references from 16Mb to 18Mb • Updated AC Test Conditions table and removed Output Load 2 diagram
8160E18_r2_11; 8160E18_r2_12	Content	• Removed pin locations from pin description table • Removed Preliminary banner
8160E18_r2_12; 8160E18_r2_13	Format/Content	• Updated format • Updated timing diagrams