SERIES 2+ FLASH MEMORY CARDS

4-, 8-, 20- AND 40 MEGABYTES

iMC004FLSP, iMC008FLSP, iMC020FLSP, iMC040FLSP

- **Single Power Supply**
- **Automatically Reconfigures for 3.3 V and 5 V Systems**
- **150 ns Maximum Access Time with 5 V Power Supply**
- **250 ns Maximum Access Time with 3.3 V Power Supply**
- **High-Performance Random Writes**
  - **0.85 MB/S Sustained Throughput**
  - **1 KB Burst Write at 10 MB/S**
- **25 µA Typical Deep Power-Down**
- **Revolutionary Architecture**
  - **Pipelined Command Execution**
  - **Write during Erase**
  - **Series 2 Command Super-Set**
- **State-of-the-Art 0.6 µm ETOX™ IV Flash Technology**
- **1 Million Erase Cycles per Block**
- **Up to 640 Independent Lockable Blocks**
- **PCMCIA 2.1/JEIDA 4.1-Compatible**
- **PCMCIA Type 1 Form Factor**
- **Series 2+ User's Manual**

Intel's Series 2+ Flash Memory Card sets the new record for high-performance disk emulation and eXecute-In-Place (XIP) applications in mobile PCs and dedicated equipment. Manufactured with Intel's 28F016SA 16-Mbit (DD28F032SA 32-Mbit) FlashFile™ memory, this card takes advantage of a revolutionary architecture that provides innovative capabilities, low-power operation and very high read/write performance.

The Series 2+ card provides today's highest density, highest performance nonvolatile read/write solution for solid-state storage applications. These applications are enhanced further with this product's symmetrically-blocked architecture, extended MTBF, low-power 3.3 V operation, built-in V_{PP} generator, and multiple block locking methods. The Series 2+ card's dual read and write voltages allow interchange between 3.3 V and 5.0 V systems.

December 1997

Order Number: 290491-007

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REVISION HISTORY

Number	Description
-001	Original Version
-002	Page Buffer Write to Flash Command Code correction (from 08H to 0CH) Series 2+ Tuples and AC Characteristics Tables include support for 150 ns access
-003	TTL DC Characteristics tables added General DC Characteristics table changed to reflect TTL levels
-004	AC Characteristics condensed to include V_{PP} pump information
005	Series 2+ 8-Meg and 40-Meg Cards added to datasheet Component Management Register tables reformatted I_{CCR} values increased for CMOS and TTL 3.3 V timings updated to 250 ns.
-006	Changed I_{PPSL} and I_{PPS} Max values
-007	Changed CMOS Interfacing DC Characteristics to increase V_{CC} Sleep Current

1.0 SCOPE OF DOCUMENT

The documentation for Intel's Series 2+ Flash Memory Card includes this datasheet and the *Series 2+ Flash Memory Card User's Manual* (297373). The datasheet provides all AC and DC characteristics (including timing waveforms) and a convenient reference for the device command set and the card's integrated registers (including the 28F016SA's status registers). The *Series 2+ Memory Card User's Manual* provides a complete description of the methods for using the card. It also contains the full list of software algorithms and flowcharts and a section for upgrading Intel's Series 2 Flash Memory Cards designs.

2.0 PRODUCT OVERVIEW

The 4-, 8-, and 20-Mbyte Series 2+ Flash Memory Cards each contain a flash memory array that consists of two, four, and ten 28F016SA TSOP memory devices, respectively. Each 28F016SA contains 32 distinct, individually-erasable, 64-Kbyte blocks. Therefore, the 4-, 8-, and 20-Mbyte cards contain 64, 128 and 320 independantly lockable blocks, respectively.

The 40-Mbyte Series 2+ Flash Memory Cards contain a flash memory array that consists of ten DD28F032SA TSOP memory devices. Each DD28F032SA contains two 28F016SA die in a single package, resulting in 64 distinct, individually-erasable, 64-Kbyte blocks. The 40-Mbyte cards have 640 independently lockable blocks.

The Series 2+ Card offers additional product features to those of the Series 2 Card family (refer to the iMC0XXFLSA datasheets). Some of the more notable card-level enhancements include: interchangeable operation at 3.3 V or 5.0 V, block locking and internal V_{PP} generation.

The Series 2+ card incorporates V_{CC} detect circuitry, referred to as SmartPower, to sense the voltage level present at the card interface. The card's control logic automatically configures its circuitry and the 28F016SA/DD28F032SA memory array accordingly. The Card Information Structure (CIS) reports that the card is 3.3 V or 5.0 V compatible. The card also detects the presence of 12.0 V on the V_{PP} pin and passes this supply to each memory device. When the 12.0 V power supply is unavailable, the card can generate the required V_{PP} via its internal V_{PP} generation circuitry, whether V_{CC} is 3.3 V or 5.0 V.

At the device level, internal algorithm automation allows write and erase operations to be executed using a two-write command sequence in the same way as the 28F008SA FlashFile memory in the Series 2 Card. A super-set of commands and additional performance enhancements have been added to the basic 28F008SA command set:

- Page Buffer Write to Flash results in writes up to four times faster than Series 2 Cards.
- Command Queueing permits the devices to receive new commands during the execution of the current command set.
- Automatic data writes during erase allows the 28F016SA to perform write operations to one block of memory while performing an erase on another block.
- Software locking of memory blocks provides a means to selectively protect code or data within the card.
- Erase all unlocked blocks provides a quick and simple method to sequentially erase all the blocks within a 28F016SA memory device.

The Series 2+ Card has two ways to put the flash devices into a sleep mode for reduced power consumption:

1. Issue a command to individual devices, referred to as the software-controlled sleep mode. The device will retain status register data contents and finish any operation in progress using this approach.
2. Write to the card's PCMCIA-compatible configuration and status register to activate a reset power-down to all devices simultaneously.

The card achieves its PCMCIA-compatible word-wide access by pairing the 28F016SA/ DD28F032SA devices resulting in an accessible memory block size of 64 Kwords. The card's decoding logic (contained within the ASICs) allows the system to write or read one word at a time, or one byte at a time by referencing the high or low byte. Erasure can be performed on the entire block pair (high and low byte simultaneously) or on the high and low portions separately. Although the 28F016SA/DD28F032SA support byte or word-wide data access, the byte interface was utilized within the card to allow the delivery of higher

performance benefits, such as doubling the effective page buffer size and write performance.

The Series 2+ Card's ASICs also contain the component management registers that provide five control functions: ready-busy mode selection, software write protection, card status, voltage control, and soft reset.

The memory card interface supports the Personal Computer Memory Card Industry Association (PCMCIA 2.10) and Japanese Electronics Industry Development Association (JEIDA 4.1) 68-pin card format. The Series 2+ Flash Card meets all PCMCIA/JEIDA Type 1 mechanical specifications.

3.0 SERIES 2+ ARCHITECTURE OVERVIEW

The Series 2+ Card consists of three major functional elements—the flash memory array, card control and SmartPower circuitry. The card control logic handles the interface between the flash memory array and the host system's PCMCIA signals. SmartPower circuitry provides the card's integrated V_{PP} generator and a means for detecting the socket's voltage levels.

3.1 Card Signal Description

The 68-pin PCMCIA format provides the system interface for the Series 2+ Flash Memory Card (see Tables 1 and 2). The detailed specifications for this interface is described in the PCMCIA *2.10 Standard Specification*. The Series 2+ Flash Card product family conforms to the requirements of previous PCMCIA Versions Release 1.0, Release 2.0 and Release 2.01 of the *PC Card Standard*. Release 2.10 redefined pins 43 and 57 as VS_1 and VS_2 (previously REFRESH and RFU, respectively).

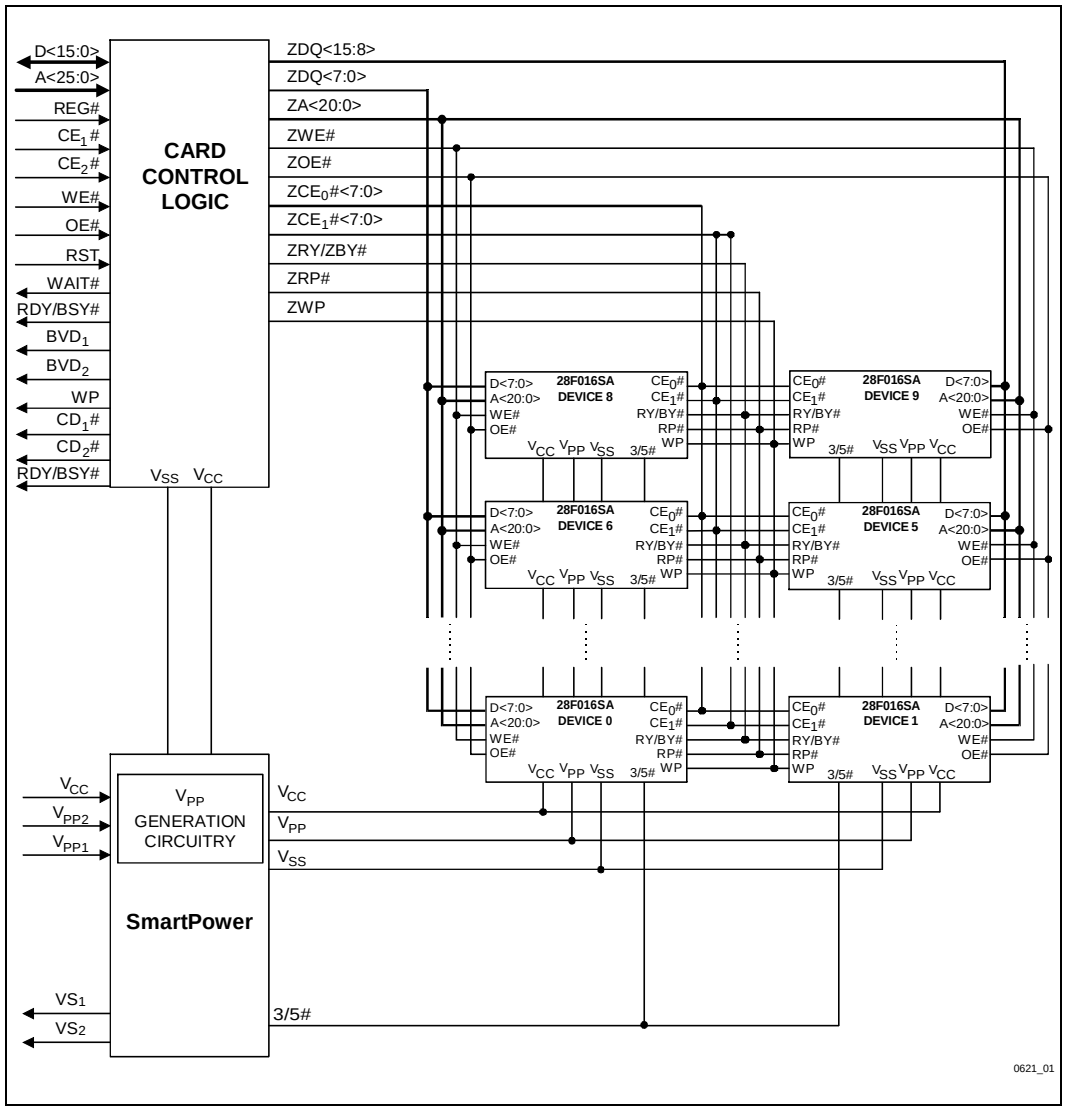

Figure 1. Series 2+ Flash Memory Card Block Diagram Showing Major Functional Elements

Table 1. Series 2+ Flash Memory Card Signals

Pin	Signal	I/O	Function	Active	Pin	Signal	I/O	Function	Active
1	GND		Ground		27	A_2	I	Address Bit 2	
2	DQ_3	I/O	Data Bit 3		28	A_1	I	Address Bit 1	
3	DQ_4	I/O	Data Bit 4		29	A_0	I	Address Bit 0	
4	DQ_5	I/O	Data Bit 5		30	DQ_0	I/O	Data Bit 0	
5	DQ_6	I/O	Data Bit 6		31	DQ_1	I/O	Data Bit 1	
6	DQ_7	I/O	Data Bit 7		32	DQ_2	I/O	Data Bit 2	
7	CE_1#	I	Card Enable 1	LOW	33	WP	O	Write Protect	HIGH
8	A_{10}	I	Address Bit 10		34	GND		Ground	
9	OE#	I	Output Enable	LOW	35	GND		Ground	
10	A_{11}	I	Address Bit 11		36	CD_1#	O	Card Detect 1	LOW
11	A_9	I	Address Bit 9		37	DQ_{11}	I/O	Data Bit 11	
12	A_8	I	Address Bit 8		38	DQ_{12}	I/O	Data Bit 12	
13	A_{13}	I	Address Bit 13		39	DQ_{13}	I/O	Data Bit 13	
14	A_{14}	I	Address Bit 14		40	DQ_{14}	I/O	Data Bit 14	
15	WE#	I	Write Enable	LOW	41	DQ_{15}	I/O	Data Bit 15	
16	RDY/BSY#	O	Ready/Busy	LOW	42	CE_2#	I	Card Enable 2	LOW
17	V_{CC}		Supply Voltage		43	VS_1	O	Voltage Sense 1	LOW
18	V_{PP1}		Supply Voltage		44	RFU		Reserved	
19	A_{16}	I	Address Bit 16		45	RFU		Reserved	
20	A_{15}	I	Address Bit 15		46	A_{17}	I	Address Bit 17	
21	A_{12}	I	Address Bit 12		47	A_{18}	I	Address Bit 18	
22	A_7	I	Address Bit 7		48	A_{19}	I	Address Bit 19	
23	A_6	I	Address Bit 6		49	A_{20}	I	Address Bit 20	
24	A_5	I	Address Bit 5		50	A_{21}	I	Address Bit 21	
25	A_4	I	Address Bit 4		51	V_{CC}		Supply Voltage	
26	A_3	I	Address Bit 3		52	V_{PP2}		Supply Voltage	

Table 1. Series 2+ Flash Memory Card Signals (Continued)

Pin	Signal	I/O	Function	Active
53	A_{22}	I	Address Bit 22	
54	A_{23}	I	Address Bit 23	
55	A_{24}	I	Address Bit 24	
56	A_{25}	I	Address Bit 25	
57	VS_2	O	Voltage Sense 2	N.C.
58	RST	I	Reset	HIGH
59	WAIT#	O	Extend Bus Cycle	LOW
60	RFU		Reserved	

Pin	Signal	I/O	Function	Active
61	REG#	I	Attribute Memory Select	LOW
62	BVD_2	O	Battery Voltage Detect 2	
63	BVD_1	O	Battery Voltage Detect 1	
64	DQ_8	I/O	Data Bit 8	
65	DQ_9	I/O	Data Bit 9	
66	DQ_{10}	I/O	Data Bit 10	
67	CD_2#	O	Card Detect 2	LOW
68	GND		Ground	

Table 2. Series 2+ Flash Memory Card Signal Description

Symbol	Type	Name and Function
A_0–A_{25}	INPUT	**ADDRESS INPUTS:** Address A_0 through A_{25} are address bus lines which enable direct addressing of up to 64 megabytes of memory on the card. Signal A_0 is not used in word access mode. A_{25} is the most significant bit.
DQ_0–DQ_{15}	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** DQ_0 through DQ_{15} constitute the bi-directional data bus. DQ_{15} is the most significant bit.
CE_1#,CE_2#	INPUT	**CARD ENABLE 1 & 2:** CE_1# enables even bytes, CE_2# enables odd bytes. Multiplexing A_0, CE_1# and CE_2# allows 8-bit hosts to access all data on D_0 through D_7.
OE#	INPUT	**OUTPUT ENABLE:** Active low signal gating read data from the memory card.
WE#	INPUT	**WRITE ENABLE:** Active low signal gating write data to the memory card.
RDY/BSY#	OUTPUT	**READY/BUSY OUTPUT:** Indicates status of internally timed erase or write activities. A high output indicates the memory card is ready to accept accesses. A low output indicates that a device in the memory card is busy with internally timed erase or write activities.
CD_1#,CD_2#	OUTPUT	**CARD DETECT 1 & 2:** These signals provide for correct memory card insertion detection. They are positioned at opposite ends of the card to detect proper alignment. The signals are connected to ground internally on the memory card, and will be forced low whenever a card is placed in the socket. The host socket interface circuitry shall supply 10K or larger pull-up resistors on these signal pins.
WP	OUTPUT	**WRITE PROTECT:** Write Protect reflects the status of the Write Protect switch on the memory card. WP set to high = write protected, providing internal hardware write lockout to the flash array.

Table 2. Series 2+ Flash Memory Card Signal Description (Continued)

Symbol	Type	Name and Function
V_{PP1},V_{PP2}		**WRITE/ERASE POWER SUPPLY:** (12 V nominal) for erasing memory array blocks or writing bytes in the array. These pins must be 12 V to perform and Write/Erase operation when not using the card's integrated V_{PP} generator. These signals may be disconnected but are required for ExCA™ standard compliance.
V_{CC}		**CARD POWER SUPPLY:** (3.3 V or 5 V nominal) for all internal circuitry.
GND		**GROUND** for all internal circuitry.
REG#	INPUT	**REGISTER SELECT:** Provides access to Series 2+ Flash Memory Card registers and Card Information Structure in the Attribute Memory Plane.
RST	INPUT	**RESET:** Active high signal for placing card in Power-On Default State.
WAIT#	OUTPUT	**WAIT:** (Extend Bus Cycle) This signal is driven high for compatibility.
BVD_1, BVD_2	OUTPUT	**BATTERY VOLTAGE DETECT:** These signals are driven high to maintain SRAM card compatibility.
VS_1, VS_2	OUTPUT	**VOLTAGE SENSE:** Notify the host socket of the card's V_{CC} requirements. VS_1 grounded and VS_2 open indicates a 3.3 V/5 V card has been inserted.
RFU		**RESERVED FOR FUTURE USE**
N.C.		**NO INTERNAL CONNECTION TO CARD**; pin may be driven or left floating.

3.2 Series 2+ Card Control Logic

The Card Control Logic, contained within two ASICS, handles the address decoding and data control for the Series 2+ Card. The component management registers are also contained within the Card Control Logic.

3.2.1 ADDRESS DECODE LOGIC

At the highest level, the Address Decode section determines when to select the Common Memory (REG# = V_{IH}) or Attribute Memory (REG# = V_{IL}) Planes. Within the Attribute Memory Plane (Figure 2) , the address decode logic determines when to select the Card Information Structure (CIS) or Component Management Registers (CMR). The CIS contains tuple information and is located at even-byte addresses beginning with address 0000H (refer to Section 6.0). The CMRs are mapped at even byte locations beginning at address 4000H (refer to Section 3.3 for a detailed description).

3.2.2 DATA CONTROL

As shown in Table 3, data paths and directions are selected by the Data Control logic using REG#, A_0, WE#, OE#, CE_1#, and CE_2# as logic inputs. The Data Control logic selects any of the PCMCIA word-wide, byte-wide, and odd-byte modes for either Reads or Writes to Common or Attribute Memory. All accesses to the Attribute Memory Plane must be made through D[7:0] no valid data can be written on the high byte. Reads of D[15:8] will yield FFH.

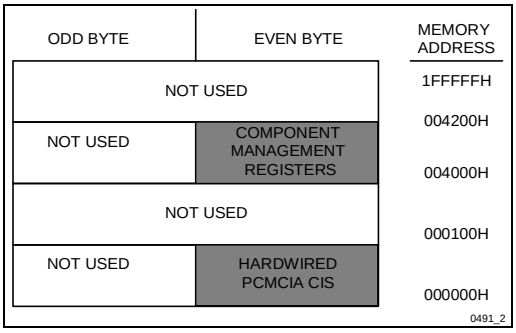

Figure 2. Attribute Memory Plane

Table 3. Data Access Mode Truth Table

COMMON MEMORY PLANE										
Mode	**REG#**	**CE_2#**	**CE_1#**	**A_0**	**OE#**	**WE#**	**V_{PP2}**	**V_{PP1}**	**D[15:8]**	**D[7:0]**
Standby	X	V_{IH}	V_{IH}	X	X	X	V_{PPL}	V_{PPL}	High-Z	High-Z
Byte-Read	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	High-Z	Even
	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	High-Z	Odd
Word-Read	V_{IH}	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	Odd	Even
Odd Byte-Read	V_{IH}	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	Odd	High-Z
Byte-Write	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	XXX	V_{PPH}	XXX	Even
	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{PPH}	XXX	XXX	Odd
Word-Write	V_{IH}	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	Odd	Even
Odd Byte-Write	V_{IH}	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	V_{PPH}	V_{PPL}	Odd	XXX
ATTRIBUTE MEMORY PLANE										
Mode	**REG#**	**CE_2#**	**CE_1#**	**A_0**	**OE#**	**WE#**	**V_{PP2}**	**V_{PP1}**	**$D_{[15:8]}$**	**$D_{[7:0]}$**
Standby	X	V_{IH}	V_{IH}	X	X	X	V_{PPL}	V_{PPL}	High-Z	High-Z
Byte-Read	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	High-Z	Even
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	High-Z	FFH
Word-Read	V_{IL}	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	FFH	Even
Odd Byte-Read	V_{IL}	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	FFH	High-Z
Byte-Write	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{PPL}	V_{PPL}	XXX	Even
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{PPL}	V_{PPL}	XXX	XXX
Word-Write	V_{IL}	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	V_{PPL}	V_{PPL}	XXX	Even
Odd Byte-Write	V_{IL}	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	V_{PPL}	V_{PPL}	XXX	XXX

NOTE:

When using the V_{PP} generator, V_{PP1} and V_{PP2} are “don’t care.”

3.3 Component Management Registers

The Component Management Registers (CMRs) are classified into two categories: those defined by PCMCIA Rev 2.0, and those included by Intel to enhance the interface between the host system and the card’s flash memory array. The CMRs provide five control functions: ready-musy mode selection, voltage control, software write protection, card status and soft reset. For more details about the CMR functionality, consult Intel’s *Series 2+ Flash Memory Card User’s Manual* (297373).

3.4 SmartPower

The SmartPower circuitry generates and monitors the card’s programming voltages. When a host system does not provide a valid V_{PP} supply, the card’s integrated generator can be switched on via the voltage control register. The SmartPower circuitry also detects the host system’s V_{CC} level (3.3 V or 5.0 V) and configures the card’s flash memory devices, accordingly driving the 3/5# pin to the memory array to the appropriate value.

The SmartPower circuitry is enabled by writing a “1” to Bit 0 of the voltage control register.

Table 4. Configuration Option Register - PCMCIA (Soft Reset Register)

Attribute Memory Plane Address: 4000H
Read/Write

SRESET	LevlREQ	Configuration Index					
7	6	5	4	3	2	1	0

Default: 02H

Bit 7 = Soft Reset
1 = Reset State
0 = End Reset Cycle

Bit 6 = Level Request
Driven Low

Bits 5-0 = Configuration Index
May Be Written with Values 1-4, Refer to Index in CIS Card Configuration Table Tuple.

Table 5. Card Configuration and Status Register - PCMCIA (Global Power-Down Register)

Attribute Memory Plane Address: 4002H
Read/Write

Reserved					PWRDWN	Reserved	
7	6	5	4	3	2	1	0

Default: 00H

Bit 2 = Power-Down
1 = 28F016SAs in Reset Power-Down
0 = Power-Up

Table 6. Card Status Register - Intel

Attribute Memory Plane Address: 4100H
Read Only

Reserved		SRESET	CMWP	PWRDWN	CISWP	WP	RDY/BSY#
7	6	5	4	3	2	1	0

Default: 01H or 03H

Bit 5 = Soft Reset
1 = Reset State

Bit 4 = Common Memory Write Protect
1 = Write Protected

Bit 3 = Power-Down
1 = Power-Down

Bit 2 = Common Memory CIS Write Protect
1 = Write Protected

Bit 1 = Write Protect Switch
1 = Write Protected

Bit 0 = Card Ready/Busy#
1 = Ready

Table 7. Write Protection Register - Intel

Attribute Memory Plane Address: 4104H
Read/Write

Reserved					BLKEN	CMWP	CISWP
7	6	5	4	3	2	1	0

Default: 04H

Bit 2 = Block Locking Enable
- 1 = Enable Independent 28F016SA Block Locking
- 0 = All Blocks Unlocked

Bit 1 = Common Memory Write Protect
- 1 = Common Memory Minus the CMCIS in Write Protect Status
- 0 = Write Protect According to Independent 28F016SA Block Locking

Bit 0 = Common Memory CIS Write Protect
- 1 = Common Memory CIS in Write Protect Status
- 0 = Write Protect According to Independent 28F016SA Block Locking

Table 8. Voltage Control Register - Intel

Attribute Memory Plane Address: 410CH
Read/Write

V_{CC} LEVEL	Reserved					V_{PP} VALID	V_{PP} GEN
7	6	5	4	3	2	1	0

Default: 82 or 02H

Bit 7 = V_{CC} Level: Read Only Bit
- 1 = Host Supplying 3.3 V
- 0 = Host Supplying 5 V

Bit 1 = V_{PP} Valid
- 1 = V_{PP} between 11.4 V and 12 V
- 0 = V_{PP} Invalid

Bit 0 = V_{PP} Generation
- 1 = Turn on Integrated V_{PP} Generator
- 0 = Turn off Integrated V_{PP} Generator

Note: The V_{PP} Valid bit only reflects the state of the V_{PP} Generator, NOT the external V_{PP}.

Table 9. Ready/Busy Mode Register - Intel

Attribute Memory Plane Address: 4140H
Read/Write

Reserved						RACK	MODE
7	6	5	4	3	2	1	0

Default: 00H

Bit 1 = Ready Acknowledge
- 0 = Clear RDY/BSY#

Bit 0 = RDY/BSY# Mode
- 1 = High-Performance Mode
- 0 = PCMCIA Level Mode

4.0 DEVICE COMMAND SET

The 28F016SA/DD28F032SA-based Series 2+ Command Set increases functionality over earlier 28F008SA-based designs while maintaining backwards compatibility. The extended command set incorporates many new features to improve programmability and write performance such as: page buffered writing, individual block locking, multiple RDY/BSY# configurations and device level queuing capabilities. The following pages list the Series 2+ command set and Bus Cycle Operations overview.

Series 2+ Command Set

Codes (H)	Series 2 Compatible Mode
00H	Invalid/Reserved
10H	Alternate Data Write
20H	Single Block Erase
40H	Data Write
50H	Clear Status Registers
70H	Read CSR
90H	Read ID Codes
B0H	Erase Suspend
D0H	Confirm/Resume
FFH	Read Flash Array

Codes (H)	Series 2+ Performance Enhancement
0CH	Page Buffer Write to Flash
71H	Read GSR or BSRs
72H	Page Buffer Swap
74H	Single Load to Page Buffer
75H	Read Page Buffer
77H	Lock Block
80H	Abort
96H,01H	RY/BY# Level Mode Enable
96H,02H	RY/BY# Pulse-On-Write
96H,03H	RY/BY# Pulse-On Erase
96H,04H	RY/BY# Disable
97H	Upload Status Bits
99H	Upload Device Information
A7H	Erase All Unlocked Blocks
E0H	Sequential Load to Page Buffer
F0H	Sleep

Table 10. 28F008SA-Compatible Mode Command Bus Definitions

Command	First Bus Cycle				Second Bus Cycle			
	R/W	Addr	Data		R/W	Addr	Data	
			Byte	Word			Byte	Word
Read Array	W	DA	FFH	FFFFH	R	DA	AD	AD
Intelligent Identifier	W	DA	90H	9090H	R	IA	ID	ID
Read CSR (See 1)	W	DA	70H	7070H	R	DA	CSRD	CSRD
Clear Status Register (See 2)	W	DA	50H	5050H				
Word/Byte Write §	W	WA	40H	4040H	W	WA	WD	WD
Word/Byte Write (Alternate) §	W	WA	10H	1010H	W	WA	WD	WD
Block Erase/Confirm §	W	BA	20H	2020H	W	BA	D0H	D0D0H
Erase Suspend/Resume	W	DA	B0H	B0B0H	W	DA	D0H	D0D0H

ADDRESSES:

DA	Device Address
BA	Block Address
IA	Identifier Address
WA	Write Address

DATA:

AD	Array Data
CSRD	CSR Data
ID	Identifier Data
WD	Write Data

§ = Queueable Commands

NOTES:

1. The CSR is automatically available after the device enters data write, erase or suspend operations.
2. Clears CSR.3, CSR.4 and CSR.5. Also clears GSR.5 and all BSR.5 and BSR.2 bits.

Table 11. 28F016SA-Super-Set Mode Performance Enhancement Command Bus Definitions

Command	Notes	First Bus Cycle				Second Bus Cycle				Third Bus Cycle			
		Oper	Addr	Data		Oper	Addr	Data		Oper	Addr	Data	
				Byte	Word			Byte	Word			Byte	Word
Read Page Buffer		W	DA	75H	7575H	R	PA	PD	PDPD				
Page Buffer Swap	6	W	DA	72H	7272H								
Single Load to Page Buffer		W	DA	74H	7474H	W	PA	PD	PDPD				
Sequential Load to Page Buffer	4,5	W	DA	E0H	E0E0H	W	DA	BCH		W	DA	BCH	
Page Buffer Write to Flash Array §	3,4,5	W	DA	0CH	0C0CH	W	A_0	BC(L,H)		W	WA	BC(H,L)	
RY/BY# Pulse-On-Erase §	7	W	DA	96H	9696H	W	DA	D0H	D0D0H				
RY/BY# Pulse-On-Write §	7	W	DA	96H	9696H	W	DA	D1H	D1D1H				
RY/BY# Enable to Level-Mode §	7	W	DA	96H	9696H	W	DA	D2H	D2D2H				
RY/BY# Disable §	7	W	DA	96H	9696H	W	DA	D3H	D3D3H				
Lock Block/ Confirm §		W	DA	77H	7777H	W	BA	D0H	D0D0H				
Upload Status Bits/ Confirm §	2	W	DA	97H	9797H	W	DA	D0H	D0D0H				
Read Extended Status Registers	1	W	DA	71H	7171H	R	RA	GSRD/BSRD					
Erase All Unlocked Blocks/ Confirm §		W	DA	A7H	A7A7H	W	DA	D0H	D0D0H				
Sleep		W	DA	F0H	F0F0H								
Abort		W	DA	80H	8080H								
Upload Device Information		W	DA	99H	9999H	W	DA	D0H	D0D0H				

ADDRESSES		DATA		DATA COUNTS	
DA	Device Address	AD	Write Address	WC(L,H)	Word Count (Low, High)
BA	Block Address	CSRD	CSR Data	BC(L,H)	Byte Count (Low, High)
IA	Identifier Address	G/BSRD	GSR/BSR Data	WD(L,H)V	Write Data (Low, High)
PA	Page Buffer Address	ID	Identifier Data		
RA	Extended Register Address	WD	Write Data		
WA	Write Address	PD	Page Buffer Data		
X	Don't Care				

§ = Queueable Commands

NOTES:

1. RA can be the GSR address or any BSR address.
2. Upon device power-up, all BSR lock-bits are locked. The Lock Status Upload command must be written to reflect the actual lock-bit status.
3. A_0 is automatically complemented to load the second byte of data.
4. BCH/WCH must be at 00H for this product because of the 256-byte Page Buffer size *and* to avoid writing the Page Buffer contents into more than one 256-byte segment within an array block. They are simply shown for Page Buffer expandability.
5. PA and PD (whose count is given in cycles 2 and 3) are supplied starting in the fourth cycle (not shown).
6. This command allows the user to swap between available page buffers (0 or 1).
7. These commands reconfigure RY/BY# output to one of two pulse modes, or they enable and disable the RY/BY# function.

5.0 DEVICE STATUS REGISTER

Each 28F016SA has three types of status registers: the Compatible Status Register (CSR), the Global Status Register (GSR) and the Block Status Register (BSR). The CSR is identical to the 28F008SA status register. The GSR contains queue and page buffer information about each device. Each block within the device has a BSR assigned to it. The BSR contains the block locking status and other information specific to the block being addressed.

Table 12. Compatible Status Register

Read Only Register

WSMS	ESS	ES	DWS	VPPS	Reserved		
7	6	5	4	3	2	1	0

Default: 80H

CSR.7 = WRITE STATE MACHINE STATUS (WSMS)
1 = Ready
0 = Busy

CSR.6 = ERASE-SUSPEND STATUS (ESS)
1 = Erase Suspended
0 = Erase In Progress/Completed

CSR.5 = ERASE STATUS (ES)
1 = Error In Block Erasure
0 = Successful Block Erase

CSR.4 = DATA-WRITE STATUS (DWS)
1 = Error in Data Write
0 = Data Write Successful

CSR.3 = V_{PP} STATUS (VPPS)
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

Table 13. Global Status Register

WSMS	OSS	DOS	DSS	QS	PBAS	PBS	PBSS
7	6	5	4	3	2	1	0

GSR.7 = WRITE STATE MACHINE STATUS
- 1 = Ready
- 0 = Busy

GSR.6 = OPERATION SUSPEND STATUS
- 1 = Operation Suspended
- 0 = Operation in Progress/Completed

GSR.5 = DEVICE OPERATION STATUS
- 1 = Operation Unsuccessful
- 0 = Operation Successful or Currently Running

GSR.4 = DEVICE SLEEP STATUS
- 1 = Device in Sleep
- 0 = Device Not in Sleep

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0 0 = Operation Successful or Currently Running	If operation currently running, then GSR.7 = 0.
0 1 = Device in Sleep Mode or Pending Sleep	If device pending sleep, then GSR.7 = 0.
1 0 = Operation Unsuccessful	
1 1 = Operation Unsuccessful or Aborted	Operation aborted: Unsuccessful due to Abort command.

GSR.3 = QUEUE STATUS
- 1 = Queue Full
- 0 = Queue Available

GSR.2 = PAGE BUFFER AVAILABLE STATUS
- 1 = One or Two Page Buffers Available — The device contains two Page Buffers.
- 0 = No Page Buffer Available

GSR.1 = PAGE BUFFER STATUS
- 1 = Selected Page Buffer Ready
- 0 = Selected Page Buffer Busy — Selected Page Buffer is currently busy with WSM operation.

GSR.0 = PAGE BUFFER SELECT STATUS
- 1 = Page Buffer 1 Selected
- 0 = Page Buffer 0 Selected

NOTES:

[1] RY/BY# output or WSMS bit must be checked to determine completion of an operation (block lock, erase suspend, any RY/BY# reconfiguration, Upload Status Bits, block erase or data program) before the appropriate Status bit (OSS or DOS) is checked for success.

NOTE:

1. When multiple operations are queued, checking BSR.7 only provides indication of completion for that particular block. GSR.7 provides indication when all queued operations are completed.

Table 14. Block Status Register

BS	BLS	BOS	BOAS	QS	VPPS	Reserved	
7	6	5	4	3	2	1	0

Default: 80H

BSR.7 = BLOCK STATUS (BS)
1 = Ready
0 = Busy

BSR.6 = BLOCK-LOCK STATUS (BLS)
1 = Block Unlocked for Write/Erase
0 = Block Locked for Write/Erase

BSR.5 = BLOCK OPERATION STATUS (BOS)
1 = Operation Unsuccessful
0 = Operation Successful or Currently Running

BSR.4 = BLOCK OPERATION ABORT STATUS (BOAS)
1 = Operation Aborted
0 = Operation Not Aborted

BSR.3 = QUEUE STATUS (QS)
1 = Queue Full
0 = Queue Available

BSR.2 = V_{PP} STATUS (VPPS)
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

6.0 PCMCIA CARD INFORMATION STRUCTURE

The Card Information Structure (CIS) begins at address 00000000H of the card's Attribute Memory Plane. It contains a variable length chain of data blocks (tuples) that conform to a basic format (Table 15). The CIS of the Series 2+ Flash Memory Card is found in Table 16.

Table 15. PCMCIA Tuple Format

Bytes	Data
0	Tuple Code: CISTPL_xxx. The tuple code 0FFH indicates no more tuples in the list.
1	Tuple Link: TPL_LINK. Link to the next tuple in the list. This can be viewed as the number of additional bytes in tuple, excluding this byte. A link field of zero indicates an empty tuple body. A link field containing 0FFH indicates the last tuple in the list.
2-n	Bytes specific to this tuple.

Table 16. Tuples for Series 2+ Card

Address	Value	Description
00h	01H	**CISTPL_DEVICE**
02h	04H	TPL_LINK
04h	57H	FLASH
06h	22H	150 ns
	32H	250 ns
08h		CARD SIZE
	0EH	4 MB
	1EH	8 MB
	4EH	20 MB
	9EH	40 MB
0AH	FFH	END OF DEVICE
0CH	1CH	**CISTPL_DEVICE_OC**
0EH	05H	TPL_LINK
10H	02H	OTHER CONDITIONS - 3 V_{CC}
12H	57H	FLASH
14H	32H	250 ns
16H		CARD SIZE
	0EH	4 MB
	1EH	8 MB
	4EH	20 MB
	9EH	40 MB
18H	FFH	END OF DEVICE
1AH	17H	**CISTPL_DEVICE_A**
1CH	04H	TPL_LINK
1EH	1FH	ROM
20H	22H	150 ns
22H	01H	2 Kb
24H	FFH	END OF DEVICE
26H	1DH	**CISTPL_DEVICE_OA**
28H	05H	TPL_LINK
2AH	02H	OTHER CONDITIONS - 3 V_{CC}
2CH	17H	ROM
2EH	32H	250 ns
30H	01H	2 Kb
32H	FFH	END OF DEVICE
34H	18H	**CISTPL JEDEC_C**
36H	02H	TPL_LINK
38H	89H	INTEL J-ID

Address	Value	Description
3AH	A0H	28F016 J-ID
3CH	00H	NULL CONTROL TUPLE
3EH	15H	**CISTPL VERS 1**
40H	39H	TPL_LINK
42H	04H	TPLLV1_MAJOR
44H	01H	TPLLV1_MINOR
		TPLLV1_INFO
46H	49H	I
48H	6EH	n
4AH	74H	t
4CH	65H	e
4EH	6CH	l
50H	00H	END TEXT
52H	53H	S
54H	32H	2
56H	45H	E
58H	34H	4 MB
	38H	8 MB
	32H	20 MB
	34H	40 MB
5AH	20H	4 MB
	20H	8 MB
	30H	20 MB
	30H	40 MB
5CH	53H	S
	20H	SPACE
5EH	57H	W
	20H	SPACE
60H	00H	ENDTEXT
62H	43H	C
64H	4FH	O
66H	50H	P
68H	59H	Y
6AH	52H	R
6CH	49H	I
6EH	47H	G
70H	48H	H
72H	54H	T

Table 16. Tuples for Series 2+ Card (Continued)

Address	Value	Description	Address	Value	Description
74H	20H	SPACE	BEH	40H	TPCC_RADR
76H	49H	I	C0H	03H	TPCC_RMSK
78H	6EH	n	C2H	00H	NULL CONTROL TUPLE
7AH	74H	t	C4H	1BH	**CISTPL_CFTABLE_ENTRY**
7CH	65H	e	C6H	08H	TPL_LINK
7EH	6CH	l	C8H	01H	**TPCE_INDEX (01H)**
80H	20H	SPACE	CAH	01H	TPCE_FS (V_{CC} ONLY)
82H	43H	C	CCH	79H	TPCE_PD V_{CC} PARAMETER SELECTION BYTE
84H	4FH	O			
86H	52H	R			
88H	50H	P	CEH	55H	V_{CC} NOMINAL VOLTAGE 5 V ± 5%
8AH	4FH	O			
8CH	52H	R	D0H	53H	I_{CC} STATIC 500 µA
8EH	41H	A	D2H	1EH	I_{CC} AVERAGE 150 mA
90H	54H	T	D4H	1EH	I_{CC} PEAK 150 mA
92H	49H	I	D6H	1BH	I_{CC} PWRDWN 200 µA
94H	4FH	O	D8H	1BH	**CISTPL_CFTABLE_ENTRY**
96H	4EH	N	DAH	0FH	TPL_LINK
98H	20H	SPACE	DCH	02H	**TPCE_INDEX (02H)**
9AH	31H	1	DEH	02H	TPCE_FS (V_{CC} AND V_{PP})
9CH	39H	9	E0H	79H	TPCE_PD V_{CC} PARAMETER SELECTION BYTE
9EH	39H	9			
A0H	33H	3			
A2H	20H	SPACE	E2H	55H	V_{CC} NOMINAL VOLTAGE 5 V ± 5%
A4H	47H	G			
A6H	4CH	L	E4H	2BH	I_{CC} STATIC 250 µA
A8H	41H	A	E6H	06H	I_{CC} AVERAGE 100 mA
AAH	44H	D	E8H	06H	I_{CC} PEAK 100 mA
ACH	45H	E	EAH	52H	I_{CC} PWRDWN 50 µA
AEH	4BH	K			TPCE_PD
B0H	00H	END TEXT	ECH	79H	V_{PP} PARAMETER
B2H	FFH	END OF LIST			SELECTION BYTE
B4H	1AH	**CISTPL_CONF**	EEH	8EH	12.0 V ± 5%
B6H	05H	TUPL_LINK	F0H	7DH	NC OK ON STANDBY & PWD
B8H	01H	TPCC_SZ	F2H	53H	I_{PP} STATIC 500 µA
BAH	04H	TPCC_LAST	F4H	25H	I_{PP} AVERAGE 20 mA
BCH	00H	TPCC_RADR	F6H	25H	I_{PP} PEAK 20 mA

Table 16. Tuples for Series 2+ Card (Continued)

Address	Value	Description
F8H	52H	IPP PWRDWN 50 µA
FAH	1BH	**CISTPL_CFTABLE_ENTRY**
FCH	09H	TPL_LINK
FEH	03H	**TPCE_INDEX (03H)**
100H	01H	TPCE_FS (V_{CC} ONLY)
102H	79H	TPCE_PD V_{CC} PARAMETER SELECTION BYTE
104H	B5H	V_{CC} = 3.3 V
106H	1EH	EXTENSION BYTE
108H	04H	I_{CC} STATIC 1 mA
10AH	1EH	I_{CC} AVERAGE 150 mA
10CH	1EH	I_{CC} PEAK 150 mA
10EH	53H	I_{CC} PWRDWN 500 µA
110H	1BH	**CISTPL_CFTABLE_ENTRY**
112H	10H	TPL_LINK
114H	04H	**TPCE_INDEX (04H)**
116H	02H	TPCE_FS (V_{CC} AND V_{PP})
118H	79H	TPCE_PD V_{CC} PARAMETER SELECTION BYTE
11AH	B5H	V_{CC} = 3.3 V
11CH	1EH	EXTENSION BYTE
11EH	2BH	I_{CC} STATIC 250 µA
120H	06H	I_{CC} AVERAGE 100 mA
122H	06H	I_{CC} PEAK 100 mA
124H	52H	I_{CC} PWRDWN 50 µA
126H	79H	TPCE_PD V_{PP} PARAMETER SELECTION BYTE
128H	8EH	12.0 V =/- 5%
12AH	7DH	NC OK ON STANDBY & PWD
12CH	53H	I_{PP} STATIC 500 µA
12EH	25H	I_{PP} AVERAGE 20 mA
130H	25H	I_{PP} PEAK 20 mA
132H	1BH	I_{PP} PWRDWN 150 µA
134H	00H	NULL CONTROL TUPLE

Address	Value	Description
136H	00H	NULL CONTROL TUPLE
138H	1EH	**CISTPL DEVICEGEO**
13AH	06H	TPL_LINK
13CH	02H	DGTPL_BUS
13EH	11H	DGTPL_EBS
140H	01H	DGTPL_RBS
142H	01H	DGTPL_WBS
144H	01H	DGTPL_PART = 1
146H	01H	FLASH DEVICE INTERLEAVE
148H	20H	**CISTPL_MANFID**
14AH	04H	TPL_LINK (04H)
		TPLMID_MANF
14CH	89H	LSB
14EH	00H	MSB
150H	12H	4 MB - 150 ns
	22H	8 MB - 150 ns
	42H	20 MB - 150 ns
	62H	40 MB - 150 ns
152H	84H	TPLMID_CARD MSB
154H	21H	**CISTPL_FUNCID**
156H	02H	TPL_LINK
158H	01H	TPLFID_FUNCTION (MEMORY)
15AH	00H	TPLFID_SYSINIT (NONE)
15CH	FFH	**CISTPL_END**
	00H	INVALID ADDRESS
		(156H-1FEH)

7.0 SYSTEM DESIGN CONSIDERATIONS

7.1 Power Supply Decoupling

Flash memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current issues: standby, active and transient current peaks which are produced by rising and falling edges of CE_1# and CE_2#. The capacitive and inductive loads on the card and internal flash memory device pairs determine the magnitudes of these peaks.

Three-line control and proper decoupling capacitor selection suppress transient voltage peaks. Series 2+ cards contain on-card ceramic decoupling capacitors connected between V_{CC} and GND, and between V_{PP1}/V_{PP2} and GND.

The card connector should also have a 4.7 µF electrolytic capacitor between V_{CC} and GND, as well as between V_{PP1}/V_{PP2} and GND. The bulk capacitors overcome voltage slumps caused by printed-circuit-board trace inductance, and supply charge to the smaller capacitors as needed.

7.2 Power-Up/Down Protection

The PCMCIA/JEIDA-specified socket properly sequences the power supplies to the flash memory card via shorter and longer pins. This design assures that hot insertion and removal will not result in card damage or data loss.

Each device in the memory card is designed to offer protection against accidental erasure or writing, caused by spurious system-level signals that may exist during power transitions. The card will power-up into the read state.

A system designer must guard against active writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both WE# and CE_1# must be low for a command write, driving either to V_{IH} will inhibit writes. With its control register architecture, alteration of device contents only occurs after successful completion of the two-step command sequences. While these precautions are sufficient for most applications, an alternative approach would allow V_{CC} to reach its steady state value before raising V_{PP1}/V_{PP2} above V_{CC} + 2.0 V. In addition, upon powering down, V_{PP1}/V_{PP2} should be below V_{CC} + 2.0 V before lowering V_{CC}.

NOTE

The Integrated V_{PP} generator defaults to the power off condition after reset and system power-up. The V_{PP} Generation circuitry must be enabled for the memory card to operate in 3.3 V-only or 5.0 V-only mode.

7.3 Hot Insertion/Removal

The capability to remove or insert PC cards while the system is powered on (i.e., hot insertion/removal) requires careful design approaches on the system and card levels. To design for this capability, consider card over-voltage stress, system power fluxuations and control line stability.

8.0 ELECTRICAL SPECIFICATIONS

NOTICE: This is a production datasheet. The specifications are subject to change without notice.

8.1 Absolute Maximum Ratings*

** WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may effect device reliability.*

Operating Temperature

During Read ..... 0 °C to +60 °C(1)
During Write ..... 0 °C to +60 °C

Storage Temperature..... –30 °C to +70 °C(2)

Voltage on Any Pin with
Respect to Ground ..... –2.0 V to V_{CC} +2.0 V(2)

V_{PP1}/V_{PP2} Supply Voltage with
Respect to Ground .. –2.0 V to V_{CC} +14.0 V(2,3)

V_{CC} Supply Voltage with
Respect to Ground .....–0.5 V to +7.0 V

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC input voltage is -0.5 V. During transitions, inputs may undershoot to 2.0 V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.
3. Maximum DC input voltage on V_{PP1}/V_{PP2} may overshoot to +14.0 V for periods less than 20 ns.
4. V_{PP} generator turned “on” for 3.3 V or 5.0 V only operation.

8.2 Operating Conditions

Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC} at 3.3 V, 12 V V_{PP}	V_{CC} Supply Voltage (±0.3 V)	3.0	3.6	V
V_{CC} at 3.3 V, V_{PP} Gen(4)	V_{CC} Supply Voltage (±0.15 V)	3.15	3.45	V
V_{CC} at 5.0 V	V_{CC} Supply Voltage (±0.25 V)	4.75	5.25	V

8.3 Capacitance(1)

T_A = +25 °C, f = 1 MHz

Symbol	Pins	Typ	Max	Unit
C_{IN}	A_0	15	30	pF
C_{IN}	Address/Control	10	20	pF
C_{IN}	V_{CC}, V_{PP}	2	2	pF
C_{OUT}	Output	10	20	pF

8.4 DC Characteristics

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
I_{LI}	Input Leakage Current	1,3		±20	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1		±20	µA	$V_{CC} = V_{CC}$ Max $V_{OUT}=V_{CC}$ or GND
V_{IL5}	Input Low Voltage	1	0	0.8	V	V_{CC} = 5 V
$V_{IL3.3}$				0.7		V_{CC} = 3.3 V
V_{IH5}	Input High Voltage	1	2.4	V_{CC} + 0.5	V	V_{CC} = 5 V
$V_{IH3.3}$			2.2	V_{CC} + 0.3		V_{CC} = 3.3 V
V_{OL}	Output Low Voltage	1		0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	1	V_{CC} – 0.4	V_{CC}	V	I_{OH} = –2.0 mA
V_{PPL}	V_{PP} during Read Only Operations	1,2	0	6.5	V	
V_{PPH}	V_{PP} during Read/Write Operations	1	11.4	12.6	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage	1	2.0		V	

NOTES:

1. Values are the same for byte and word wide modes for all card densities.
2. Block erases/data writes are inhibited when V_{PP} and V_{PPL} are not guaranteed in the range between V_{PPH} and V_{PPL}.
3. Exceptions: With V_{IN} = GND, the leakage current on CE_1#, CE_2#, REG#, OE#, and WE# will be < 500 µA due to internal pull-up resistors. With $V_{IN} = V_{CC}$, RST leakage current will be < 500 µA due to internal pull-down resistors. With $V_{IN} = V_{CC}$, A_{21}–A_{25} leakage current will be <100 µA due to internal pull down resistors.

8.5 DC Characteristics—CMOS Interfacing

V_{CC} = 3.3 V

Sym	Parameter	Density (Mbytes)	Notes	x8 Mode		x16 Mode		Unit	Test Conditions
				Typ	Max	Typ	Max		
I_{CCR}	V_{CC} Read Current	4, 8, 20, 40	1, 2, 3		75		100	mA	$V_{CC} = V_{CC}$ Max t_{CYCLE} = 250 ns
I_{CCW}	V_{CC} Write Current	4, 8, 20, 40	1, 2, 3, 4		40		50	mA	V_{PP} Gen = OFF during Data Write
			1, 2, 3, 5		100		175	mA	V_{PP} Gen = ON during Data Write
I_{CCE}	V_{CC} Erase Current	4, 8, 20, 40	1, 2, 3, 4		40		50	mA	V_{PP} Gen = OFF
			1, 2, 3, 5		80		150	mA	V_{PP} Gen = ON
I_{CCSL}	V_{CC} Sleep Current	4	1, 3, 4, 6	25	75	25	75	µA	$V_{CC} = V_{CC}$ Max
		8		25	95	25	95		Control Signals =
		20		35	155	35	155		V_{CC}
		40		45	255	45	255		
I_{CCS}	V_{CC} Standby Current	4	1, 2, 3, 4, 6	75	115	110	210	µA	$V_{CC} = V_{CC}$ Max
		8		80	125	115	230		Control Signals =
		20		85	155	120	250		V_{CC}
		40		100	200	150	300		
I_{PPW}	V_{PP} Write Current	4, 8, 20, 40	1, 2, 3, 4	10	15	20	30	mA	Data Write in Progress $V_{PP} = V_{PPH}$
I_{PPE}	V_{PP} Erase Current	4, 8, 20, 40	1, 2, 3, 4	6	12	12	22	mA	Block (Pair) Erase in Progress $V_{PP} = V_{PPH}$
I_{PPSL}	V_{PP} Sleep Current	4, 8, 20, 40	1, 2, 3, 4	0	0.5	0	0.5	mA	$V_{PP} \leq V_{CC}$
I_{PPS}	V_{PP} Standby/ Read Current	4, 8, 20, 40	1, 2, 3, 4	0	0.5	0	0.5	mA	$V_{PP} \leq V_{CC}$

CMOS Test Conditions: V_{IL} = GND ± 0.2 V $V_{IH} = V_{CC}$ ± 0.2 V

NOTES:

1. All currents are RMS values unless otherwise specified. Typical V_{CC} = 5 V, V_{PP} = 12 V, T = 25 °C.
2. Two devices active in word mode, one device active in byte mode.
3. Devices not addressed are in sleep mode.
4. V_{PP} Generation Circuitry turned off.
5. V_{PP} Generation Circuitry turned on.
6. Control Signals, CE_1#, CE_2#, OE#, WE#, REG#.

8.6 DC Characteristics—CMOS Interfacing

V_{CC} = 5.0 V

Sym	Parameter	Density (Mbytes)	Notes	x8 Mode		x16 Mode		Unit	Test Conditions
				Typ	Max	Typ	Max		
I_{CCR}	V_{CC} Read Current	4, 8, 20, 40	1, 2, 3		140		160	mA	$V_{CC} = V_{CC}$ Max t_{CYCLE} = 250 ns
I_{CCW}	V_{CC} Write Current	4, 8, 20, 40	1, 2, 3, 4		85		120	mA	V_{PP} Gen = OFF during Data Write
			1, 2, 3, 5		120		150	mA	V_{PP} Gen = ON during Data Write
I_{CCE}	V_{CC} Erase Current	4, 8, 20, 40	1, 2, 3, 4		75		100	mA	V_{PP} Gen = OFF
			1, 2, 3, 5		100	75	150	mA	V_{PP} Gen = ON
I_{CCSL}	V_{CC} Sleep Current	4	1, 3, 4, 6	25	75	25	75	µA	$V_{CC} = V_{CC}$ Max
		8		25	95	25	95		Control Signals =
		20		35	155	35	155		V_{CC}
		40		45	255	45	255		
I_{CCS}	V_{CC} Standby Current	4	1, 2, 3, 4, 6	75	115	110	210	µA	$V_{CC} = V_{CC}$ Max
		8		80	125	115	230		Control Signals =
		20		85	155	120	250		V_{CC}
		40		100	200	150	300		
I_{PPW}	V_{PP} Write Current	4, 8, 20, 40	1, 2, 3, 4	6	12	14	24	mA	Data Write in Progress $V_{PP} = V_{PPH}$
I_{PPE}	V_{PP} Erase Current	4, 8, 20, 40	1, 2, 3, 4	6	12	12	22	mA	Block (Pair) Erase in Progress $V_{PP} = V_{PPH}$
I_{PPSL}	V_{PP} Sleep Current	4, 8, 20, 40	1, 2, 3, 4	0	0.5	0	0.5	mA	$V_{PP} \leq V_{CC}$
I_{PPS}	V_{PP} Standby/ Read Current	4, 8, 20, 40	1, 2, 3, 4	0	0.5	0	0.5	mA	$V_{PP} \leq V_{CC}$

CMOS Test Conditions: V_{IL} = GND ± 0.2 V, $V_{IH} = V_{CC}$ ± 0.2 V

NOTES:

1. All currents are RMS values unless otherwise specified. Typical V_{CC} = 5 V, V_{PP} = 12 V, T = 25 °C.
2. Two devices active in word mode, one device active in byte mode.
3. Devices not addressed are in sleep mode.
4. V_{PP} Generation Circuitry turned off.
5. V_{PP} Generation Circuitry turned on.
6. Control Signals, CE_1#, CE_2#, OE#, WE#, REG#.

8.7 DC Characteristics—TTL Interfacing

V_{CC} = 3.3 V

Sym	Parameter	Density (Mbytes)	Notes	x8 Mode		x16 Mode		Unit	Test Conditions
				Typ	Max	Typ	Max		
I_{CCR}	V_{CC} Read Current	4, 8, 20, 40	1, 2, 3		75		90	mA	$V_{CC} = V_{CC}$ Max t_{CYCLE} = 250 ns
I_{CCW}	V_{CC} Write Current	4, 8, 20, 40	1, 2, 3, 4		85		100	mA	V_{PP} Gen = OFF during Data Write
			1, 2, 3, 5		150		225	mA	V_{PP} Gen = ON during Data Write
I_{CCE}	V_{CC} Erase Current	4, 8, 20, 40	1, 2, 3, 4		85		100	mA	V_{PP} Gen = OFF
			1, 2, 3, 5		125		180	mA	V_{PP} Gen = ON
I_{CCSL}	V_{CC} Sleep Current	4, 8, 20, 40	1, 3, 4, 6		70		70	mA	$V_{CC} = V_{CC}$ Max Control Signals = V_{IH}
I_{CCS}	V_{CC} Standby Current	4, 8, 20, 40	1, 2, 3, 4, 6		70		70	mA	$V_{CC} = V_{CC}$ Max Control Signals = V_{IH}
I_{PPW}	V_{PP} Write Current	4, 8, 20, 40	1, 2, 3, 4	10	15	20	30	mA	Data Write in Progress $V_{PP} = V_{PPH}$
I_{PPE}	V_{PP} Erase Current	4, 8, 20, 40	1, 2, 3, 4	5	10	10	20	mA	Block (Pair) Erase in Progress $V_{PP} = V_{PPH}$
I_{PPSL}	V_{PP} Sleep Current	4, 8, 20, 40	1, 2, 3, 4	0	0.5	0	0.5	mA	$V_{PP} \le V_{CC}$
I_{PPS}	V_{PP} Standby/ Read Current	4, 8, 20, 40	1, 2, 3, 4	0	0.5	0	0.5	mA	$V_{PP} \le V_{CC}$

TTL Test Conditions: V_{IL} = 0.7 V, V_{IH} = 2.2 V

NOTES:

1. All currents are RMS values unless otherwise specified. Typical V_{CC} = 5 V, V_{PP} = 12 V, T = 25 °C.
2. Two devices active in word mode, one device active in byte mode.
3. Devices not addressed are in sleep mode.
4. V_{PP} Generation Circuitry turned off.
5. V_{PP} Generation Circuitry turned on.
6. Control Signals, CE_1#, CE_2#, OE#, WE#, REG#.

8.8 DC Characteristics—TTL Interfacing

V_{CC} = 5.0 V

Sym	Parameter	Density (Mbytes)	Notes	x8 Mode		x16 Mode		Unit	Test Conditions
				Typ	Max	Typ	Max		
I_{CCR}	V_{CC} Read Current	4, 8, 20, 40	1, 2, 3		170		190	mA	$V_{CC} = V_{CC}$ Max t_{CYCLE} = 150 ns
I_{CCW}	V_{CC} Write Current	4, 8, 20, 40	1, 2, 3, 4		135		170	mA	V_{PP} Gen = OFF during Data Write
			1, 2, 3, 5		170		250	mA	V_{PP} Gen = ON during Data Write
I_{CCE}	V_{CC} Erase Current	4, 8, 20, 40	1, 2, 3, 4		125		150	mA	V_{PP} Gen = OFF
			1, 2, 3, 5		150		200	mA	V_{PP} Gen = ON
I_{CCSL}	V_{CC} Sleep Current	4, 8, 20, 40	1, 3, 4, 6		100		100	mA	$V_{CC} = V_{CC}$ Max Control Signals = V_{IH}
I_{CCS}	V_{CC} Standby Current	4, 8, 20, 40	1, 2, 3, 4, 6		100		100	mA	$V_{CC} = V_{CC}$ Max Control Signals = V_{IH}
I_{PPW}	V_{PP} Write Current	4, 8, 20, 40	1, 2, 3, 4	7	12	14	24	mA	Data Write in Progress $V_{PP} = V_{PPH}$
I_{PPE}	V_{PP} Erase Current	4, 8, 20, 40	1, 2, 3, 4	5	10	10	20	mA	Block (Pair) Erase in Progress $V_{PP} = V_{PPH}$
I_{PPSL}	V_{PP} Sleep Current	4, 8, 20, 40	1, 2, 3, 4	0	0.5	0	0.5	mA	$V_{PP} \leq V_{CC}$
I_{PPS}	V_{PP} Standby/ Read Current	4, 8, 20, 40	1, 2, 3, 4	0	0.5	0	0.5	mA	$V_{PP} \leq V_{CC}$

TTL Test Conditions: V_{IL} = 0.8 V, V_{IH} = 2.4 V

NOTES:

1. All currents are RMS values unless otherwise specified. Typical V_{CC} = 5 V, V_{PP} = 12 V, T = 25 °C.
2. Two devices active in word mode, one device active in byte mode.
3. Devices not addressed are in sleep mode.
4. V_{PP} Generation Circuitry turned off.
5. V_{PP} Generation Circuitry turned on.
6. Control Signals, CE_1#, CE_2#, OE#, WE#, REG#.

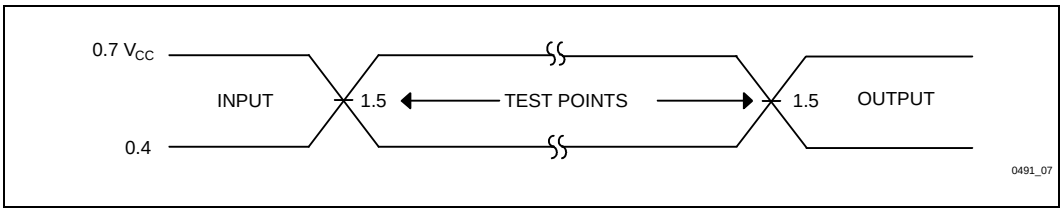


Figure 3. Transient Input/Output Reference Waveform (V_{CC} = 5.0 V) for Standard Test Configuration

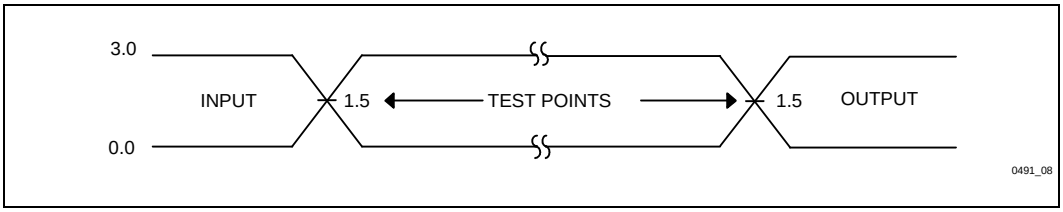


Figure 4. Transient Input/Output Reference Waveform (V_{CC} = 3.3 V) for Standard Test Configuration

8.9 AC Characteristics

AC timing diagrams and characteristics are designed to meet or exceed PCMCIA 2.1 specifications. No delay occurs when switching between the Common and Attribute Memory Planes.

8.9.1 READ OPERATIONS: COMMON MEMORY

Symbol		Parameter	150 ns at 5 V		250 ns at 3.3 V		Unit
JEDEC	PCMCIA		Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	150		250		ns
t_{AVQV}	t_a (A)	Address Access Time		150		250	ns
t_{ELQV}	t_a (CE)	Card Enable Access Time		150		250	ns
t_{GLQV}	t_a (OE)	Output Enable Access Time		75		125	ns
t_{EHQX}	t_{dis} (CE)	Output Disable Time from CE#		75		100	ns
t_{GHQZ}	t_{dis} (OE)	Output Disable Time from OE#		75		100	ns
t_{GLQX}	t_{en} (CE)	Output Enable Time from CE#	5		5		ns
t_{ELQX}	t_{en} (OE)	Output Enable Time from OE#	5		5		ns
t_{PHQV}		Power-Down Recovery to Output Delay. V_{CC} = 5 V		530		670	ns

NOTE:

1. Sampled, not 100% tested

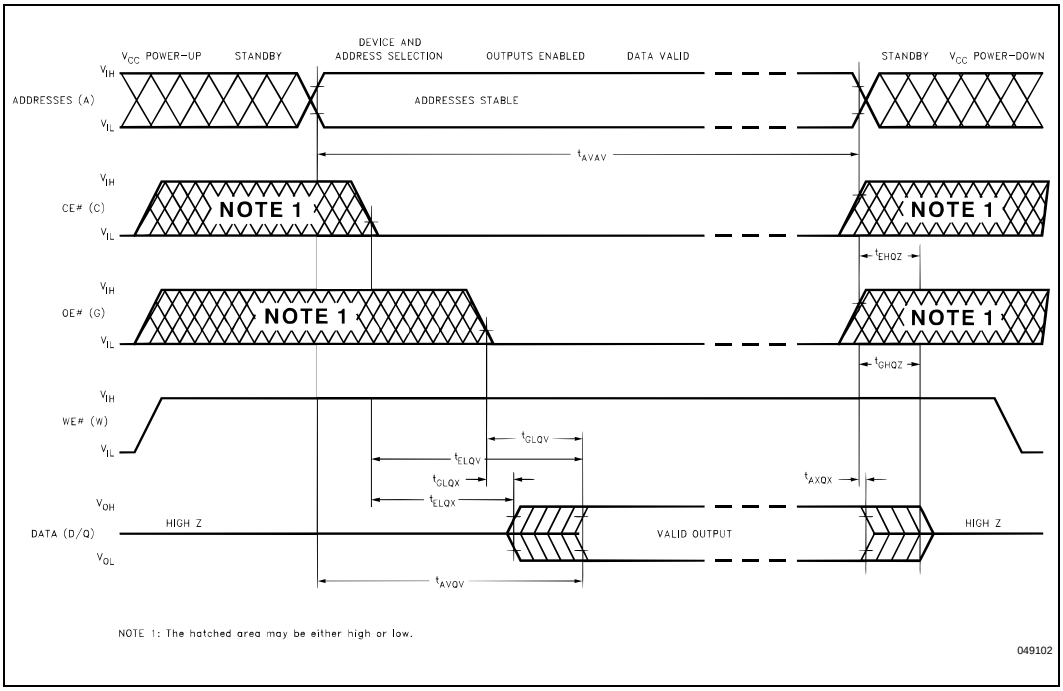


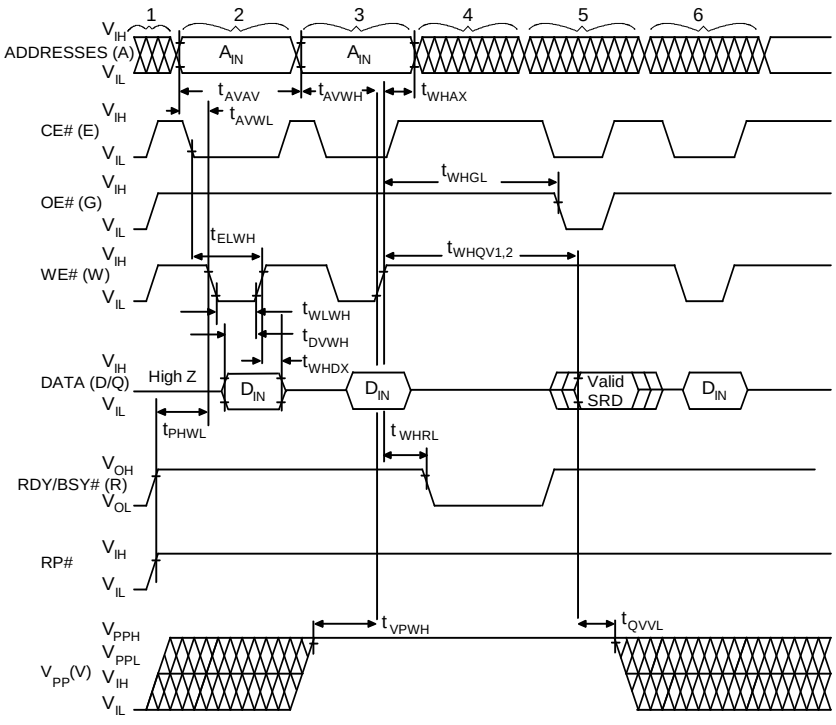
Figure 5. AC Waveforms for Read Operations

8.9.2 WRITE OPERATIONS: COMMON AND ATTRIBUTE MEMORY (1)

Symbol		Parameter	150 ns at 5 V		250 ns at 3.3 V		Unit
JEDEC	PCMCIA		Min	Max	Min	Max	
t_{AVAV}	t_cW	Write Cycle Time	150		250		ns
t_{WLWH}	t_w (WE)	Write Pulse Width	80		150		ns
t_{AVWL}	t_{su} (A)	Address Setup Time	20		30		ns
t_{AVWH}	t_{su} (A-WEH)	Address Setup Time for WE#	100		180		ns
t_{VPWH}	t_{vps}	V_{PP} Setup to WE# Going High	100		180		ns
t_{ELWH}	t_{su} (CEWEH)	Card Enable Setup Time for WE#	100		180		ns
t_{DVWH}	t_{su} (D-WEH)	Data Setup Time for WE#	50		80		ns
t_{WHDX}	t_h (D)	Data Hold Time	20		30		ns
t_{WHAX}	t_{rec} (WE)	Write Recover Time	20		30		ns
t_{WHRL}		WE# High to RDY/BSY#		140		140	ns
t_{QVVL}		V_{PP} Hold from Operation Complete	0		0		ns
t_{WHGL}	t_h (OE-WE)	Output Enable Hold from WE#	80		120		ns
t_{PHWL}		Power-Down Recovery to WE# Going Low		1		1	µs

NOTE:

1. Read timing characteristics during erase and data write operations are the same as during read-only operations. Refer to *Read Operations: Common Memory*



NOTES:

1. V_{CC} Power-Up and Standby
2. Write Program or Erase Setup Command
3. Write Valid Address and Program or Erase Confirm Command
4. Automated Program or Erase Delay
5. Read Status Register Data
6. Write Read Array Command

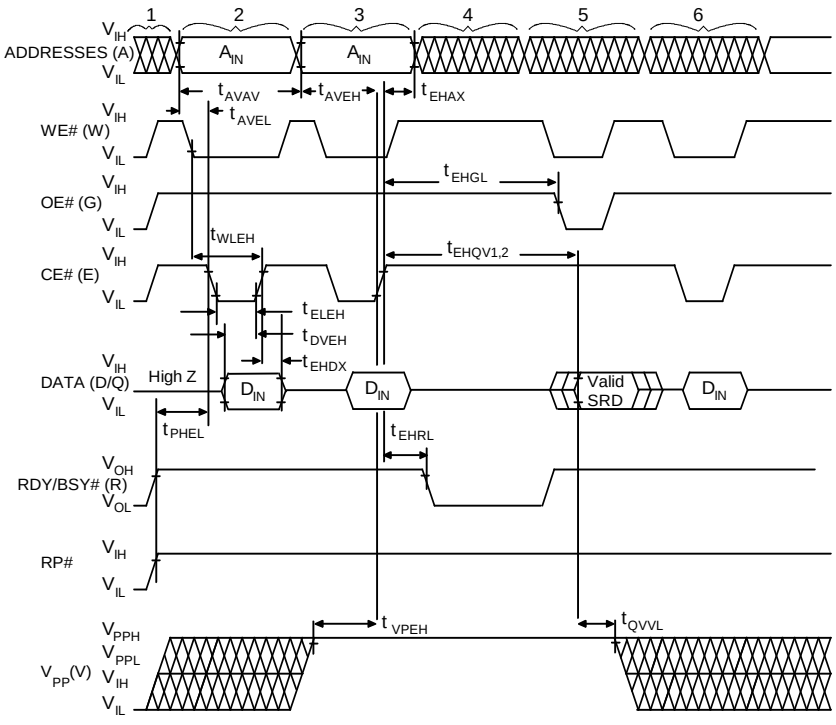
Figure 6. AC Waveforms for Write Operations

8.9.3 CE#-CONTROLLED WRITE OPERATIONS: COMMON AND ATTRIBUTE MEMORY

Symbol		Parameter	150 ns at 5 V		250 ns at 3.3 V		Unit
JEDEC	PCMCIA		Min	Max	Min	Max	
t_{AVAV}	t_cW	Write Cycle Time	150		250		ns
t_{ELEH}	t_w (WE)	Chip Enable Pulse Width	80		150		ns
t_{AVEL}	t_{su} (A)	Address Setup Time	20		30		ns
t_{AVEH}	t_{su} (A-WEH)	Address Setup Time for CE#	100		180		ns
t_{VPEH}	t_{vps}	V_{PP} Setup to CE# Going High	100		180		ns
t_{WLEH}	t_{su}(CE-WEH)	Write Enable Setup Time for CE#	100		180		ns
t_{DVEH}	t_{su} (D-WEH)	Data Setup Time for CE#	50		60		ns
t_{EHDX}	t_h (D)	Data Hold Time	20		30		ns
t_{EHAX}	t_{rec} (WE)	Write Recover Time	20		30		ns
t_{EHRL}		CE# High to RDY/BSY#		140		140	ns
t_{QVVL}		V_{PP} Hold from Operation Complete	0		0		ns
t_{EHGL}	t_h (OE-WE)	Output Enable Hold from WE#	80		120		ns
t_{PHEL}		Power-Down Recovery to CE# Going Low		1		1	µs

NOTE:

1. Read timing characteristics during erase and data write operations are the same as during read-only operations. Refer to *Read Operations: Common Memory.*



NOTES:

1. V_{CC} Power-Up and Standby
2. Write Data Write or Erase Setup Command
3. Write Valid Address and Data (Data Write) or Erase Confirm Command
4. Automated Data Write or Erase Delay
5. Read Status Register Data
6. Write Read Array Command

Figure 7. Alternate AC Waveform for Write Operations

8.9.4 POWER-UP/POWER-DOWN

Symbol	Parameter	Notes	Min	Max	Units
PCMCIA					
V_i (CE)	CE# Signal Level (0.0 V < V_{CC} < 2.0 V)	1	0	V_{iMAX}	V
	CE# Signal Level (2.0 V < V_{CC} < V_{IH})	1	V_{CC} - 0.1	V_{iMAX}	V
	CE# Signal Level (V_{IH} < V_{CC})	1	V_{IH}	V_{iMAX}	V
t_{su} (V_{CC})	CE# Setup Time		20		ms
t_{su} (RESET)	CE# Setup Time		20		ms
t_{rec} (V_{CC})	CE# Recover Time		1.0		µs
t_{pr}	V_{CC} Rising Time	2	0.1	300	ms
t_{pf}	V_{CC} Falling Time	2	3.0	300	ms
t_w (RESET)	RESET Width		10		µs
t_h (Hi-Z Reset)	RESET Width		1		ms
t_s (Hi-Z Reset)	RESET Width		0		ms

NOTES:

1. V_{iMAX} means Absolute Maximum Voltage for input in the period of 0.0 V < V_{CC} < 2.0 V, V_i (CE#) is only 0.00 V ~ V_{iMAX}.
2. The t_{pr} and t_{pf} are defined as “linear waveforms” in the period of 10% to 90%, or vice-versa. Even if the waveform is not a “linear waveform,” its rising and falling time must meet this specification.

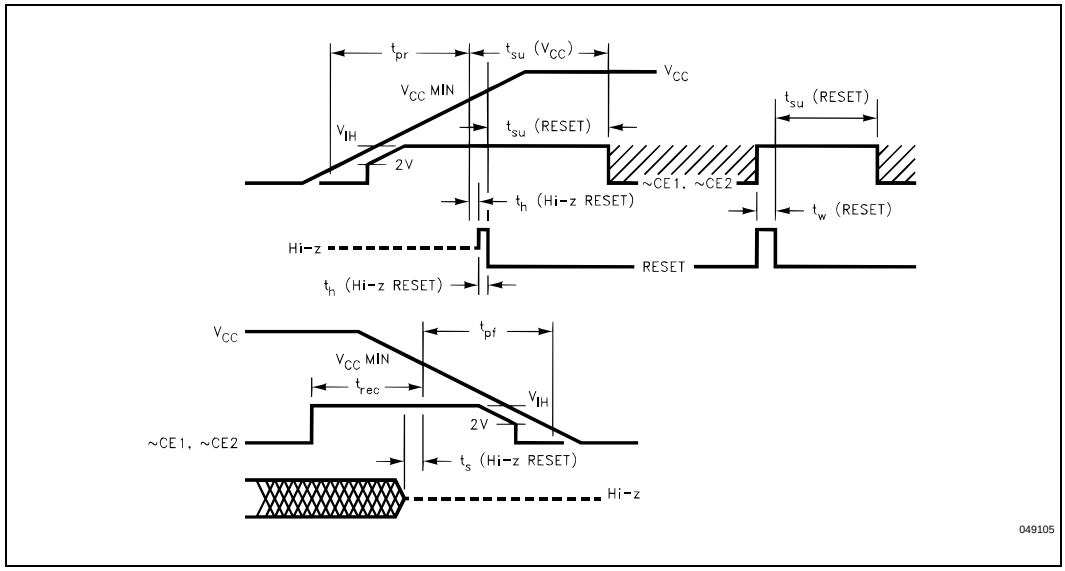


Figure 8. Power-Up Timing for Systems Supporting RESET#

8.10 Erase and Data Write Perfomance(1,3)

V_{CC} = 3.3 V ± 0.3 V, T_A = 0 °C to +70 °C

Sym	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
	Page Buffer Word Write Time	2		2.2		µs	
t_{WHQV1} t_{EHQV1}	Word/Byte Write Time	2		9 µs	3 mS		
t_{WHQV2} t_{EHQV2}	Block Write Time	2		0.6	2.1	sec	Byte Write Mode
	Block Erase Time	2		0.8	10	sec	
	Full Chip Erase Time	2		51.2		sec	

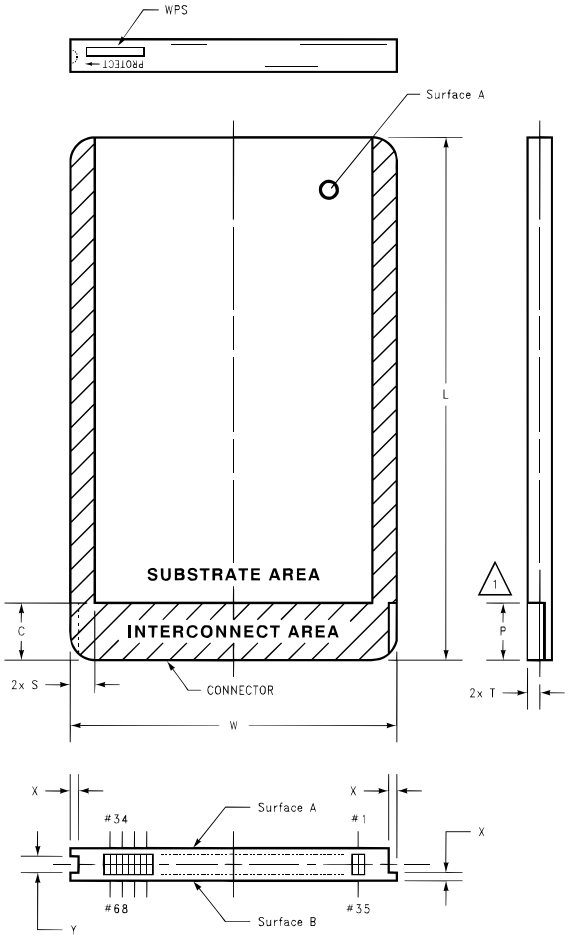
V_{CC} = 5.0 V ± 0.5 V, T_A = 0 °C to +70 °C

Sym	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
	Page Buffer Word Write Time	2		2.1		µs	
t_{WHQV1} t_{EHQV1}	Word Byte/Write Time	2,4		6 µs	3 mS		
t_{WHQV2} t_{EHQV2}	Block Write Time	2		0.4	2.1	sec	Byte Write Mode
	Block Erase Time	2		0.6	10	sec	
	Full Chip Erase Time	2		38.4		sec	

NOTES:

1. 25 °C, and normal voltages.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. To maximize system performance, the RDY/BSY# signal should be polled instead of using the maximum word/byte write time as a delay timer.
   The maximum word/byte write time is the absolute maximum time it takes the write algorithm to complete. The overwhelming majority of the bits program in the typical value specified.

9.0 PACKAGING



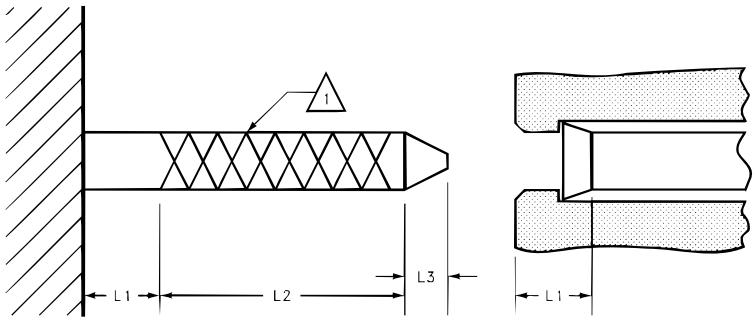
C MIN	L ± 0.008	P MIN 1	S MIN	T 2	W ± 0.004	X ± 0.002	Y ± 0.002
0.294 (10.0)	3.370 (85.60)	0.394 (10.0)	0.118 (3.0)	0.065 (1.65)	2.126 (54.0)	0.039 (1.00)	0.063 (1.60)

1 POLARIZATION KEY LENGTH.

2 INTERCONNECT AREA TOLERANCE = ±0.002
SUBSTRATE AREA TOLERANCE = ±0.004

3 MILLIMETERS ARE IN PARENTHESIS ().

049106.eps



PIN SOCKET CONTACT

1. PIN/SOCKET CONTACT AREA
2. MILLIMETERS ARE IN PARENTHESIS ()

049107.eps

10.0 ORDERING INFORMATION

iMC020FLSP,SBXXXXX

WHERE:

i	= INTEL
MC	= MEMORY CARD
020	= DENSITY IN MEGABYTES (004,020 AVAILABLE)
FL	= FLASH TECHNOLOGY
S	= BLOCKED ARCHITECTURE
P	= PERFORMANCE
SBXXXXX	= CUSTOMER IDENTIFIER

11.0 ADDITIONAL INFORMATION

Order Number	Document
290434	*Series 2 Flash Memory Cards* Datasheet
297373	*Series 2+ Flash Memory Card User's Manual*
290489	*28F016SA 16-Mbit (1 Mb x 16, 2 Mb x 8) FlashFile™ Memory* Datasheet
290429	*28F008SA 8-Mbit (1 Mb x 8) FlashFile™ Memory* Datasheet
292126	*AP-377 The 28F016SA Software Drivers*

NOTE:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.