

Dual Output Driver

Description

The CS-3706 integrated circuit provides an interface between low-level TTL inputs and high-power switching devices such as power MOSFETs. A typical application is single-ended PWM control to push-pull power control conversion.

The primary function of this device is to convert a bipolar single-ended low current digital input to a pair of totem pole outputs which can

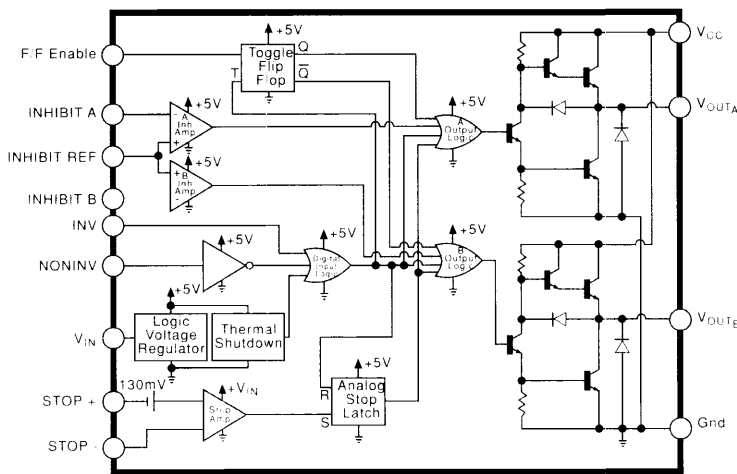
source or sink up to 1.5A. An internal flip-flop, driven by double-pulse suppression logic, can be enabled to provide single-ended to push-pull conversion. With the flip-flop disabled, the outputs work in parallel for 3.0A capability.

Protection functions are also included for pulse-by-pulse current limiting, automatic deadband control and thermal shutdown.

Features

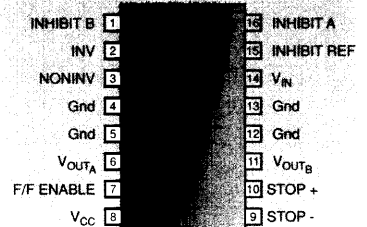
- Single-Ended PWM Control to Push-Pull Conversion
- Push-Pull Conversion to Parallel Conversion
- High-Power Transistors, MOSFET Compatible
- Low-Cross-Conduction Current Spike
- Analog Latched Shutdown
- Internal Deadband Control Circuit
- Low Quiescent Current
- 5V to 49V Operation
- Thermal Shutdown Protection

Block Diagram



Package Options

16 Lead PDIP



Note: All Four Ground Pins must be Connected to Common Ground.

Logic Supply Voltage (V_{DD})	40.0V
Output Supply Voltage (V_C)	40.0V
Output Current (each output, source, or sink)	
Steady State	±500mA
Peak Transient for Less Than 100us	±1.5A
Capacitive Discharge Energy	20.0μJ
Digital Inputs (INV, NONINV)	5.5V
Analog Inputs (STOP +, STOP -)	V_{IN} V
Inhibit Inputs (INHIBIT A, INHIBIT B, INHIBIT REF)	5.5V
Operating Temperature Range	0 to 70°C
Storage Temperature Range	-65 to 150°C
Lead Temperature Soldering	
Wave Solder(through hole styles only)	10 sec. max, 260°C peak

Notes: All voltages are with respect to the four ground pins which must be connected together. All currents are positive into, negative out of the specified terminal.

Parameter	Conditions	8	12	mA
V_{IN} Supply Current	$V_{IN}=40V, V_{CC}=20V, INV=0V,$ Unused pins=open.	8	12	mA
V_{CC} Leakage Current	$V_{IN}=0V, V_C=40V$	0.05	0.10	mA
Digital Input High Level		2.2		V
Digital Input Leakage	$V_I=5V$	0.05	0.10	mA
Output High Sat., V_C-V_{OUT}	$I_{OUT}=-500mA$		2.5	V
Output Low Sat., V_{OUT}	$I_{OUT}=500mA$		2.5	V
Inhibit Threshold	$V_{REF}=3.5V$	3.3	3.7	V
Analog Threshold	$V_{CM}=0V$ to 15 V	100	130	150
Thermal Shutdown	Turn on	155		°C
Thermal Shutdown	Turn off			°C

From Inv. Input to Output:	open	1.0	2.2	nF
Rise Time Delay	110	130	140	ns
10% to 90% Rise	20	40	60	ns
Fall Time Delay	80	90	110	ns
90% to 10% Fall	25	30	50	ns

V_C Cross-Conduction	Output Rise	25		ns
Current Spike Duration	Output Fall	0		ns

Analog Shutdown Delay	Stop (+) Ref. = 0 Stop (-) Input = 0 to 0.5V	180		ns
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Outputs

The totem-pole outputs have been designed to minimize cross-conduction current spikes while maximizing fast, high-current rise and fall times. Current limiting can be done externally either at the outputs or at the common V_C pin. The output diodes included have slow recovery and should be shunted with high-speed external diodes when driving high-frequency inductive loads.

Flip/Flop

Grounding F/F Enable activates the internal flip-flop to alternate the two outputs. With pin open, the two outputs operate simultaneously and can be paralleled for higher current operation. Since the flip-flop is triggered by the digital input, an off-time of at least 200nsec. must be provided to allow the flip/flop to change states. Note that the circuit logic is configured such that the "OFF" state is defined as the outputs low.

Digital Inputs

With both an inverting and non-inverting input available, either active-high or active-low signals may be accepted. These are true TTL compatible inputs—the threshold is approximately 1.2V with no hysteresis; and external pull-up resistors are not required.

Inhibit Circuit

Although it may have other uses, this circuit is included to eliminate the need for deadband control when driving relatively slow bipolar power transistors. A diode from each inhibit input to the opposite power switch collector will keep one output from turning on until the other has turned-off. The threshold is determined by the voltage on INHIBIT REF which can be set from 0.5 to 3.5 V. When this circuit is not used, ground INHIBIT REF and leave INHIBIT A&B open.

Analog Shutdown

This circuit is included to get a latched shutdown as close to the outputs as possible, from a time standpoint. With an internal 130mV threshold, this comparator has a common-mode range from ground to ($V_{IN} - 3V$). When not used, both inputs should be grounded. The time required for this circuit to latch is inversely proportional to the amount of overdrive but reaches a minimum of 180nsec. As with the flip-flop, an input off-time of at least 200nsec is required to reset the latch between pulses.

Supply Voltage

With an internal 5V regulator, this circuit is optimized for use with a 7 to 40V supply, however, with some slight response time degradation, it can also be driven from 5V. When V_{IN} is low, the entire circuit is disabled and no current is drawn from V_{CC} . When combined with a CS-384X PWM, the Driver Bias switch can be used to supply V_{IN} to the CS-3706. V_{IN} switching should be fast as undefined operation of the outputs may occur with V_{IN} less than 5V.

Thermal Considerations

Should the chip temperature reach approximately 155°C, a parallel, non-inverting input is activated driving both outputs to the low state.

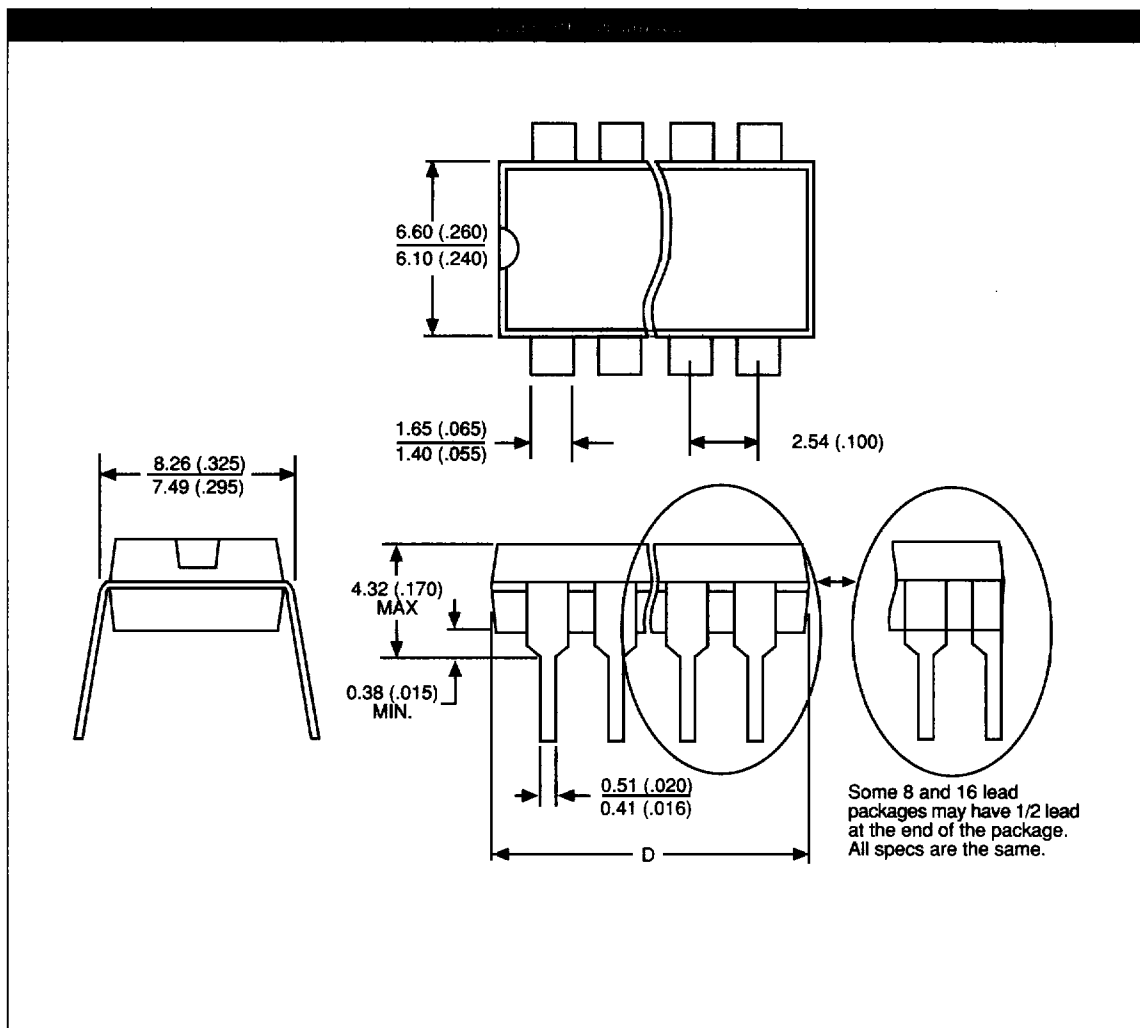
Truth Table

INV.	N.I.	OUT
H	H	L
L	H	H
H	L	L
L	L	L

$\overline{OUT} = \overline{INV}$ and N.I.
 $\overline{OUT} = INV$ or N.I.

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16L PDIP	19.18	18.92	.755	.745

Thermal Data		16L PDIP	
$R_{\theta JC}$	typ	15	$^{\circ}C/W$
$R_{\theta JA}$	typ	50	$^{\circ}C/W$



Part Number	Description
CS-3706N16	16L Plastic Batwing DIP