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MV1445

COMBINED PCM HDB3 DECODER, DIGITAL CLOCK REGENERATOR AND TIMESLOT ZERO RECEIVER

The MV1445 combines the HDB3 Decoder, Digital Clock Regnerator and Timeslot Zero Receiver functions required by a 2.048Mbit 30 channel PCM transmission link operating in accordance with the appropriate CCITT Recommendations and forms part of the GPS 2Mbit PCM signalling series of devices. The circuit is fabricated in CMOS and operates from a single +5V supply.

The HDB3 Decoder section of the MV1445 is responsible for decoding the incoming 2.048Mbit HDB3 encoded pseudo-ternary PCM data stream back into NRZ binary form. This decoding is carried out in accordance with Annex A to CCITT Recommendation G.703.

In order to perform this process, the HDB3 Decoder requires a 2.048MHz clock signal to be recovered from the incoming HDB3 data stream. This clock regeneration may be carried out externally using a tuned circuit or internally using the on-chip Digital Clock Regenerator. This digital clock regenerator circuit continuously re-synchronises a divide-by-8 counter being clocked at 16.384MHz to the incoming HDB3 data stream and performs in accordance with the tolerance to input jitter specification of CCITT Recommendation G.823.

The Timeslot Zero Receiver function searches for the CCITT Frame Alignment signal in the NRZ data stream being output by the HDB3 Decoder and when this pattern is detected the receiver synchronises itself to it in accordance with the Frame Alignment strategy detailed in CCITT Recommendation G.732. Once frame alignment has been achieved the Timeslot Zero Receiver produces various timing outputs for the use of external circuitry and extracts the user data bits of timeslot zero.

FEATURES

- Single +5V supply.
- All Inputs and Outputs TTL compatible.
- HDB3 Decoding carried out in accordance with CCITT Recommendation G.703.
- Provides HDB3 Error Monitor, Loss of Input Alarm and AIS Monitor.
- On-chip digital clock regenerator operates in accordance with tolerance to input jitter specification of CCITT Recommendation G.823.
- Receiver Frame Synchronisation carried out in accordance with CCITT Recommendation G.732.
- Provides Alarm Outputs for Reception of Corrupted Alignment word and Loss of Frame Alignment.
- Extracts the International Spare Bits from Alternate Frames or from Frames 13 and 15 of the CCITT CRC-4 multiframe.

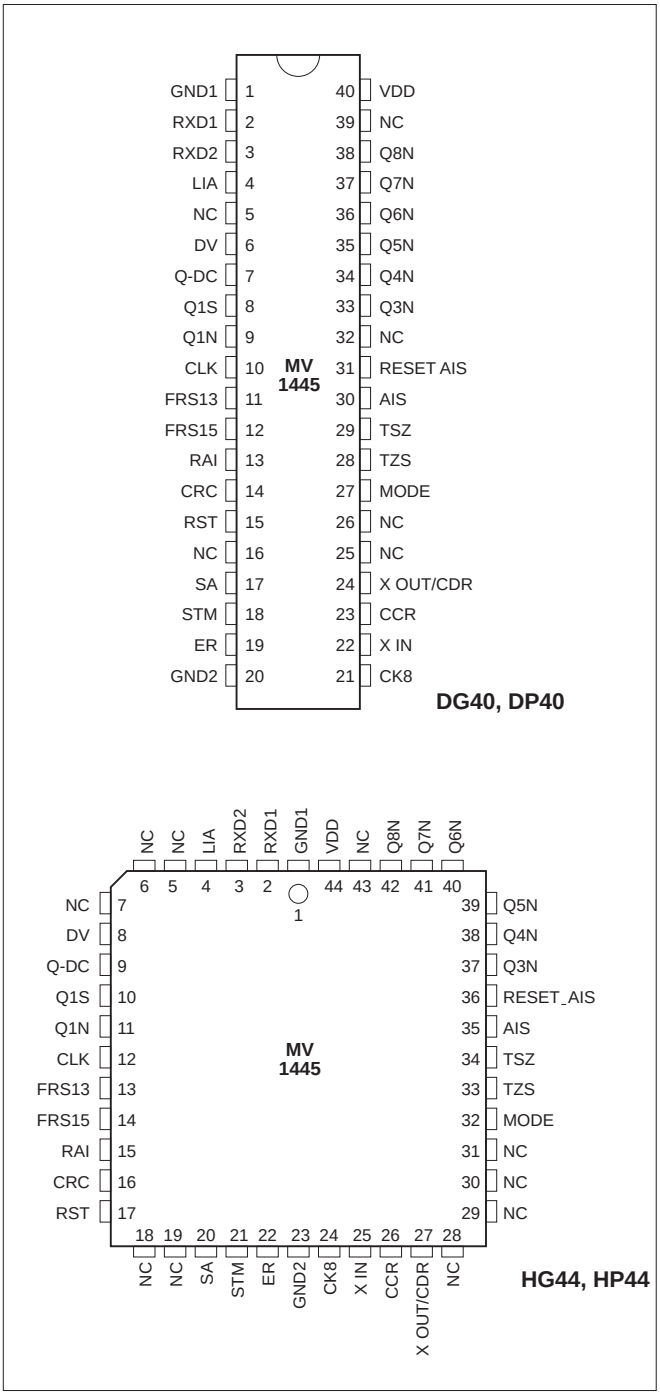


Fig. 1 Pin connections - top view

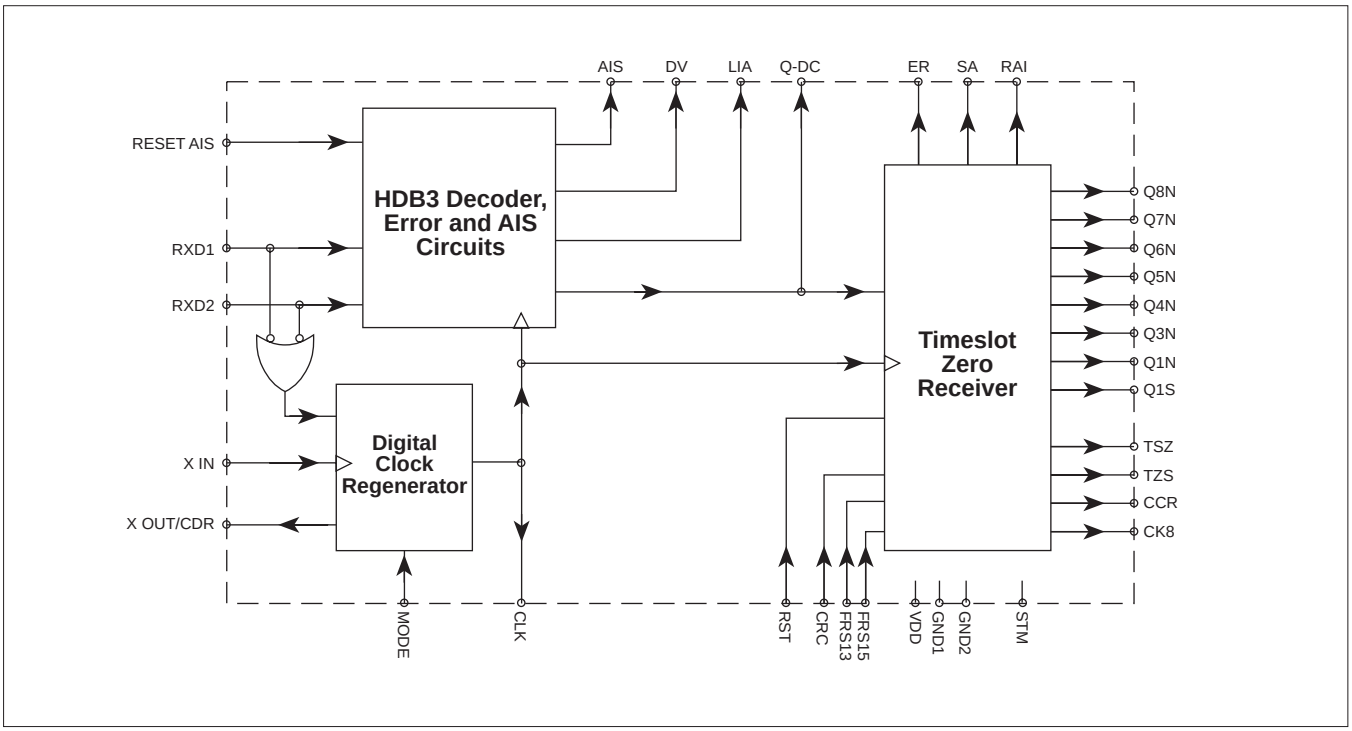


Fig. 2 Block diagram

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

ELECTRICAL RATINGS

Supply Voltage	-0.5V to +7V
Input Voltage	-0.5V to VDD +0.5V
Output Voltage	-0.5V to VDD +0.5V

FUNCTIONAL DESCRIPTION

The MV1445 combines the HDB3 Decoder, Digital Clock Regenerator and Timeslot Zero Receiver functions required by a 2.048Mbit 30 channel PCM transmission link operating in accordance with the appropriate CCITT Recommendations. The block diagram of the MV1445 is shown in Fig.2 and the function of each block is now described separately.

HDB3 Decoder

The HDB3 decoder circuit is responsible for converting the 2.048Mbit HDB3 encoded pseudo-ternary PCM data stream on its inputs, RXD1 and RXD2, back in to NRZ binary form to be output to external circuitry and the Timeslot Zero Receiver. This conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G.703, Annex A.

High Density Bipolar 3 (HDB3) is a ternary transmission code in which the number of consecutive zeros which may occur is restricted to three, to ensure adequate clock recovery at the receiver. In any sequence of four consecutive binary zeroes, the last zero is substituted by a mark of the same polarity of the previous mark, thus breaking the Alternate Mark Inversion (AMI) code. This mark is termed a violation. In addition, the first zero may also be substituted by a mark if the last mark and last violation are of the same polarity. This mark does not violate the AMI code and ensures that successive violations alternate in polarity and as such introduce no DC component to the HDB3 signal.

The HDB3 Decoder synchronously decodes the data on its RXD input pins into NRZ form under control of a 2.048MHz system clock. There is a 5 clock period delay between the HDB3 data being clocked in from the RXD inputs and the NRZ data appearing on the Q-DC output. In addition to the basic HDB3 decoding the circuit also provides three alarm outputs. The first of these alarms is DV (Double Violation) and a logic high on this output denotes that two successive violations have been received with the same polarity, thus violating the HDB3 decoding laws. The second alarm, LIA (Loss of Input Alarm), is used to denote that 11 consecutive zeroes have been received on the RXD inputs. The third alarm output is AIS (Alarm Indication Signal). This output will go high if less than 3 decoded zeros have been detected in the preceding RESET AIS=1 period (i.e. between RESET AIS=0 pulses) and as such this alarm can be used to detect the CCITT Alarm Indication Signal. The timing diagrams of the HDB3 Decoder circuit are shown in Fig. 3.

Digital Clock Regenerator

In order to decode the incoming HDB3 data stream the HDB3 decoder requires a 2.048MHz clock to be recovered from the incoming data stream. This may either be produced externally using a tuned circuit or internally using the on-chip digital clock regenerator.

Selection between these 2 recovery modes is carried out by the MODE control pin, and with MODE high, internal clock recovery is selected.

When external clock recovery is selected, a logical 'OR' function of the inverted HDB3 inputs is output on the X OUT/ CDR pin for the use of the external clock recovery circuit. The 2.048MHz clock signal thus regenerated is then input back to the MV1445 on the CLK I/O pin.

In internal clock recovery mode, the digital clock regenerator requires either a 16.384MHz clock signal to be input to the X IN pin or a 16.384MHz crystal to be connected between pins X IN and X OUT/CDR. The 16.384MHz clock signal thus produced is used to clock a divide-by-8 counter to produce the recovered 2.048MHz system clock. This counter is continuously re-synchronised to the incoming data stream and attempts to choose the 16.384MHz clock edge furthest from the falling edge of either of the RXD inputs to use as the rising edge of the 2MHz recovered clock, giving the highest tolerance to incoming jitter. This circuit performs in full compliance with the tolerance to input jitter specification of CCITT Recommendation G.823. The regenerated clock thus produced is input to the HDB3 Decoder and Timeslot Zero Receiver circuits and is also output to external circuitry on the CLK I/O pin.

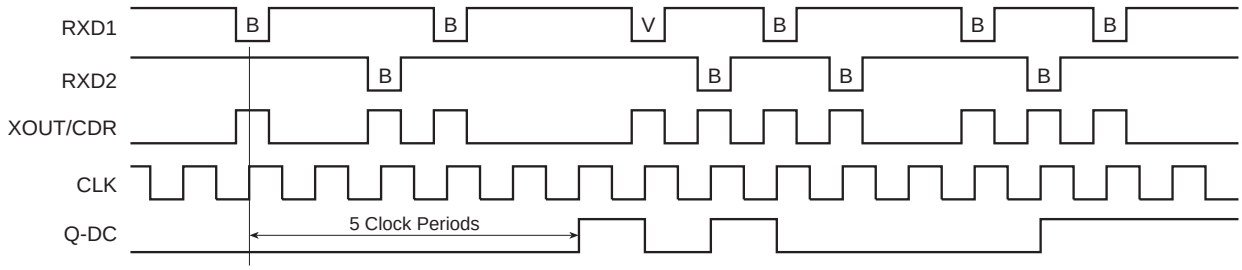
Timeslot Zero Receiver

The Timeslot Zero Receiver circuit is responsible for searching for and locking on to the CCITT Frame Alignment Signal present in timeslot zero of the NRZ PCM data stream being decoded by the HDB3 Decoder. This process is carried out in accordance with the loss and recovery of frame alignment strategy described in CCITT Recommendation G.732. Once frame alignment has been achieved the Timeslot Zero Receiver circuit outputs various timing reference signals for the synchronisation of external circuitry. These timing outputs will all free run if frame synchronisation is subsequently lost. In addition, a control input, RST, may be used to reset this synchronisation process, forcing the receiver out of frame alignment.

The Timeslot Zero Receiver circuit produces 4 timing outputs for use by external circuitry if required. The first of these timing outputs is TSZ which is an 8 clock period long, high going pulse masking the position of timeslot zero and facilitates the frame alignment of external circuitry. The second timing output, TZS, is a 4KHz signal which changes state once per frame, one clock period after the end of timeslot zero, and is high during sync frames to allow sync and non-sync frames to be distinguished. The third timing output, CCR, is a low going pulse, one clock period wide, occurring during bit 1, timeslot 1 of sync frames. The final timing output, CK8, is an 8KHz signal going low at the end of bit 7 of each timeslot zero and high at the end of bit 7 in each timeslot 16.

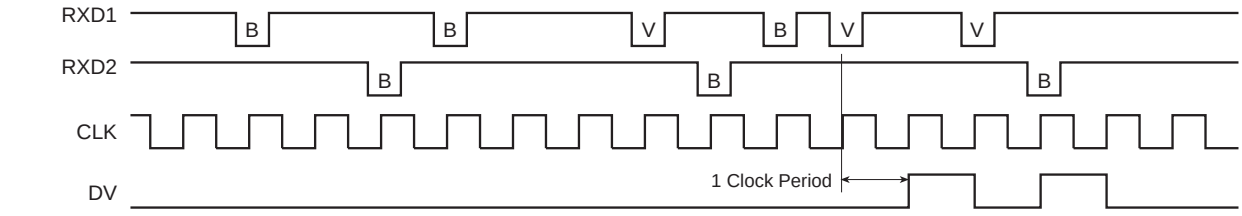
In addition to these timing outputs, two alarm outputs are provided to indicate errors in the incoming data stream. The first of these alarms, ER, goes high for one frame following a sync frame in which a corrupted FAS was detected when the receiver is in sync. Three consecutive alarms of this type will put the receiver out of sync. The second alarm, SA, goes high to indicate that the Timeslot Zero Receiver is out of frame alignment.

In addition to the frame synchronisation process, the Timeslot Zero Receiver is also responsible for extracting the user data bits of non-sync words and the two International / CRC bits of timeslot zero. The user data bits present in bits 3 to 8 of timeslot zero of non-sync frames are extracted and output on the Q3N-Q8N parallel data outputs. The third bit of non-sync words, Q3N, is used as the remote alarm bit in 2Mbit PCM systems and a third alarm output, RAI, is derived from this bit. This alarm is a persistence checked version of Q3N which goes high when two consecutive Q3N bits have been received high whilst the receiver is in sync. The Timeslot Zero Receiver also extracts the data present in bit 1 of timeslot zero under control of the CRC input. This input selects between CCITT CRC-4 and non-CRC-4 modes of operation. In non-CRC-4 mode, the international spare bits are extracted from bit 1 of all sync and non-sync frames and output on pins Q1S and Q1N respectively. In CRC-4 mode, these data outputs are extracted from bit 1 of frames 13 and 15 of the CCITT CRC-4 multiframe structure respectively. In order to accomplish this, two timing inputs, FRS13 and FRS15, are required in CRC-4 mode. These inputs are required to be high during bit 8 of the appropriate frame, low during bit 8 of any other non-sync frame and any state elsewhere. The timing diagrams for the Timeslot Zero Receiver are shown in Fig.4.



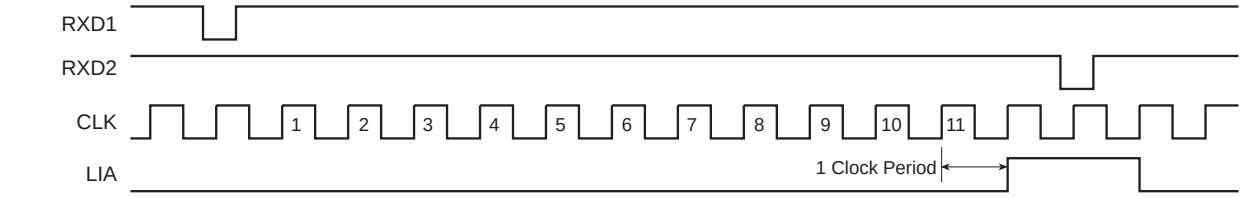
Notes:- 1) The Decoded NRZ output is delayed by 5 clock periods with respect to the HDB3 inputs.
2) The diagram assumes the last violation occured on RXD2.
3) B is HDB3 mark, V is a HDB3 violation.

Decoder waveforms



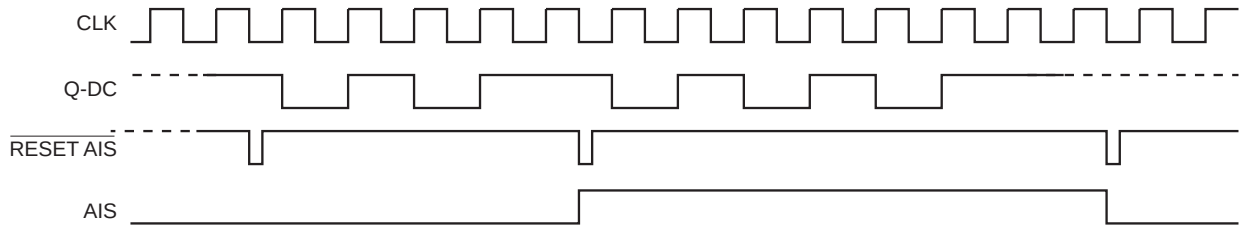
Notes:- 1)There is a single period delay between detection of an error and the rising edge of DOUBLE VIOLATION
2) The diagram assumes the last violation occured on RXD2.
3) B is HDB3 mark, V is a HDB3 violation.

HDB3 Double violation waveforms



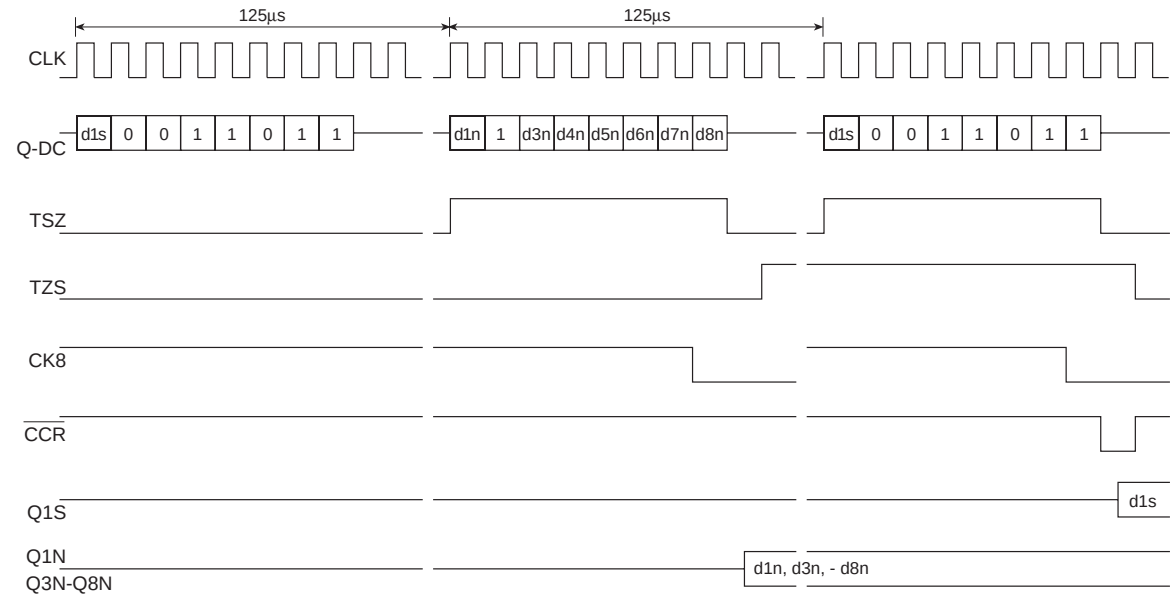
Note:- 1)The 'LOSS OF INPUT' is delayed by a single clock period with respect to the incoming HDB3 waveforms.

Loss of input violations

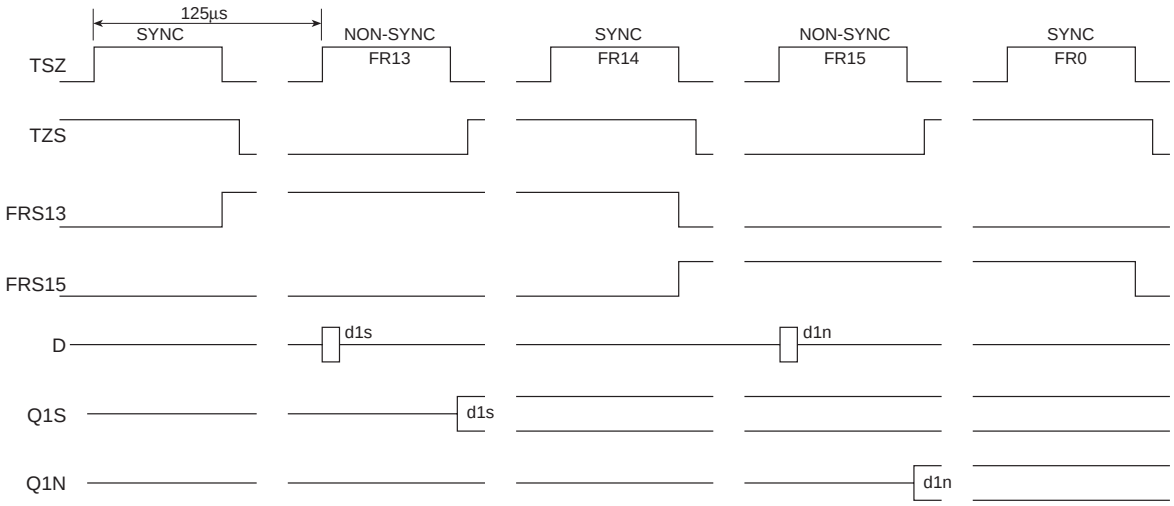


AIS and $\overline{\text{RESET AIS}}$ waveforms

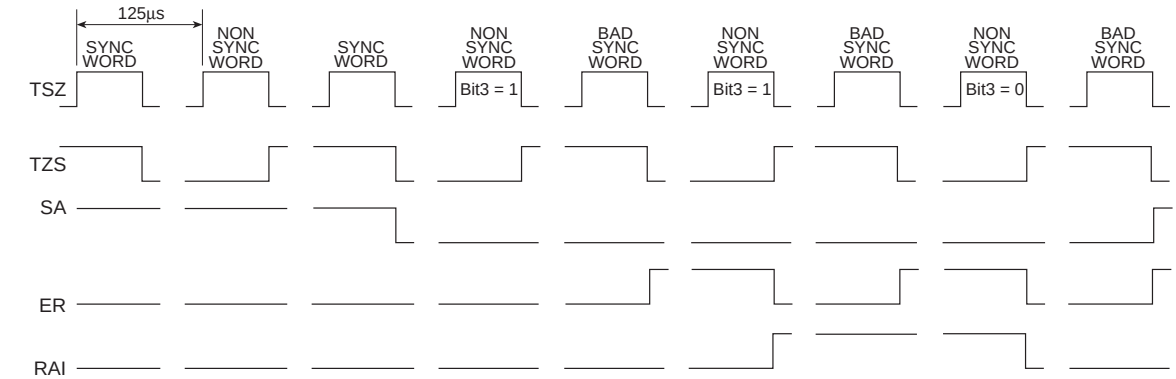
Fig. 3 HDB3 Decoder timing



Timeslot Zero Receiver first coming into sync., generating timing signals (non-CRC mode)



Timeslot Zero Receiver extracting Signalling Data (CRC mode)



Timeslot Zero Receiver synchronisation process

Fig. 4 Timeslot zero receiver timing

PIN DESCRIPTIONS

Pin name	Pin no.		Pin description
	DG40	HG44	
GND1	1	1	Digital Ground. OV (Note 1)
RXD1	2	2	HDB3 Encoded Input 1 to HDB3 Decoder. This is one of the pair of 2.048Mbit pseudo-ternary HDB3 encoded PCM data stream inputs to the HDB3 Decoder. This input asynchronously latches the incoming HDB3 data and is falling edge sensitive. Since the input is asynchronously latched it is not necessary for the RXD pulse to straddle a rising clock edge.
RXD2	3	3	HDB3 Encoded Input 2 to HDB3 Decoder. See description for pin RXD1.
LIA	4	4	Loss of Input Alarm Output from HDB3 Decoder. This output goes high one period after the detection of 11 consecutive zeroes on the RXD inputs. Any HDB3 mark on the inputs (RXD1 or RXD2=0) resets this output low after a single clock period delay.
DV	6	8	Double Violation Alarm Output from HDB3 Decoder. This output goes high for one period of CLK, one period after the detection of a HDB3 violation of the same polarity as the previous HDB3 violation.
Q-DC	7	9	NRZ Data Output from HDB3 Decoder. This output represents the HDB3 input data decoded back in to NRZ binary form, with a 5 clock period delay from the HDB3 inputs to the NRZ output. The 2.048Mbit PCM data stream on this pin is also input to the Timeslot Zero Receiver.
Q1S	8	10	International / CRC Data Bit Output of Timeslot Zero Receiver for Sync Frames. With CRC=0, this output latches data from bit 1, timeslot zero of sync frames. With CRC=1, this output latches data from bit 1, timeslot zero of frame 13 of the CRC-4 multiframe, under control of the FRS13 input. In either case this output changes state on the falling edge of CLK, half a clock period after the end of timeslot zero.
Q1N	9	11	International / CRC Data Bit Output of Timeslot Zero Receiver for Non-sync Frames. With CRC=0, this output latches data from bit 1, timeslot zero of non-sync frames. With CRC=1, this output latches data from bit1, timeslot zero of frame 15 of the CRC-4 multiframe, under control of the FRS15 input. In either case this output changes state on the faliing edge of CLK, half a clock period after the end of timeslot zero.
CLK	10	12	2.048MHz System Clock I/O pin. In Internal Clock Regeneration mode (MODE=1), this pin is used to output the internally recovered 2.048MHz clock signal to external circuitry. In external clock regeneration mode (MODE=0), this pin is used to input the externally regenerated clock signal to the HDB3 Decoder and Timeslot Zero Receiver blocks.

PIN DESCRIPTIONS (continued)

Pin name	Pin no.		Pin description
	DG40	HG44	
FRS13	11	13	Frame 13 Marker Input to Timeslot Zero Receiver. This input is used by the Timeslot Zero Receiver operating in CRC-4 mode to reference the position of Frame 13. This input is required to be high during bit 8, Frame 13 of the CRC multiframe and low during bit 8 of all other non-sync frames.
FRS15	12	14	Frame 15 Marker Input to Timeslot Zero Receiver. This input is used by the Timeslot Zero Receiver operating in CRC-4 mode to reference the position of Frame 15. This input is required to be high during bit 8, Frame 15 of the CRC multiframe and low during bit 8 of all other non-sync frames.
RAI	13	15	Remote Alarm Indication Output of Timeslot Zero Receiver. This alarm output is a persistence checked version of the Q3N output. When the receiver is in sync this output will go high if 2 consecutive Q3N bits are received high. This output changes state at the beginning of bit 1, timeslot 1 of non sync frames. When the receiver is out of sync this output is forced low in the non-sync frame following the last bad sync frame, and is held low until the receiver comes back in to sync.
CRC	14	16	CRC-4 Mode Select Input to Timeslot Zero Receiver. This input is used to control the extraction of the Q1N and Q1S data outputs from the incoming PCM data stream. A logic high on this input selects CRC-4 mode of operation.
RST	15	17	Reset Input to Timeslot Zero Receiver. A logic high on this pin straddling a falling edge of CLK will reset the state machine of the Timeslot Zero Receiver, forcing it out of frame alignment.
SA	17	20	Synchronisation Alarm Output from Timeslot Zero Receiver. This output is high whenever the receiver is out of sync and only changes state at the beginning of bit 1, timeslot 1 of sync frames.
STM	18	21	Scan Path Test Global Mode Pin. A logic high on this pin configures the MV1445 in scan test mode. For normal operation this pin should be tied low.
ER	19	22	Sync Word Error Output of Timeslot Zero Receiver. This alarm output goes high for one frame immediately after detection of a bad timeslot zero frame alignment signal, whilst the receiver is in sync. Three consecutive errors of this type will put the receiver out of sync and the last ER pulse of this sequence will be longer than 256 periods if a valid sync word is detected during the pulse.
GND2	20	23	Digital Ground. OV (Note 1)
CK8	21	24	8KHz Clock Output from Timeslot Zero Receiver. This output goes low at the beginning of bit 8, timeslot 0 and high at the beginning of bit 8, timeslot 16.

PIN DESCRIPTIONS (continued)

Pin name	Pin no.		Pin description
	DG40	HG44	
X IN	22	25	Crystal Amplifier Input of Digital Clock Regenerator Circuit. In Internal clock recovery mode this pin forms the input to the crystal oscillator circuit, used in conjunction with the X OUT/CDR pin. Alternatively, this pin may be used as a 16.384Mhz clock input to the internal clock regenerator if one oscillator is shared between several devices. This pin has no function when external clock recovery is selected and should be tied to GND.
CCR	23	26	Channel Reset Timing Output from Timeslot Zero Receiver. This output pulses low for a single period during bit 1, timeslot 1 of sync frames.
X OUT/ CDR	24	27	Crystal Amplifier/Clock Regenerate output from Digital Clock Regenerator. In internal clock recovery mode, this pin is used as the 16.384MHz output of the crystal oscillator circuit and is not used if an externally generated 16.384Mhz clock is used. In external clock recovery mode, this pin is used to output the logical 'OR' function of the inverted HDB3 inputs for the use of the external clock recovery circuit.
MODE	27	32	Clock Recovery Mode Select Input. This input is used to select between internal and external clock recovery modes. A logic high on this input selects internal clock regeneration.
TZS	28	33	Timeslot Zero Sync Frame Output from Timeslot Zero Receiver. This 4KHz output changes state at the end of bit 1, timeslot 1 (Note 2) of every frame and is high during timeslot zero of sync frames.
TSZ	29	34	Timeslot Zero Marker Output from Timeslot Zero Receiver. This timing output goes high for the 8 clock periods of timeslot zero and is low at all other times
AIS	30	35	Alarm Indication Signal Output from HDB3 Decoder. See description for RESET AIS pin.
RESET AIS	31	36	Reset AIS Input to HDB3 Decoder. A logic '0' on this input resets a decoded zeros counter in the HDB3 Decoder. It will also reset the AIS output to '0' provided 3 or more zeros have been decoded in the preceding RESET AIS=1 period, or set AIS to '1' if less than 3 zeros have been decoded in the preceding RESET AIS=1 period. This may be used to detect the CCITT Alarm Indication Signal. A logic '1' on this pin enables the decoded zeros counter.
Q3N Q4N Q5N Q6N Q7N Q8N	33 34 35 36 37 38	37 38 39 40 41 42	User Data Bit Outputs of Timeslot Zero Receiver. These 6 parallel data outputs are extracted from bits 3-8 of timeslot zero during non-sync frames. These outputs change state on the falling edge of CLK half a clock period after the end of timeslot zero.
VDD	40	44	Digital Supply Voltage. 5V

NOTES

1. In order to facilitate adequate supply decoupling, both digital ground pins should be connected to 0V.

2. The bits of a timeslot are numbered from 1 to 8 whereas the timeslots of a frame are numbered from 0 to 31 and the frames of a CCITT multiframe are numbered from 0 to 15.

3. All inputs except X IN have 100K on-chip pull down resistors. The X IN pin has neither pull-up nor pull-down resistor to allow operation as a crystal oscillator and should be tied to digital ground if external clock regeneration is selected.

ELECTRICAL CHARACTERISTICS

Test Conditions:

Supply Voltage VDD = 5V ± 0.5V Ambient Temperature T_{amb} = -40°C to +85°C

STATIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Low Level Input Voltage	V_{IL}	0.0		0.8	V	
High Level Input Voltage	V_{IH}	2.0		V_{DD}	V	
LOW Level Output Voltage	V_{OL}			0.4	V	Isink=2mA
High Level Output Voltage	V_{OHT} V_{OHC}	2.4 V_{DD}-1.0			V V	Isource=2mA Isource=lmA
Input Leakage Current	I_{IL}	-10		200	uA	$V_{IN} = V_{DD}$ or V_{SS}
Input Capacitance	C_{IN}		5		pF	All Inputs
Output Capacitance	C_{OUT}		5		pF	All Outputs

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
CLOCK						
Clock Period	t_{CP}	400			ns	See Fig. 5
Clock Rise/Fall Time	t_{CR}/t_{CF}			20	ns	See Fig. 5
Clock High/Low Time	t_{CH}/t_{CL}	150			ns	See Fig. 5
DECODER						
RXD1/2 Data Setup Time	t_{RS}	50			ns	See Fig. 6
RXD1/2 Pulse Width	t_{RW}	50			ns	See Fig. 6
CDR Propagation Delay	t_{CPDR}/ t_{CPDF}	50			ns	See Fig. 6, Notes 1 and 2.
Decoder Output Propagation Delay.	t_{OPD}	60			ns	See Fig. 6, Notes 1 and 3.
RESET AIS Hold-Off Time	t_{RAHO}	20			ns	See Fig. 6
RESET AIS Pulse Width	t_{RAW}	30			ns	See Fig. 6
Reset AIS Setup Time	t_{RAS}	20			ns	See Fig. 6
AIS Propagation Delay	t_{APD}			65	ns	See Fig. 6, Note 1.
RECEIVER						
Data / Control Setup Time	t_{DS}	50			ns	See Fig. 7, Note 4.
Data / Control Hold Time	t_{DH}	50			ns	See Fig. 7, Note 4.
Timing / Alarm Propagation Delay	t_{TAPD}			70	ns	See Fig. 7, Notes 1 and 5.
Data Outputs Propagation Delay	t_{DPD}			80	ns	See Fig. 7, Notes 1 and 6.

NOTES

1. All output propagation delays are measured with a 50pF load.
2. This parameter assumes external clock recovery is selected.
3. The t_{OPD} parameter applies to outputs Q-DC, LIA and DV, but does not apply to AIS.
4. The Timeslot Zero Receiver Data / Control setup and hold time parameters, t_{DS} and t_{DH}, apply to the following inputs: D, RST, FRS13 and FRS15.
5. The Timeslot Zero Receiver Timing / Alarm Output propagation delay parameter applies to the following outputs: TSZ, TZS, CCR, CK8, ER, SA and RAI.
6. The Timeslot Zero Receiver Data Output propagation delay parameter applies to the following outputs: QIS, QIN, Q3N, Q4N, Q5N, Q6N, Q7N and Q8N.

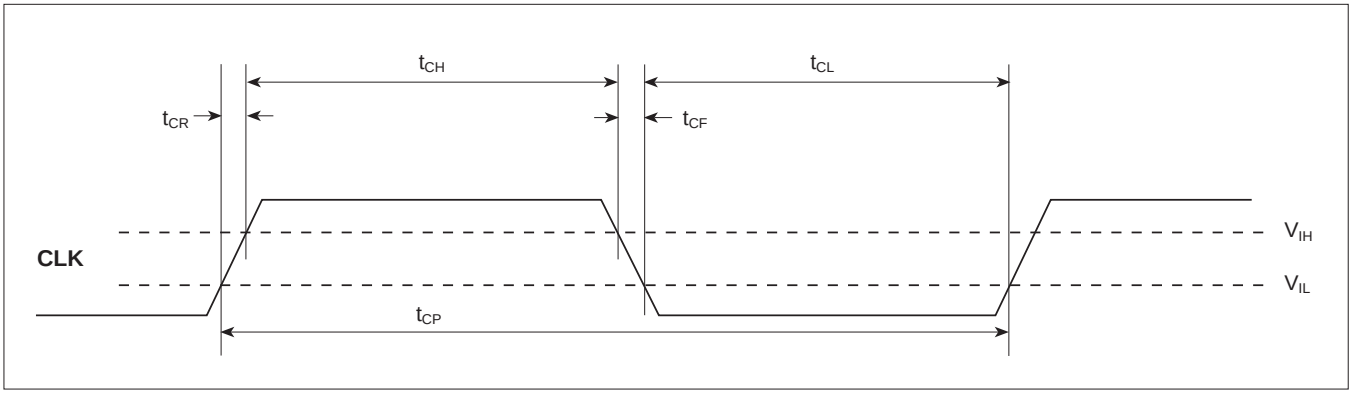


Fig. 5 Clock timing parameters

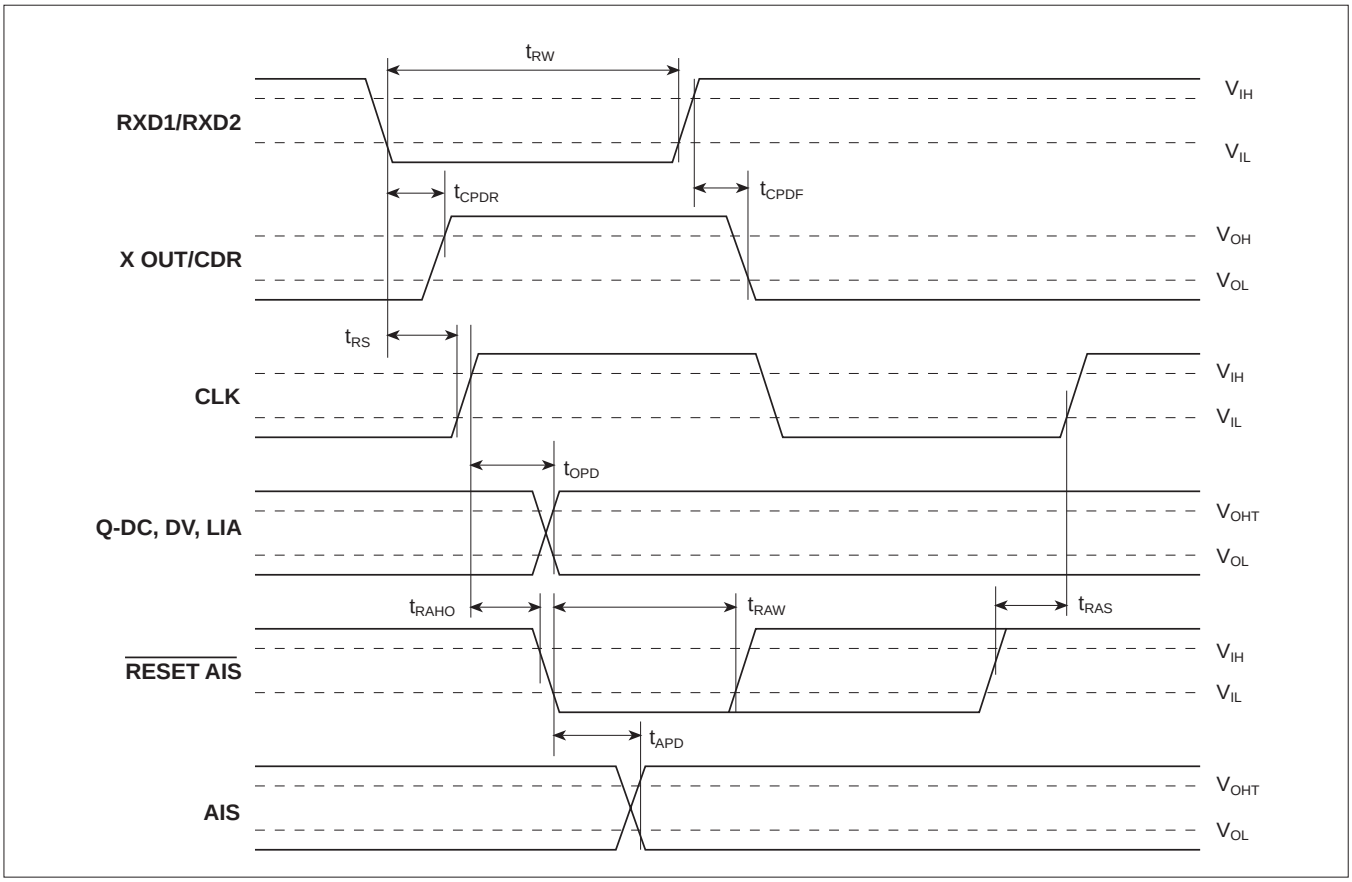


Fig. 6 HDB3 Decoder timing parameters

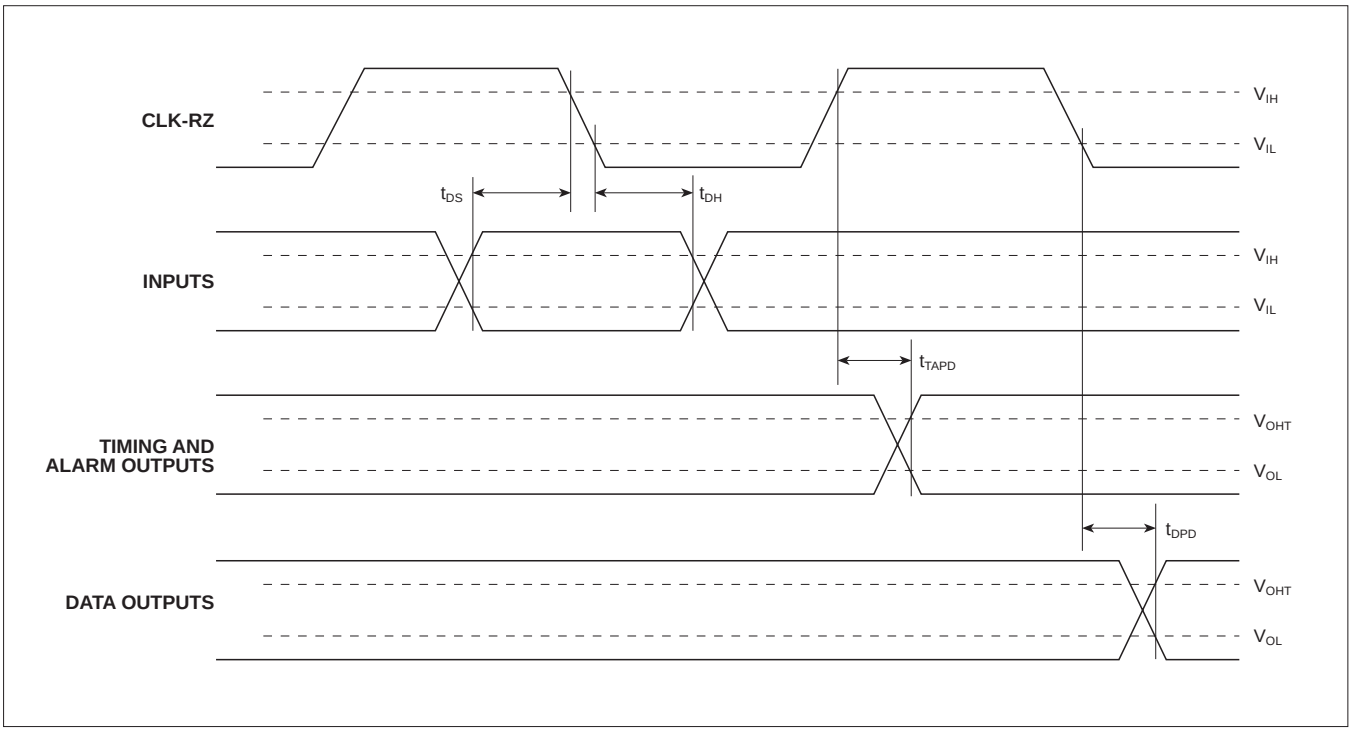


Fig. 7 Timeslot zero receiver timing

ORDERING INFORMATION

MV1445/IG/DGAS
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MV1445/IG/HPAS

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