MA31751

MEMORY MANAGEMENT UNIT & BLOCK PROTECTION UNIT

The GEC Plessey Semiconductors MA31751 Memory Management Unit / Block Protect Unit (MMU/BPU) is an optional chip which may be used to expand the capabilities of the MA31750 or the MAS281 CPU.

User configurable, the MA31751 can perform as an MMU, a BPU or both MMU and BPU, conforming to MIL-STD-1750A and 1750B. MMU mapping and BPU protection for 1M words of memory is provided by the internal memory. Up to 16 MA31751 devices can be used to give 16M words of logical mapped onto 8M words of physical address space with protection in 1750B mode.

The MA31751 is designed to have a simple interface to both the CPU and the system bus with the minimal number of control lines. This reduces board space and simplifies system design.

The MA31751 traps the MMU and BPU XIO commands to program and read the logical to physical mapping and memory access control. This provides simple memory management as defined by the MIL-STD-1750.

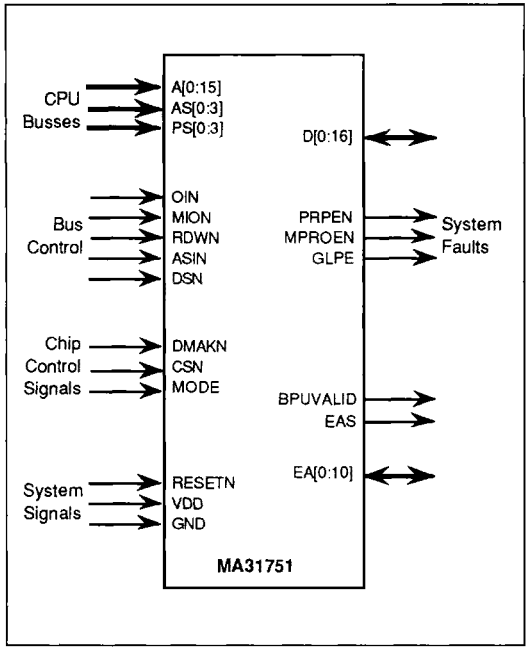


Figure 1: Chip Control Signals

FEATURES

- MIL-STD-1750A/B Compatible
- Radiation Hard CMOS/SOS Technology
- User Configurable as Either a Memory Management Unit (MMU) or a Block Protect Unit (BPU) or Both
- Memory Management Unit Configuration
  - 1 MWord Physical Address Space
  - Access Lock and Key of 4K-Word Blocks
  - Write/Execute Protection of 4K-Word Blocks
- Block Protect Unit Configuration
  - Protection of 1 K-Word Blocks
  - Global Memory Write Protection During Initialisation
- Direct Memory Access Support
- Full Support for the MAS281 Processor

1.0 DEVICE OPERATION

The MA31751 is an interface device designed to increase the memory addressing capability of the MA31750 or the MAS281 CPU. It is user configurable as an MMU and/or a BPU conforming to the MIL-STD-1750A and the proposed MIL-STD-1750B (MA31750 only). The MMU provides expanded addressing and full access lock/key protection in both modes, together with write/execute protection on 4K pages.

The BPU allows up to 1M words of memory to be protected in 1K blocks (MIL-STD-1750A). Up to 8M words may be protected by multiple MMU/BPU units (MA31750 only - draft MIL-STD-1750B).

In 1750A mode, one MA31751 unit can act as both MMU and BPU for the maximum 1M words of address space. In 1750B mode, up to 8 MA31751 units may be used to provide the maximum BPU functions and up to 16 units for the maximum MMU functions. For any given physical memory location the MMU and BPU function may be split across two MA31751 devices depending on the logical to physical address mapping.

1.1 INITIALISATION

The MA31751 is initialised by the CPU when a system reset occurs. Initially all mappings are set one to one to give a linear 1M word logical to physical mapping. The BPU defaults to no protection on a reset and requires 256 cycles to set the internal BPU memory. The CPU recognises the presence of the MMU/BPU by the setting of appropriate bits in the configuration register. When the configuration register is read, the MA31751 stores MMU, BPU, parity and 1750 mode information internally. The CPU may change the mapping and access protection when it is in privileged instruction mode using XIO commands 4D00 to 52FF as defined in MIL-STD-1750A.

1.2 ADDRESS TRANSLATION AND PROTECTION

The MMU maps system memory into 4K word pages by the mechanism shown in figure 3. A page is a block of physical memory which is uniquely specified by the physical page address, the PPA. A given address within any page is specified by the least significant 12 bits of the CPU address bus. One page register has the physical page address and the access control information relating to one page. There are 512 page registers, organized into 16 sets. The 16 sets are addressed by AS[0:3]. Each set has two groups of page registers, one for operand memory space and one for instruction memory space. These are addressed by OIN. Each group contains 16 page registers accommodating a total of 256 registers for each of operand and instruction memory space.

The MMU also checks for protection violation by comparing the processor state (PS), read from the CPU status word, with the access lock (AL) field in the page register. An additional bit in each page register allows the system to disable writes to operand pages or reads (execution) of instruction pages. If a violation occurs, the memory protect output is asserted. This typically causes a bus-fault-timeout on the processor which aborts the error cycle. Figure 2 illustrates the Access Key mapping mechanism. When memory transactions are controlled by the MA31750 or MAS281, the AS[0:3] and PS[0:3] bits necessary to perform the address translation and access protection functions respectively, are obtained from a copy of the processor status word held by the MMU. Modifications to the CPU status word are reflected in the MMU copy.

Figure 4 illustrates the standard way to map the logical CPU addresses, AS[0:3] and PB[0:3] onto the physical extended address bus for both 1750A (a 20-bit physical address) and for 1750B (a 23-bit physical address). Figure 5 shows the various selections to achieve the required memory size and protection.

AL Code	Acceptable Access Key Codes
0	0
1	0,1
2	0,2
3	0,3
4	0,4
5	0,5
6	0,6
7	0,7
8	0,8
9	0,9
A	0,A
B	0,B
C	0,C
D	0,D
E	0,E
F	0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F

Figure 2: Access Lock and Key Mapping

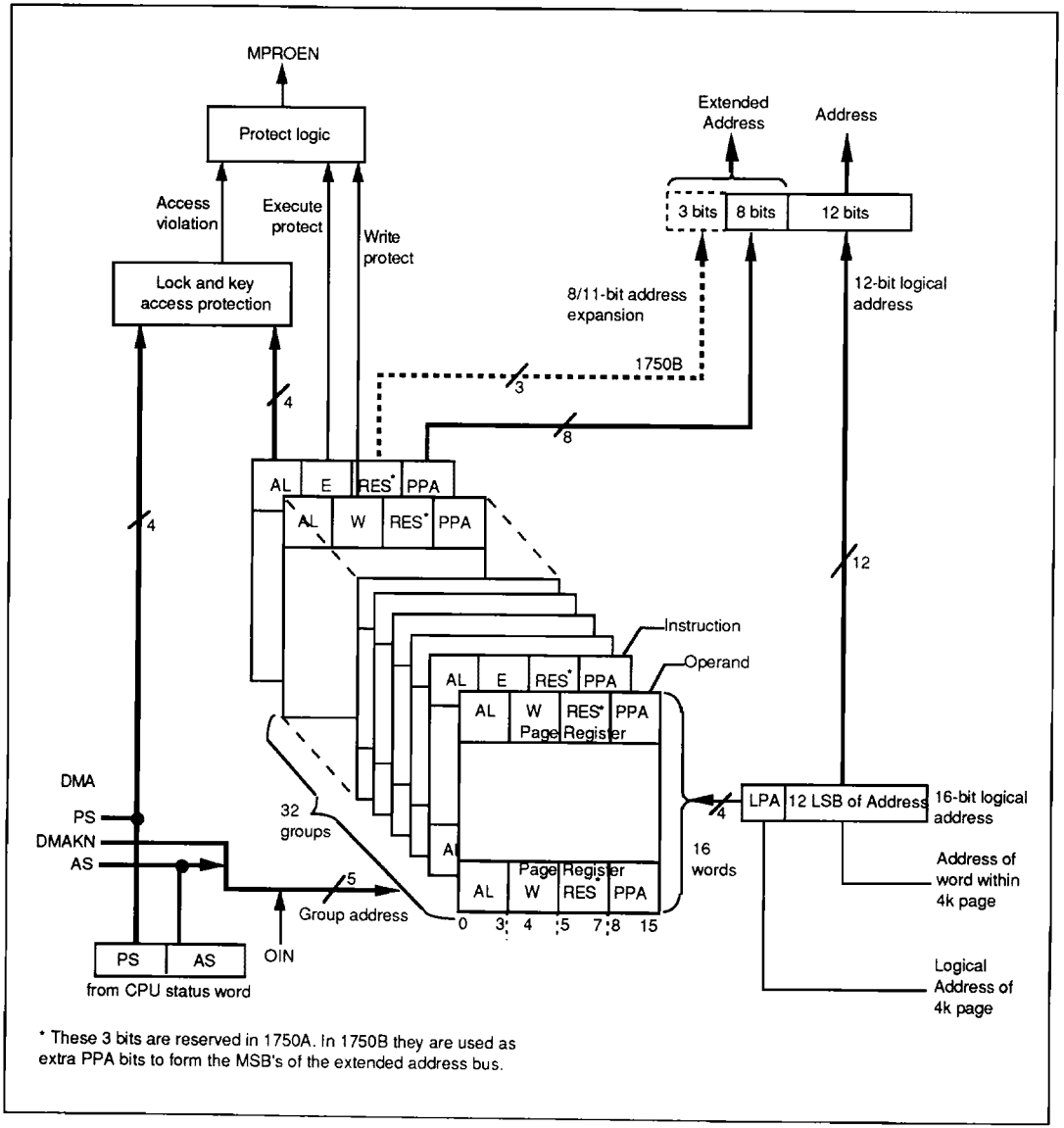
1.3 BLOCK PROTECTION

The BPU section of this device allows any 1Kword block to be write protected. The presence of a BPU in the system is determined from the CPU configuration word. Any attempt to write a protected block results in an access violation error from the BPU. If the BPU is protecting extended memory (i.e. there is an MMU in the system as well as a BPU), then the BPU cannot start its address decoding and memory access until EAS indicates that there is a valid extended address on the bus.

NOTE: MIL-STD-1750 states that the MSB of the Block Protect Register (BPR) should protect the least significant address block.

1.4 DIRECT MEMORY ACCESS

The MA31751 supports DMA access within the expanded memory space, including translation and protection .When a DMA controller is performing memory transactions, it must provide the AS[0:3] and PS[0:3] signals to the inputs of the MMU for address translation and access protection.



* These 3 bits are reserved in 1750A. In 1750B they are used as extra PPA bits to form the MSB's of the extended address bus.

Figure 3: MMU Memory Mapping Mechanism

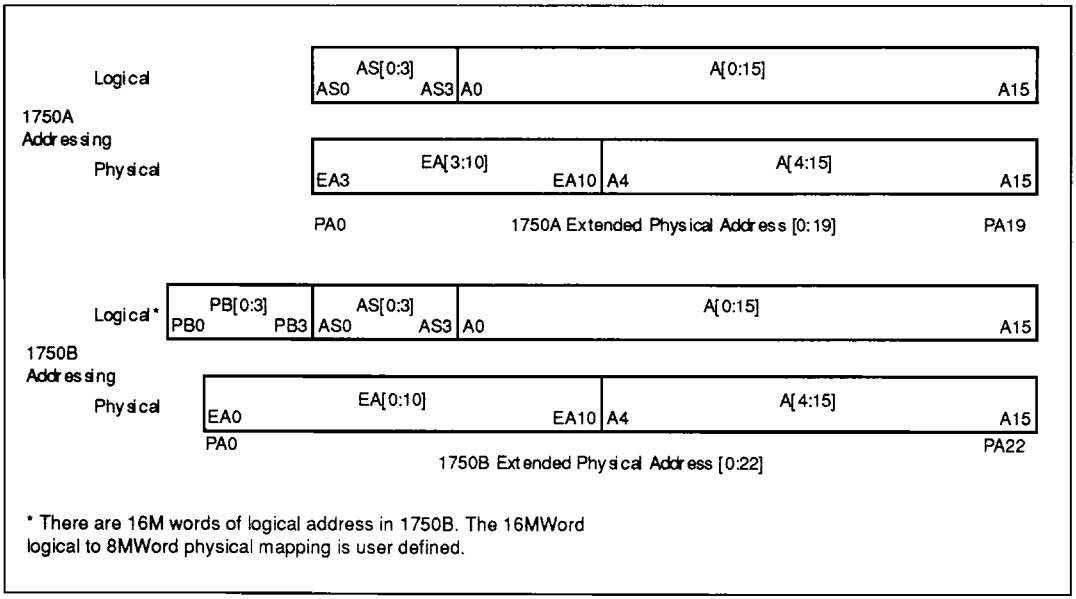


Figure 4: Extended Address Mapping in 1750A/B Mode

Addressable Physical Memory	Addressable Logical Memory	Is BPU Protection Required?	Mode	Number of MMUs	Number of BPUs	Number of MA31751s Required
64KW	64KW	NO	A	0	0	0
1MW	1MW	NO	A	1	0	1
64KW	64KW	YES	A	0	1	1
1MW	1MW	YES	A	1	1	1
64KW	64KW	NO	B	0	0	0
8MW	1MW	NO	B	1	0	1
8MW	2MW	NO	B	2	0	2
8MW	4MW	NO	B	4	0	4
8MW	8MW	NO	B	8	0	8
8MW	16MW	NO	B	16	0	16
64KW	64KW	YES	B	0	1	1
8MW	1MW	YES	B	1	8	8
8MW	2MW	YES	B	2	8	8
8MW	4MW	YES	B	4	8	8
8MW	8MW	YES	B	8	8	8
8MW	16MW	YES	B	16	8	16

Notes: 1. Memory is specified in terms of addressable instruction space.
2. It is assumed that the whole of the physical address space is used in 1750B - if this is not the case the number of MA31751 chips may be reduced.

Figure 5: MA31751 Selection Chart for Varying Memory Requirements

2.0 TIMING CONSIDERATIONS

2.1 MMU TIMINGS

To enable a fast page register look-up time, the MMU has two fast translation cache registers. These hold the address translation information on the 4K memory page which is currently being accessed. One cache register is for operand transfers and one for instruction transfers, as these often occur in different pages. The appropriate translation cache register is chosen by the operand / instruction (OIN) signal from the CPU. When either an instruction or an operand crosses a page boundary, one wait state may be added whilst the translation cache register is updated from internal memory. This system minimises the MMU overhead.

2.2 BPU TIMINGS

A similar caching system is employed in the BPU section of the MA31751 to allow more rapid detection of access violations. If the physical address crosses a 16K block boundary, then one wait state may be added.

Different combinations of cache hits and misses give different access times if the MA31751 is acting as both an MMU and a BPU. If the logical address (from the CPU) gives an MMU cache hit, the physical address is looked-up from the translation cache register (operand or instruction, depending on OIN). If the physical address gives a cache hit, the protection for the block is looked-up in the BPU cache register. This situation (both hits) gives the fastest access time. The access time is a maximum if both logical and physical addresses give cache misses.

3.0 USING THE MA31751 WITH THE MAS281

3.1 THE MODE INPUT

The mode pin provides a means to switch the MMU between being MA31750 compatible and MAS281 compatible.

In MAS281 mode, the MA31751 requires access to the configuration register in order to correctly configure the device. It must therefore reside on the local AD bus rather than the system AD bus.

3.2 ADDRESS AND DATA BUS TIMINGS

The MAS281 uses a multiplexed address and data bus format. The MMU deals with this by connecting the MAS281 AD bus to its D bus. Whilst in 281 mode the address bus A on the MMU will become an output bus. Addresses will be captured from the AD bus by a 16-bit latch inside the MA31751 which is transparent during AS high. This obviates the need for any external address demultiplexing latches. Clocks are needed in MAS281 mode therefore SYNC is connected to EA[0] and OSC to EA[1] (note that the MAS281 will only operate to MIL-STD 1750A, using EA[3:10] as the extended address bus.)

3.3 STROBE TIMINGS AND SIGNAL DEFINITIONS

To accommodate the extended (5 clock) cycle of the MAS281 all data bus transactions are made with reference to DSN.

Both RESET and INOP have the opposite logic sense on the MAS281 to that on the MA31750. ie. RESET is active high on the MAS281 and INOP high indicates an instruction on the bus. These lines are inverted internally in MAS281 mode so the signals on the MA31751 can be connected directly to system RESET and system INOP.

3.4 PARITY FUNCTION IN MAS281 MODE

On memory write cycles, the MA31751 does not get a parity bit from the MAS281. Therefore, additional parity generation logic is provided by the BMA31751 to allow parity on the memory cycles. If there is a parity error during memory read cycles, the PRPEN signal asserts low to indicate a page RAM parity fault. This would typically be connected to one of the processor fault inputs.

4. PIN DESCRIPTIONS

A description of each pin function appears in Figure 6. The acronym is presented first, followed by its function and description. Timing characteristics of each of the functions are shown in section 6.

All signals - with the exception of power and ground signals are both TTL and CMOS compatible, and are protected by an Electrostatic Discharge (ESD) protection circuit. Throughout this data sheet, active low signals are denoted either by placing a bar over the signal name,or by following the signal name with an "N" suffix, e.g.,DSN.

All unused inputs should be connected to their inactive state and should not be allowed to float.

4.1 SIGNAL DEFINITIONS

Pin Name	Function	Description
SYSTEM BUSSES		
A00-A15	Processor Address Bus	An active-high address bus for addresses and XIO commands. A15 is the LSB. In MAS281 mode, this bus becomes output only.
D00-D16	System Data Bus	Data bus used to transfer data to and from the MMU/BPU. D15 is the LSB and D16 is the parity bit. In MAS281 mode, this bus should be connected to the AD bus on the 281 (D16 unused).
EA00-EA10	Extended Address Bus	If the MMU is selected (using CSN) then EA0-EA10 provides the system extended address. EA3-EA10 should be combined with A4-A15 from the processor to give the full 20 bit 1750A system address bus and EA0-EA10 with A4-A15 gives a 23 bit 1750B system address bus. (See Fig 4).During XIO transfers, EA7-10 mimic A0-A3 to present the full processor address to the system. When the MMU is not selected, EA0-EA10 become inputs to allow the BPU to protect the appropriate section of extended memory. In MAS281 mode EA0 is connected to SYNC and EA1 is connected to OSC. (These pins are unused as extended addresses as the 281 supports only 1750A mode)
BUS CONTROL		
ASIN	Address Strobe In	The rising edge of this active-high signal generated by the CPU or DMA controller, indicates that a valid address is present on the MA31750. A falling edge of ASIN indicates that a valid address is on the AD0-AD15 bus of the MAS281.
DSN	Data Strobe	The rising edge of this active-low signal generated by the CPU or DMA controller, indicates that valid data is present on D00-D16 of the MA31750 or on AD0-AD15 of the MAS281.
EAS	Extended Address Strobe	The rising edge of this active-high signal indicates that a valid and stable extended address is available from the MA31751. The same is indicated for the MAS281 on the falling edge of EAS. This pin becomes an input when no MMU is selected and should be driven from the system address strobe. During XIO cycles, EAS follows ASIN.
MION	Memory / IO Select	This input is used to select between normal operation and command transfer (XIO) mode. A high indicates memory whilst a low indicates IO. This signal is provided by the CPU or the DMA controller.
RDWN	Read / Write Select	This input indicates the direction of data transfer on the data bus. A high level indicates that the processor is reading the bus whilst a low level indicates that the processor is driving the bus. The input is driven by the CPU or the DMA controller.
OIN	Operand / Instruction Select	This input indicates the type of data on the data bus. On the MA31750, a high indicates operand data whilst a low indicates the presence of instruction data. The opposite is true for the MAS281. The signal is provided by the CPU or the DMA controller.
EXTENDED MEMORY CONTROL		
AS0-AS3	Address State	This bus comes from the DMA controller during DMA accesses. It is used by the MMU as part of the page selection operation. (During CPU operation, this information is read from the MMU's copy of the CPU status word). If no MMU function is required, these inputs should be tied to ground.
PS0-PS3	Processor State	This bus comes from the DMA controller during DMA accesses. It is used by the MMU to provide lock and key protection on page accesses. (During CPU operation, this information is read from the MMU's copy of the CPU status word.) If no MMU function is required, these inputs should be tied to ground.

Figure 6: Pin Description Table

ERROR INDICATION

MPROEN	Memory Protect Error	This open drain output is always asserted high when AS is low. On AS rising, MPROEN goes low. If there is an MMU in the system, MPROEN is read out as the extended address is read. This can be sampled on EAS rising. MPROEN high indicates no error, however if MPROEN remains low, a memory access error has occurred. If there is also a BPU in the system, another internal RAM access occurs, MPROEN goes/stays low, and only goes high if there are no access faults, memory protect or write protect errors from the MMU, or a block protect error from the BPU. MPROEN should be sampled on BPUVALIDN if there is a BPU in the system.
PRPEN	Page RAM Parity Error	This active-low open drain output is asserted low if a parity error is detected during an MMU/BPU memory transfer.

MISCELLANEOUS

RESETN	System Reset	Device reset input. Active low for MA31750, active high for MAS281. Should be connected to system reset.
CSN	MMU Chip Select	A low on this input selects the MMU. In a 1750A system, this input may be tied to ground if MMU functions are required, or tied to MION if only BPU functions are required (must be active for XIO cycles when the device may need to respond to an MMU/BPU XIO command.) In 1750B, this input should be derived by decoding the PB[0:3] bus from the CPU. (Note that in 1750B mode, one device is required per implemented page bank.)
BPUVALIDN	BPU enabled and selected	This open drain output becomes active (low) when MPROEN is valid if there is at least one BPU present in the system .
DMAKN	DMA Acknowledge	This active-low input is used to select between the CPU and DMA protection registers within the MA31751, and should be asserted low when the CPU has relinquished control to a DMA in the system. The signal is driven by the system.
GLPE	Global Protect Enable	This active-high signal goes high in BPU mode following a system reset to indicate that the memory system is globally write-protected. The signal is set low by the XIO MPEN command. GPLE is inactive high when the BPU functions are disabled.
MODE	31750 or 281 processor	When this input is high, the MMU works with a MA31750 processor. When the pin is low, the MMU is MAS281 compatible.

POWER

VDD	Power Supply	5V DC power supply input.
GND	Ground	0V reference point.

Figure 6: Pin Description Table (continued)

5.0 DC PARAMETERS - ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current through any pin except V_{DD} and GND	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Figure 7a: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.1 DC PARAMETERS - NORMAL OPERATING CONDITIONS

			Total dose radiation not exceeding $3x10^5$ Rad(si)			Total dose radiation not exceeding 1MRad(Si)		
Symbol	Parameters	Conditions	Min	Typ	Max	Min	Max	Units
VDD	Supply Voltage	-	4.5	5.0	5.5	-	-	V
VIH	Input high voltage	-	2.0	-	-	2.0	-	V
VIL	Input low voltage	-	-	-	0.8	-	0.3	V
VOH	Output high voltage	IOH=-5mA	Vdd-0.5	-	-	Vdd-0.5	-	V
VOL	Output low voltage	IOL= 5mA	-	-	Vss+0.4	-	Vss+0.4	V
IIH	Input high current (Note 1)	-	-	-	10	-	100	uA
IIL	Input low current (Note 1)	-	-	-	-10	-	100	uA
IDDYN	Dynamic supply current	-	-	-	50	-	100	mA
IDDS	Static supply current	-	-	0.2	10	-	20	mA

VDD = 5V ±10% over full operating temperature range.
Mil-Std-883, method 5005, subgroups 1, 2, 3
Note 1: Guaranteed but not measured at -55°C

Figure 7b: Operating DC Parameters

Subgroup	Definition
1	Static characteristics specified in Figure 7b at +25°C
2	Static characteristics specified in Figure 7b at +125°C
3	Static characteristics specified in Figure 7b at -55°C
7	Functional characteristics specified at +25°C
8A	Functional characteristics specified at +125°C
8B	Functional characteristics specified at -55°C
9	Switching characteristics specified in Figure 9 at +25°C
10	Switching characteristics specified in Figure 9 at +125°C
11	Switching characteristics specified in Figure 9 at -55°C

Figure 8: Definition of Subgroups

6.0 TIMING PARAMETERS

	Parameter	Min	Typ	Max	Units
1	DSN falling to data bus active	-	25	40	ns
2	DSN falling to data from MMU valid	-	80	90	ns
3	Data valid after DSN rising (read)	10	-	-	ns
4	Data bus inactive after DSN rising	-	-	45	ns
5	Address and control setups to ASIN rising	15	-	-	ns
6	Address and control hold after ASIN falling	5	-	-	ns
7	CSN setup to DSN rising (1750B)	75	-	-	ns
8	CSN hold after DSN rising (1750B)	0	-	-	ns
9	Data hold after DSN rising (write)	10	-	-	ns
10	Data setup to DSN rising (write)	5	-	-	ns
11	ASIN falling to EAS falling	-	20	30	ns
12	Extended address valid to EAS rising	5	-	30	ns
13	ASIN rising to EA bus valid (MMU cache hit)	-	25	40	ns
14	EA bus valid to PRPEN active	5	-	15	ns
15	ASIN rising to EA bus valid (MMU cache miss)	-	60	80	ns
16	ASIN rising to MPROEN active (MMU cache hit)	-	45	60	ns
17	ASIN rising to MPROEN active (MMU cache miss)	-	85	105	ns
18	ASIN rising to MPROEN active (2 cache hits)	-	45	60	ns
19	ASIN rising to MPROEN active (1 miss, 1 cache hit)	-	85	105	ns
20	ASIN rising to MPROEN active (No MMU, BPU miss)	-	40	50	ns
21	ASIN rising to MPROEN active (MMU and BPU miss)	-	140	185	ns
22	MPROEN setup to BPUVALIDN falling	5	-	-	ns
23	ASIN rising to GLPE falling	-	20	-	ns
24	RESETN falling to GLPE rising	-	20	-	ns
25	RESETN falling to MPROEN rising	-	20	-	ns
26	MAS281 AD bus to valid MMU address	-	-	15	ns
27	A bus to valid EA bus (cache hit)	-	20	35	ns
28	A bus to valid EA bus (cache miss)	-	20	35	ns
29	ASIN rising to EAS rising	0	-	20	ns
30	EA bus setup to EAS falling	5	-	-	ns
31	MPROEN active to SYNC falling (cache hit)	4T-35	-	-	ns
32	MPROEN active to SYNC falling (cache miss)	-	4T-65	-	ns
33	MPROEN active to SYNC falling (MMU and BPU hit)	4T-35	-	-	ns
34	MPROEN active to SYNC falling (MMU miss, BPU hit)	-	4T-65	-	ns
35	MPROEN active to SYNC falling (MMU hit, BPU miss)	-	4T-55	-	ns
36	MPROEN active to SYNC falling (MMU and BPU miss)	4T-90	-	-	ns

Mil-Std-883, method 5005, subgroups 9, 10 and 11

Figure 9: Timing Parameters (typical figures reflect room temperature and supply voltage = 5V)

7.0 TIMING DIAGRAMS

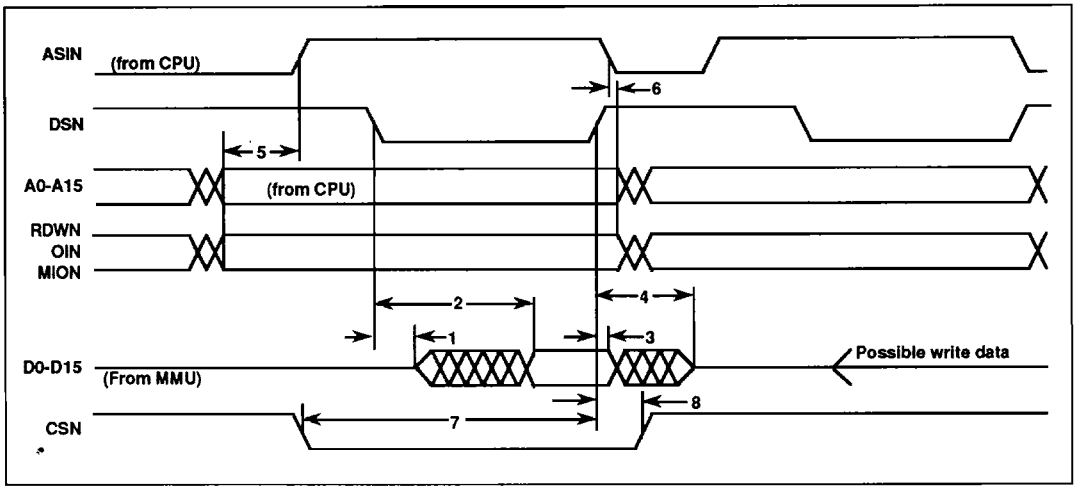


Figure 10: MA31750 XIO Read of MMU

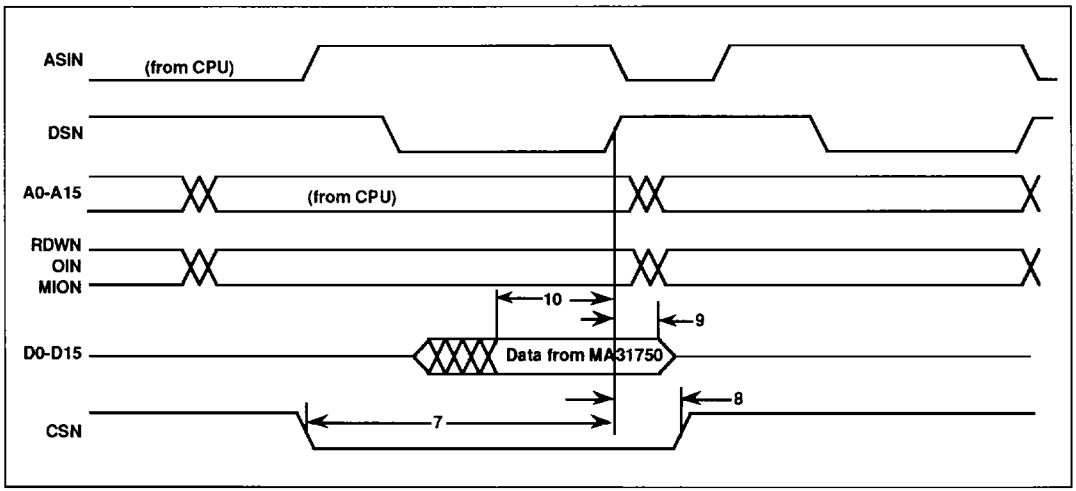


Figure 11: MA31750 XIO Write to MMU

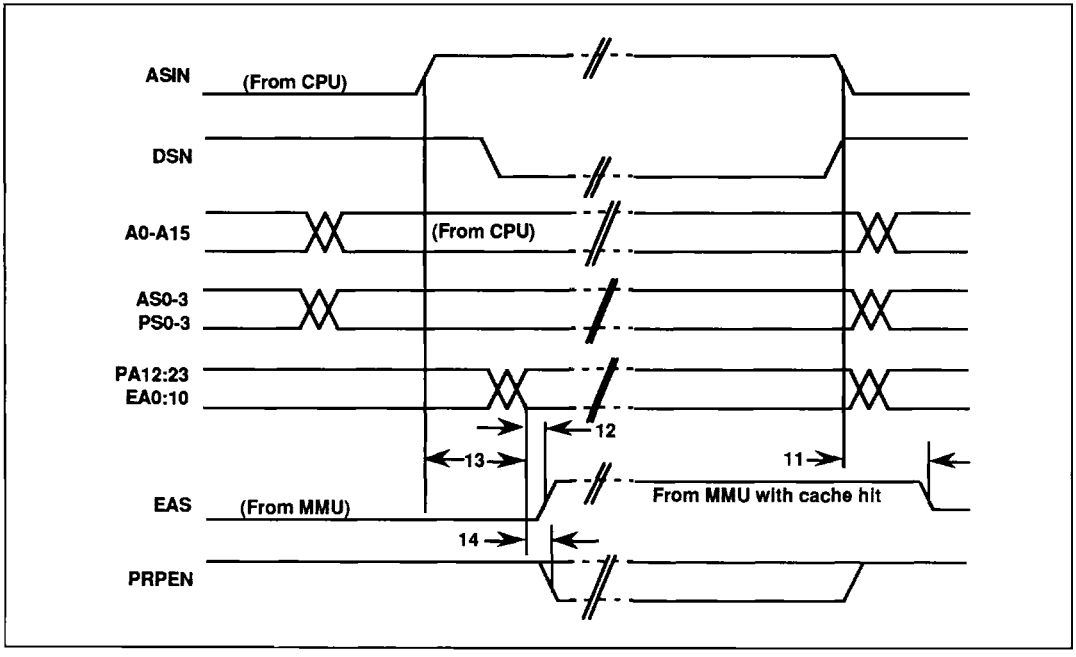


Figure 12: MMU Address Translation (Cache Hit)

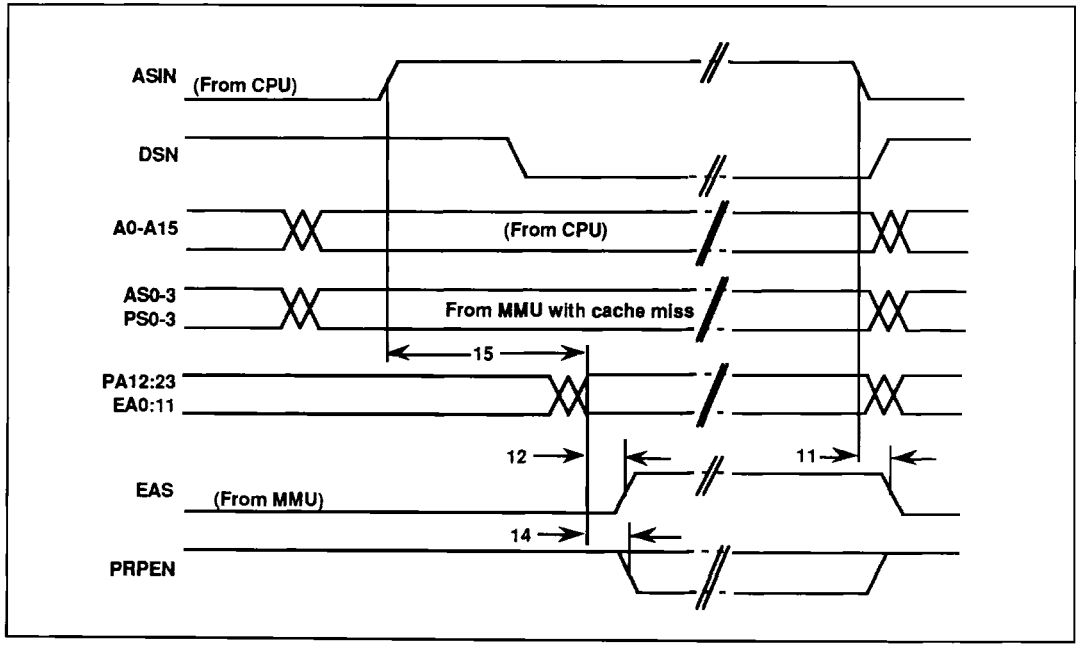


Figure 13: MMU Address Translation (Cache Miss)

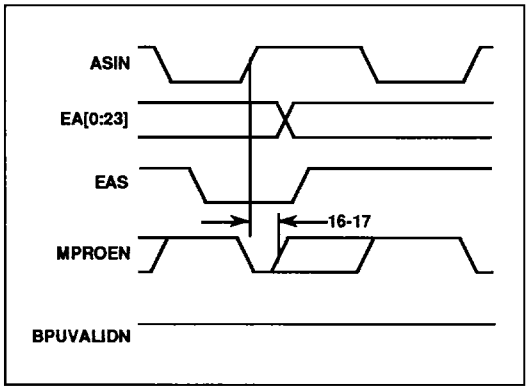


Figure 14a: MMU Timing With No BPU

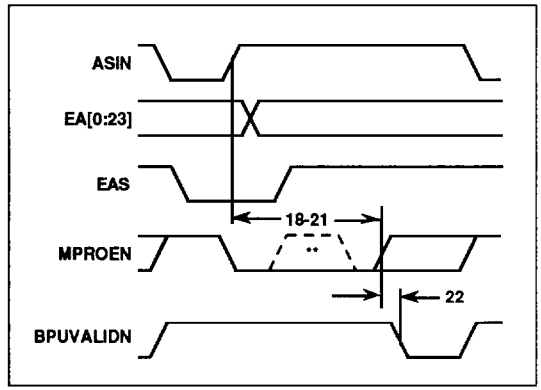


Figure 14b: MMU and BPU Timings

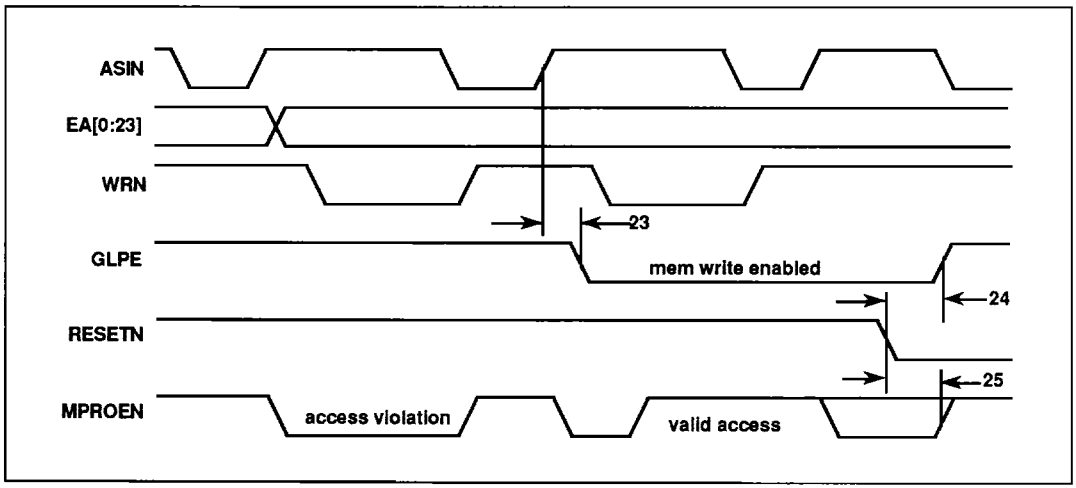


Figure 15: Reset and Enable Timings

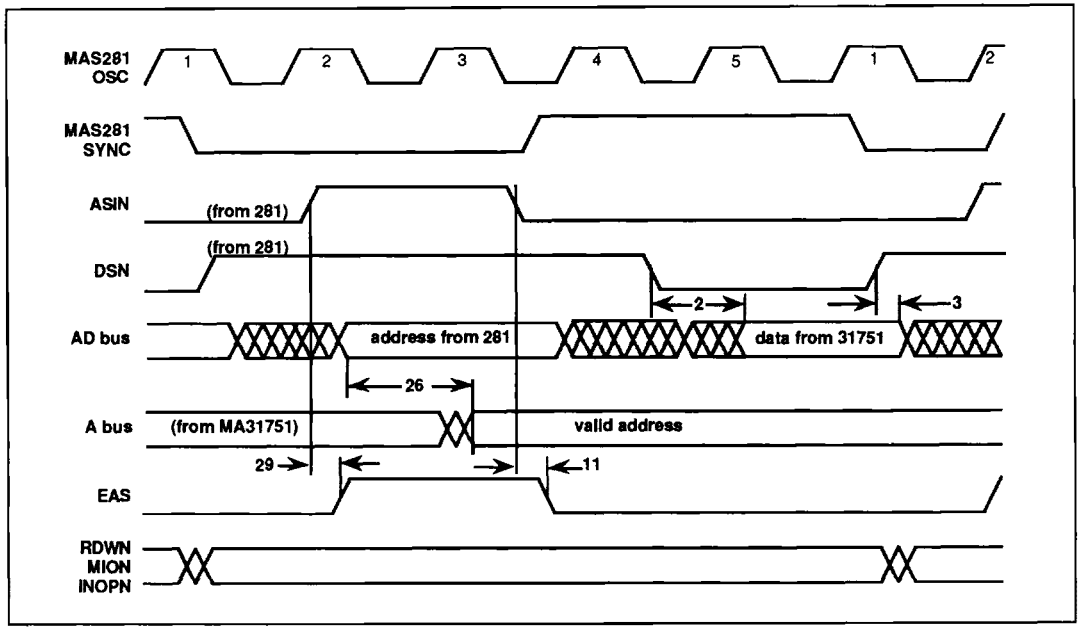


Figure 16: MAS281 XIO Read Cycle

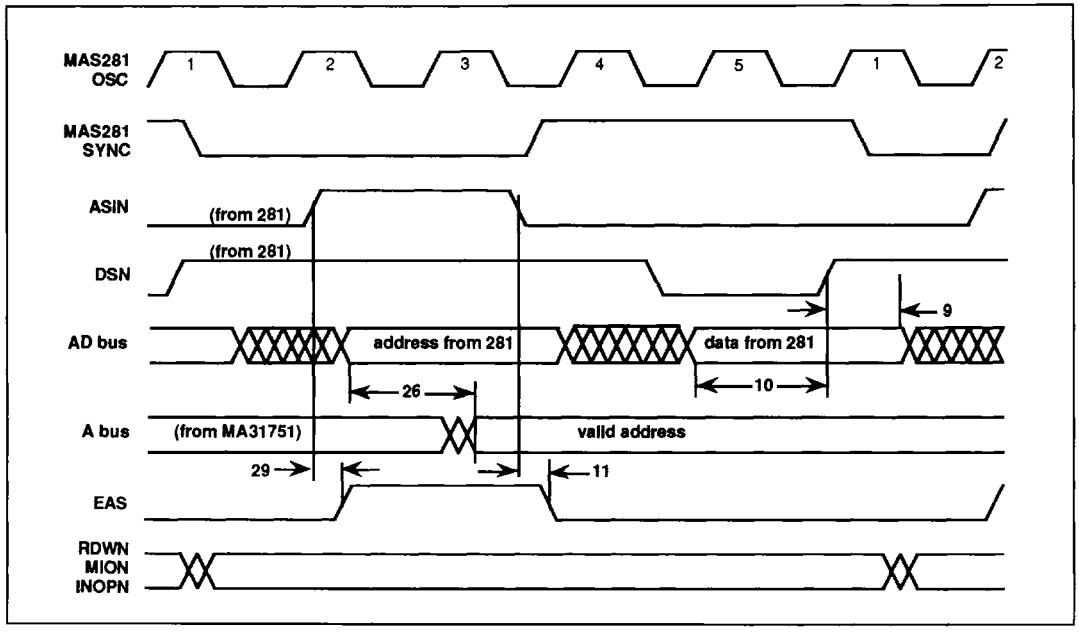


Figure 17: MAS281 XIO Write Cycle

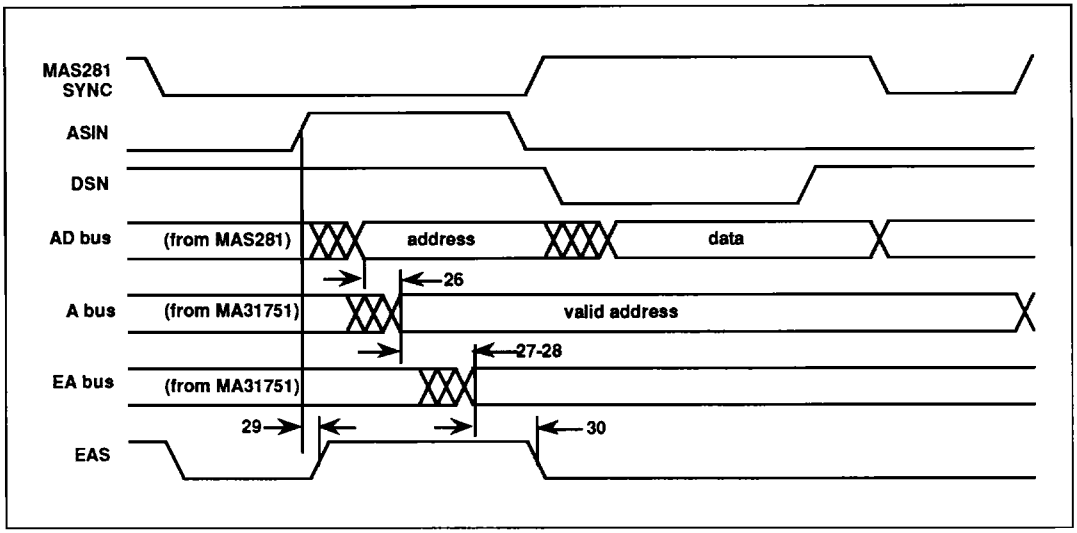


Figure 18: MAS281 Mode - Address Translation Timings

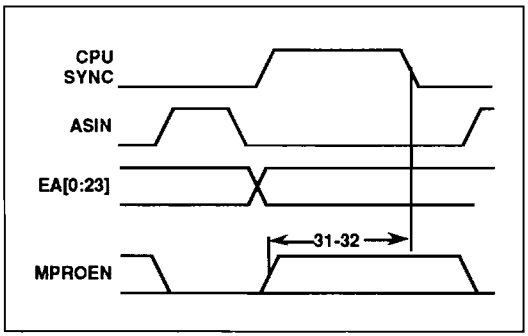


Figure 19a: MMU Timings in 281 Mode

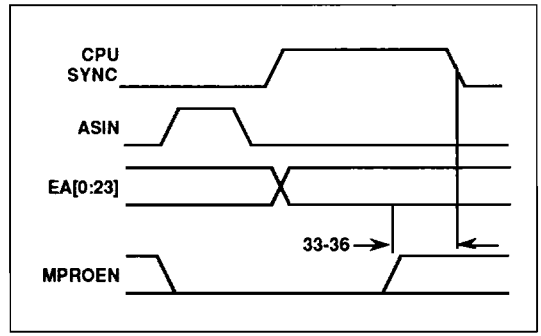
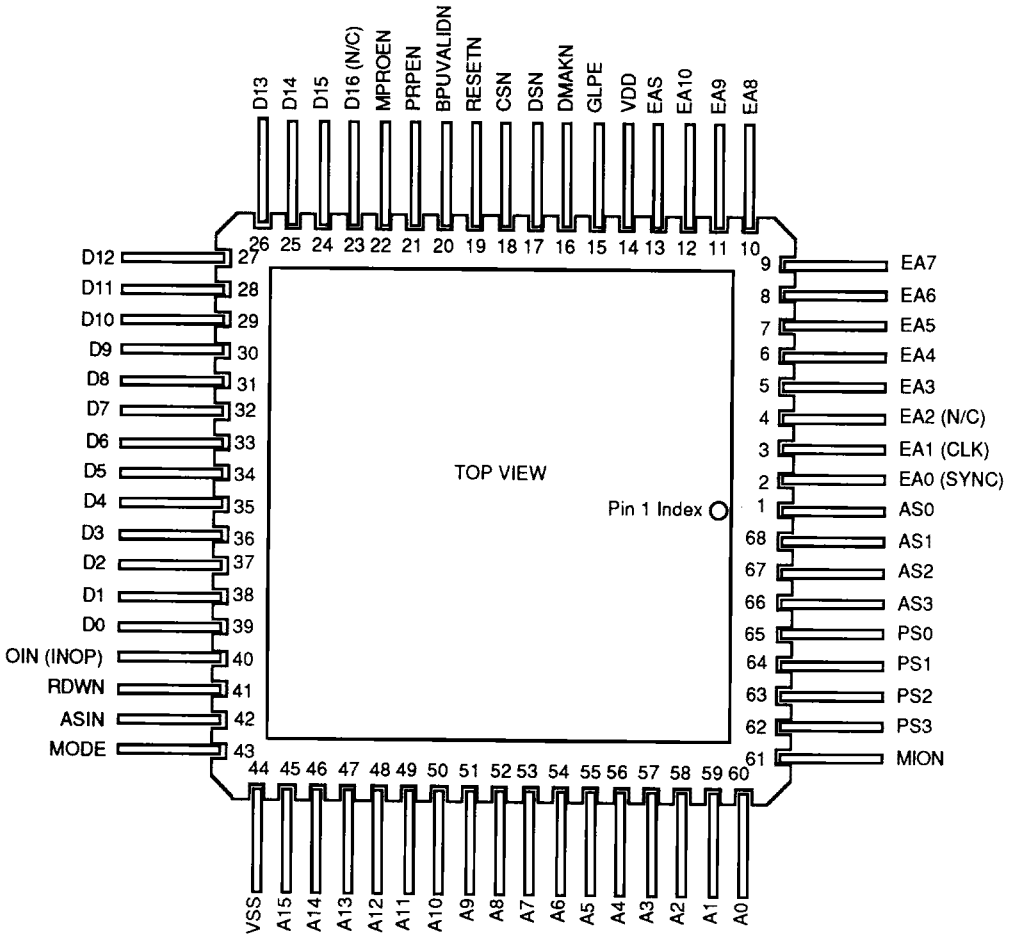


Figure 19b: MMU and BPU Timings in 281 Mode

8.0 PACKAGING INFORMATION

8.1 FLATPACK PINOUT



Note: Bracketed names indicate MAS281 mode functions.

Figure 20: 68 Pin Lead Flatpack - Package Style F

8.2 FLATPACK DIMENSIONAL DRAWING

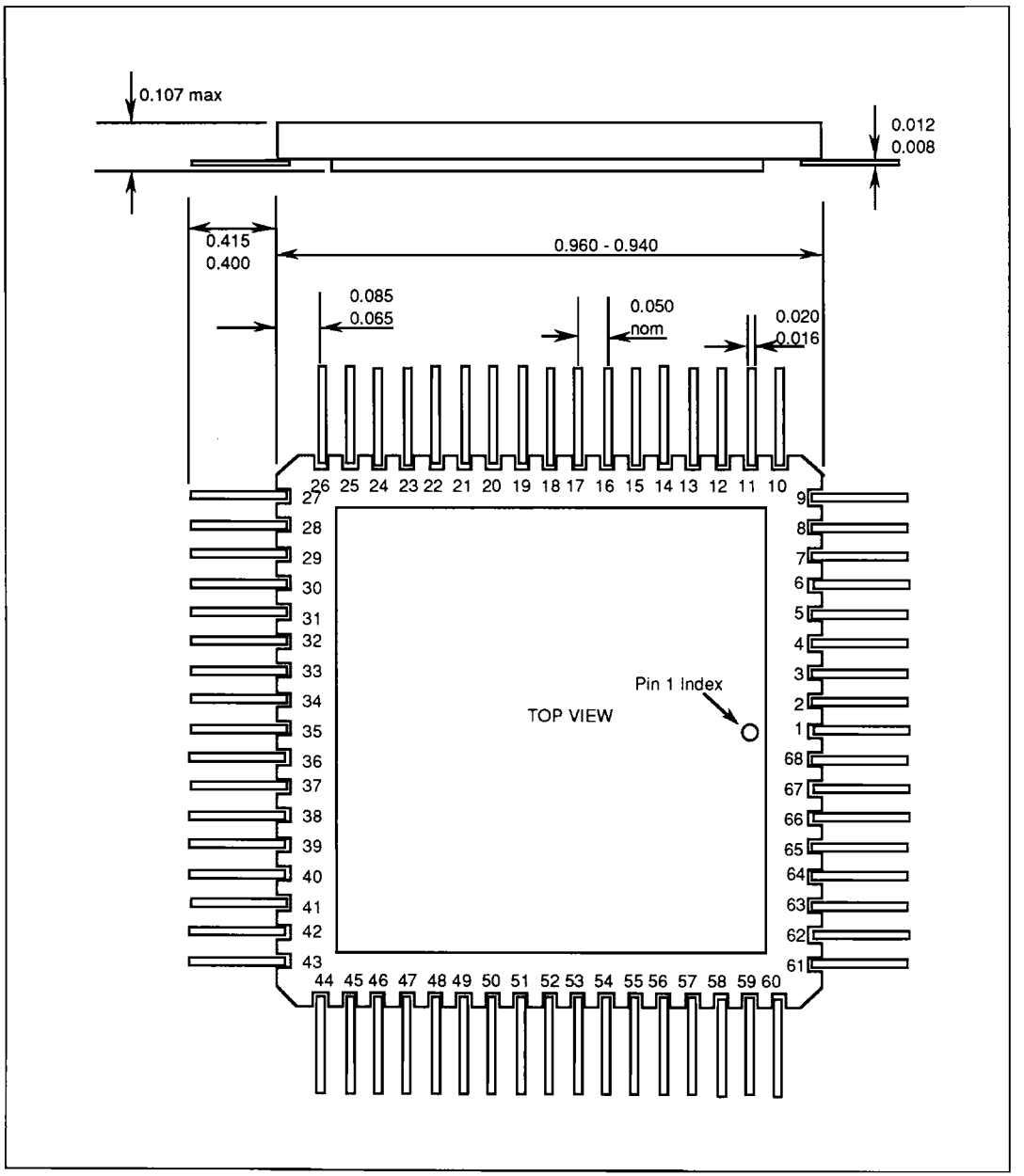
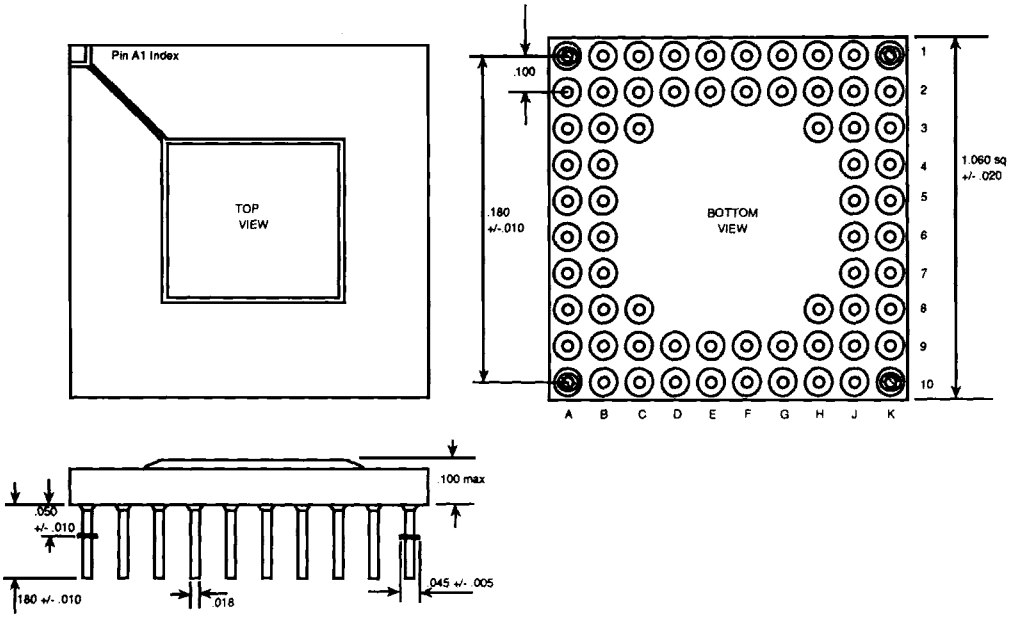


Figure 21: Dimensional Drawing of 68 Pin Lead Flatpack - Package Style F

8.3 PGA PINOUT AND DIMENSIONED DRAWING



Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	PS3	C1	PS0	G9	D7	K3	VDD
A2	A2	C2	PS2	G10	D6	K4	DMAKN
A3	A4	C3	MION	H1	EA3	K5	CSN
A4	A5	C8	GND	H2	EA6	K6	RESETN
A5	A7	C9	ASIN	H3	EA8	K7	PRPEN
A6	A8	C10	D0	H8	D12	K8	MPROEN
A7	A10	D1	AS2	H9	D10	K9	D15
A8	A12	D2	AS3	H10	D8	K10	D11
A9	A13	D9	OIN (INOP)	J1	EA5		
A10	A15	D10	D1	J2	EA7		
B1	PS1	E1	AS0	J3	EA10		
B2	A0	E2	AS1	J4	GLPE		
B3	A1	E9	D2	J5	DSN		
B4	A3	E10	D3	J6	BPUVALIDN		
B5	A6	F1	EA0 (SYNC)	J7	D16 (N/C)		
B6	A9	F2	EA1 (CLK)	J8	D14		
B7	A11	F9	D5	J9	D13		
B8	A14	F10	D4	J10	D9		
B9	MODE	G1	EA2 (N/C)	K1	EA9		
B10	RDWN	G2	EA4	K2	EAS		

Note: Bracketed names indicate MAS281 mode functions

Figure 22: PGA Pinout and Dimensioned Drawing

9.0 RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Function to specification)	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$3x10^{11}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$1x10^{15}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$<1x10^{-10}$ errors/bitday
Latch-up	Not possible

Figure 23: Radiation Performance

10.0 OTHER INFORMATION

Applications support for this and all other GPS SOS products is available now from the GPS applications support team who can be reached on:

GEC Plessey Semiconductors, Lincoln Industrial Park, Doddington Rd, Lincoln, ENGLAND, LN6 3LF

Tel: (UK) 522 502274 (direct line)
Fax: (UK) 522 502393
E-Mail: apps@lincoln.gpsemi.com

Information on pricing and availability of all GPS SOS parts is available from GPS marketing at the same address or:

Tel: (UK) 522 502394 (direct line)
Fax: (UK) 522 502277

11.0 ORDERING INFORMATION