LOGIC DEVICES INCORPORATED

LPR520/521

4 x 16-bit Multilevel Pipeline Register

FEATURES

- Four 16-bit Registers
- Implements Double 2-Stage Pipeline or Single 4-Stage Pipeline Register
- Hold, Shift, Load Instructions
- Separate Data In and Data Out Pins
- High Speed, Low Power CMOS Technology
- Three-State Outputs
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 40-pin Plastic DIP
  - 40-pin Sidebraze, Hermetic DIP
  - 44-pin Plastic LCC, J-Lead
  - 44-pin Ceramic LCC (Type C)

DESCRIPTION

T-46-09-09

The Logic Devices LPR520 and LPR521 are functionally compatible with the Advanced Micro Devices AM29520 and AM29521 but are 16 bits wide. They are implemented in low power CMOS.

The LPR520 and LPR521 contain four registers which can be configured as two independent, 2-level pipelines or as one 4-level pipeline.

The Instruction pins, I_0 and I_1, control the loading of the registers. For either device, the registers may be configured as a four-stage delay line, with data loaded into R_1 and shifted sequentially through R_2, R_3, and R_4. Also, for the LPR520, data may be loaded from the inputs into either R_1 or R_3 with only R_2 or R_4 shifting. The LPR521 devices differ from the LPR520 in that R_2 and R_4 remain unchanged during this type of data load, as shown in Tables 1 and 2. Finally, I_0 and I_1 may be set to prevent any register from changing.

The S_0 and S_1 select lines control a 4 to 1 multiplexer which routes the contents of any of the registers to the Y output pins. The independence of the I and S controls allows simultaneous write and read operations on different registers.

LPR520/521 BLOCK DIAGRAM

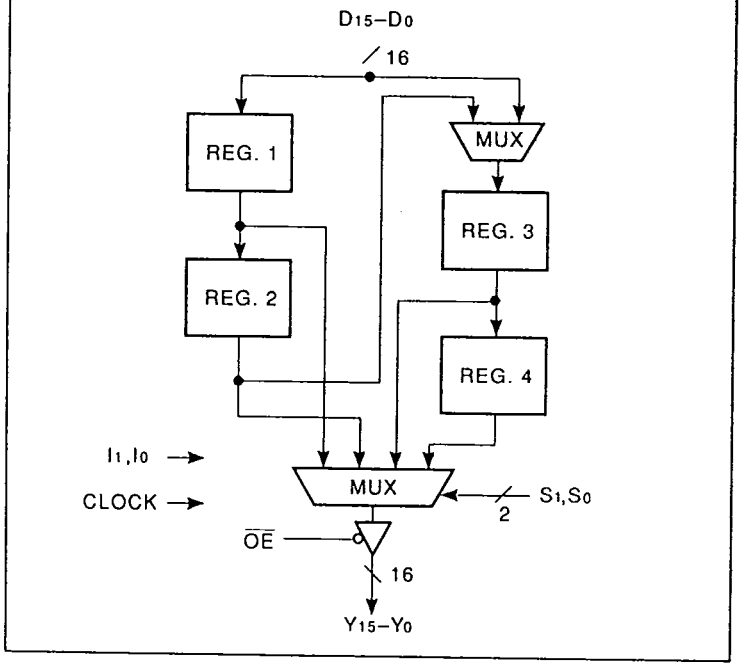

TABLE 1

I_1	I_0	L29C520 Instruction
L	L	D→R1 R1→R2 R2→R3 R3→R4
L	H	HOLD HOLD D→R3 R3→R4
H	L	D→R1 R1→R2 HOLD HOLD
H	H	ALL REGISTERS ON HOLD

TABLE 2

I_1	I_0	L29C521 Instruction
L	L	D→R1 R1→R2 R2→R3 R3→R4
L	H	HOLD HOLD D→R3 HOLD
H	L	D→R1 HOLD HOLD HOLD
H	H	ALL REGISTERS ON HOLD

TABLE 3

S_1	S_0	Reg. Selected
L	L	Reg 4
L	H	Reg 3
H	L	Reg 2
H	H	Reg 1

4 x 16-bit Multilevel Pipeline Register

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Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
Vcc supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ Vcc ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ Vcc ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		Vcc	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ Vcc (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ Vcc (Note 12)			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, Vcc = Max (Notes 4, 8)			−250	mA
I_{CC1}	Vcc Current, Dynamic	(Notes 5, 6)		10	40	mA
I_{CC2}	Vcc Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

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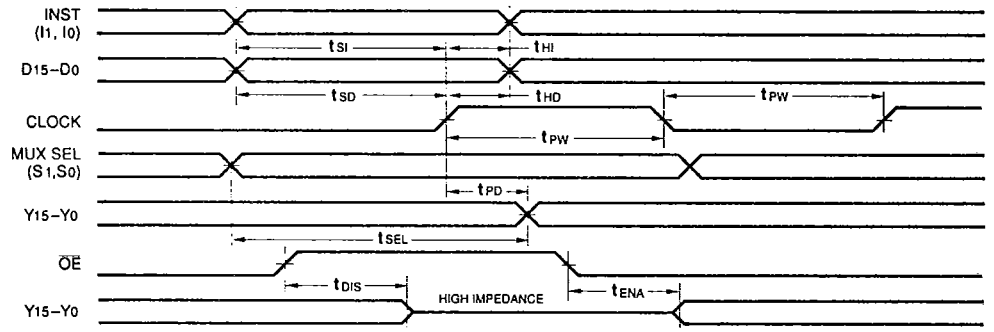
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LPR520/521- 25 Min	25 Max	22 Min	22 Max	15 Min	15 Max
t_{PD}	CLK to Y_{15}–Y_0		25		22		15
t_{SEL}	S_1,S_0 to Y_{15}–Y_0		25		20		15
t_{SD}	D_{15}–D_0 to CLK Setup	13		10		6	
t_{HD}	CLK to D_{15}–D_0 Hold	3		3		1	
t_{SI}	I_1,I_0 to CLK Setup	13		10		6	
t_{HI}	CLK to I_1,I_0 Hold	3		3		1	
t_{DIS}	$\overline{OE}$ to Output Disable (Note 11)		25		15		12
t_{ENA}	$\overline{OE}$ to Output Enable (Note 11)		25		21		15
t_{PW}	Clock Pulse Width	10		10		8	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LPR520/521- 30 Min	30 Max	24 Min	24 Max	18 Min	18 Max
t_{PD}	CLK to Y_{15}–Y_0		30		24		18
t_{SEL}	S_1,S_0 to Y_{15}–Y_0		30		22		18
t_{SD}	D_{15}–D_0 to CLK Setup	15		10		8	
t_{HD}	CLK to D_{15}–D_0 Hold	5		3		2	
t_{SI}	I_1,I_0 to CLK Setup	15		10		8	
t_{HI}	CLK to I_1,I_0 Hold	5		3		2	
t_{DIS}	$\overline{OE}$ to Output Disable (Note 11)		20		16		13
t_{ENA}	$\overline{OE}$ to Output Enable (Note 11)		25		22		16
t_{PW}	Clock Pulse Width	15		10		9	

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at GND – 0.6 V.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

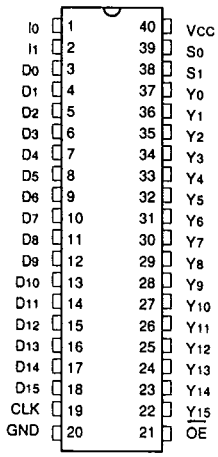
12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

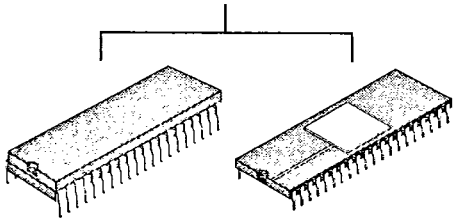
4 x 16-bit Multilevel Pipeline Register

ORDERING INFORMATION

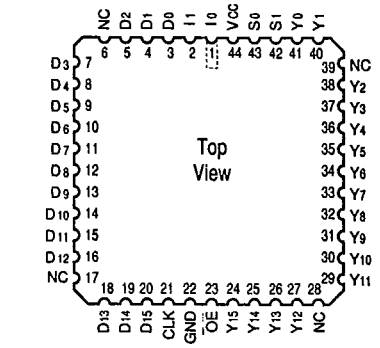
T-46-09-09

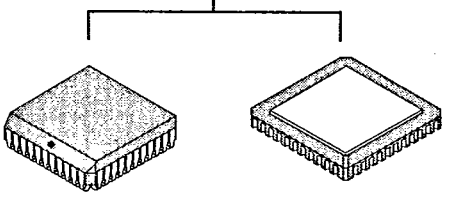
40-pin





44-pin





Speed	Plastic DIP (P3)	Sidebraze Hermetic DIP (D3)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — Commercial Screening			
25 ns 22 ns 15 ns	LPR520PC or LPR521PC — 25 / 22 / 15	LPR520DC or LPR521DC — 25 / 22 / 15	LPR520JC or LPR521JC — 25 / 22 / 15	LPR520KC or LPR521KC — 25 / 22 / 15
	–55°C to +125°C — Commercial Screening			
30 ns 24 ns 18 ns		LPR520DM or LPR521DM — 30 / 24 / 18		LPR520KM or LPR521KM — 30 / 24 / 18
	–55°C to +125°C — Extended Screening			
30 ns 24 ns 18 ns		LPR520DME or LPR521DME — 30 / 24 / 18		LPR520KME or LPR521KME — 30 / 24 / 18
	–55°C to +125°C — MIL-STD-883 Compliant			
30 ns 24 ns 18 ns		LPR520DMB or LPR521DMB — 30 / 24 / 18		LPR520KMB or LPR521KMB — 30 / 24 / 18

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Mechanical Drawings

CerDIP — Type C

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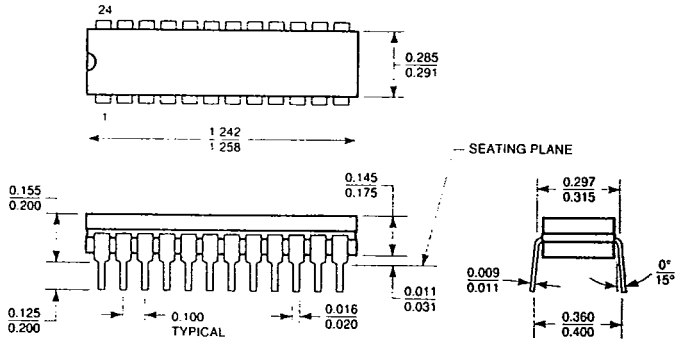
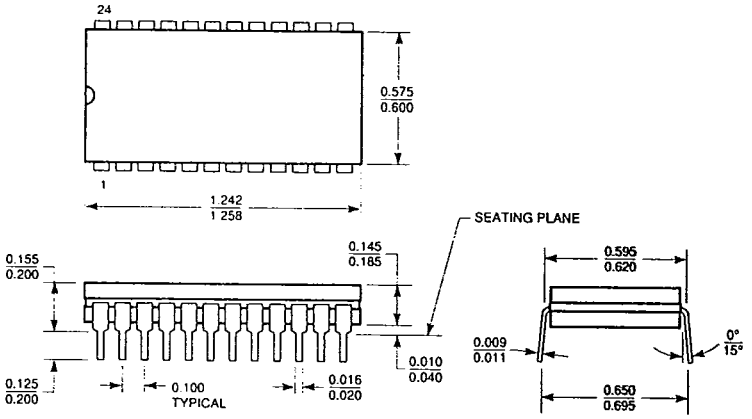
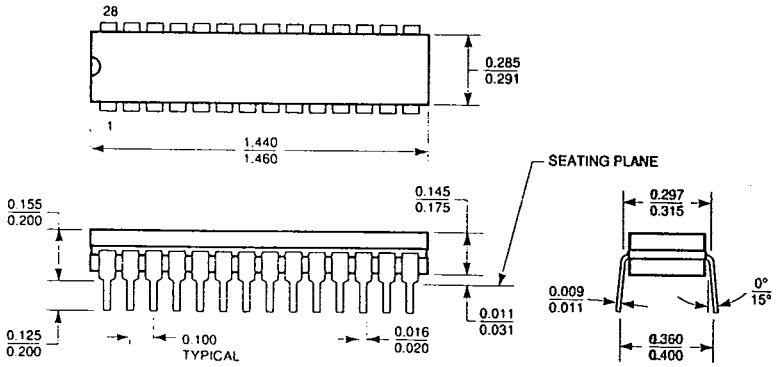
C1 — 24-pin CerDIP (0.3" Wide)



C4 — 24-pin CerDIP (0.6" Wide)



C5 — 28-pin CerDIP (0.3" Wide)



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Mechanical Drawings

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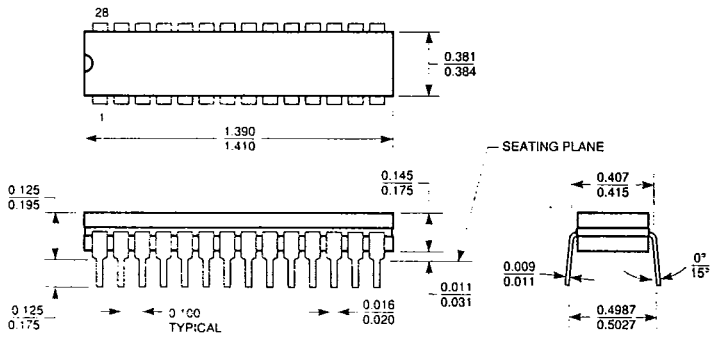
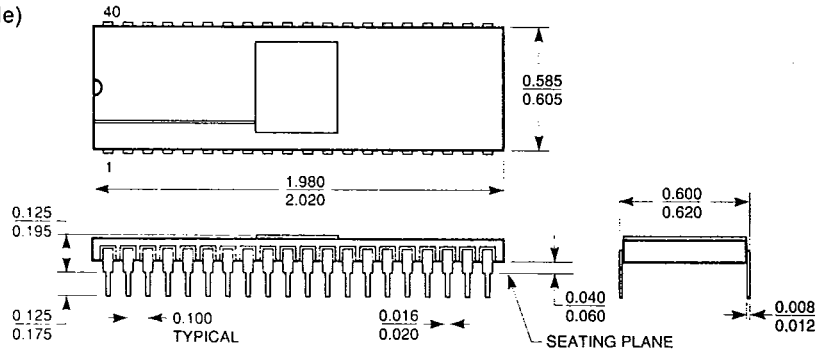
CerDIP — Type C

C10 — 28-pin CerDIP (0.4" Wide)



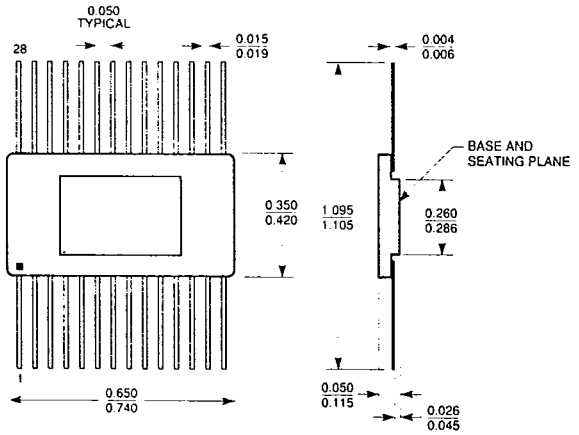
Sidebraze, Hermetic DIP — Type D

D3 — 40-pin Hermetic DIP (0.6" Wide)



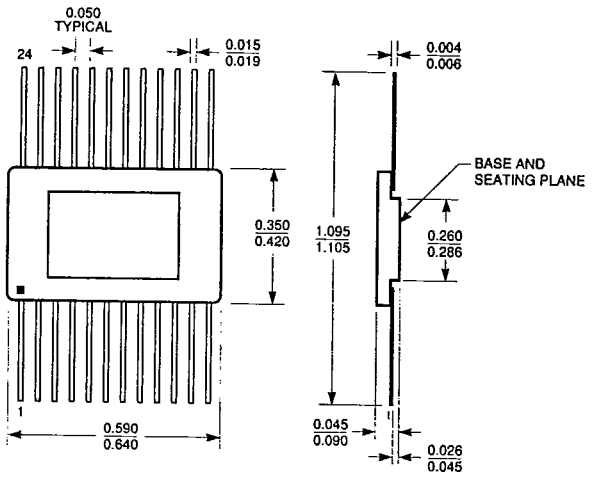
Ceramic Flat Pack — Type F

F1 — 24-pin Ceramic Flat Pack



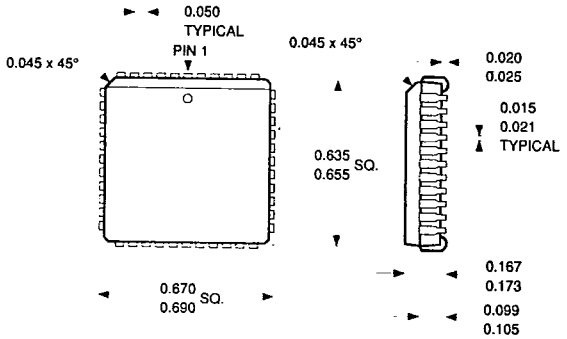
Ceramic Flat Pack — Type F

F2 — 28-pin Ceramic Flat Pack

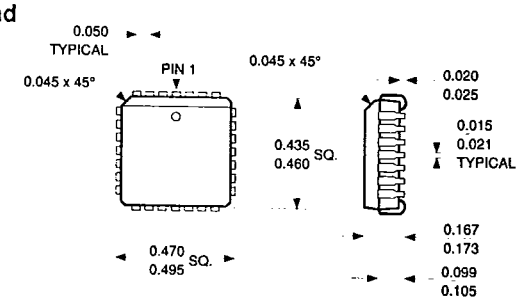


Plastic J-Lead Chip Carrier — Type J

J1 — 44-pin Plastic J-Lead (0.690" x 0.690")



J4 — 28-pin Plastic J-Lead (0.490" x 0.490")



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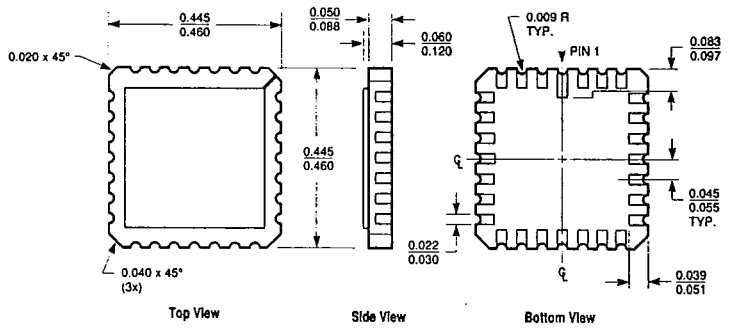
Mechanical Drawings

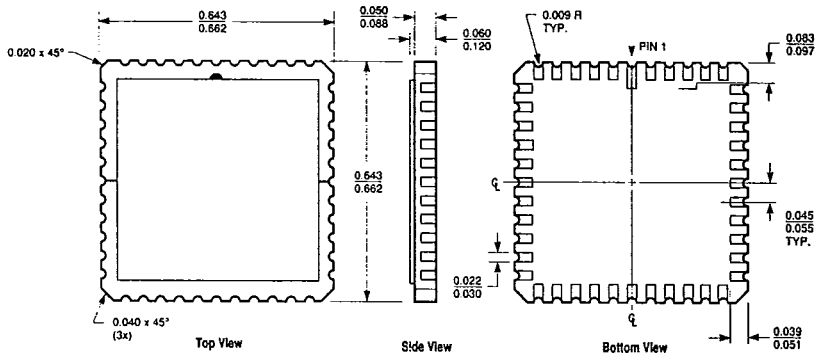
T-90-20

Ceramic Leadless Chip Carrier — Type K

K1 — 28-pin Ceramic LCC (0.450" x 0.450")

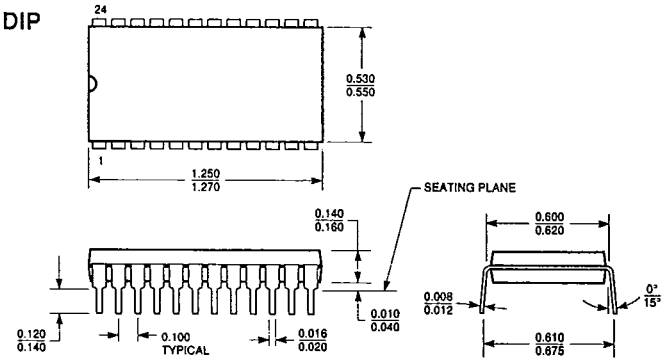


K2 — 44-pin Ceramic LCC (0.650" x 0.650")



Plastic DIP — Type P

P1 — 24-pin Plastic DIP (0.6" Wide)



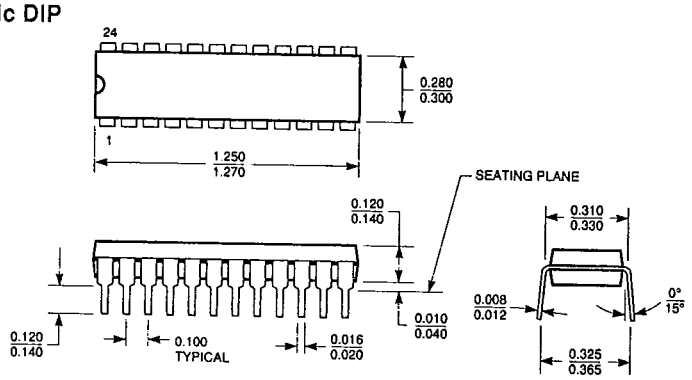
LOGIC DEVICES INCORPORATED

Mechanical Drawings

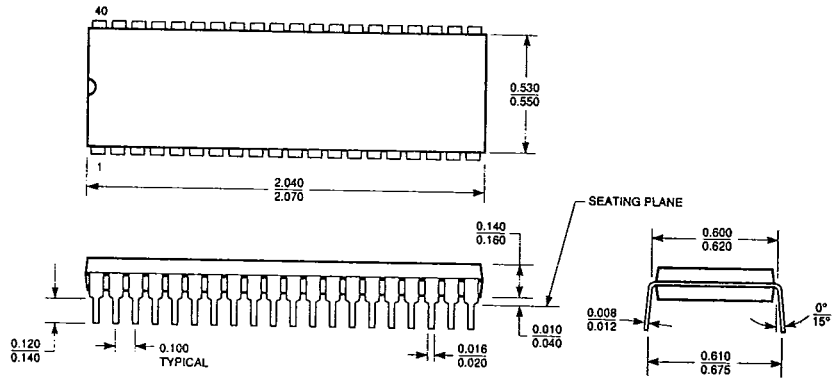
T-90-20

Plastic DIP — Type P

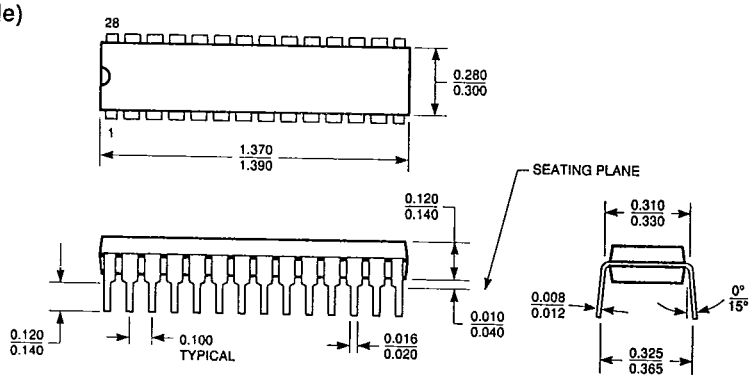
P2 — 24-pin Plastic DIP (0.3" Wide)



P3 — 40-pin Plastic DIP (0.6" Wide)



P10 — 28-pin Plastic DIP (0.3" Wide)



Plastic DIP — Type P

P11 — 28-pin Plastic DIP (0.4" wide)