Preliminary AK9832

32ch, 8-Bit D/A Converters with EEPROM

GENERAL DESCRIPTION

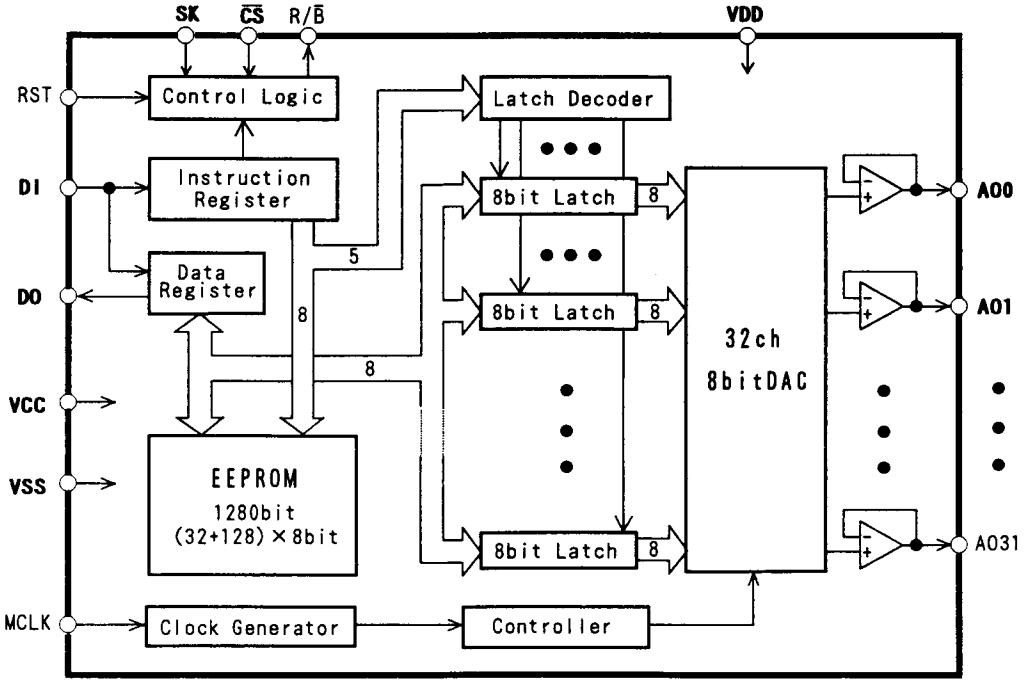
The AK9832 includes 32 channel, 8-bit D/A converters with on-chip output buffer amps and it is capable to store the input digital data of each DAC by on-chip non-volatile CMOS EEPROM. The AK9832 is optimally designed for various circuit adjustments for consumer and industrial equipments and it is ideally suited for replacing mechanical trimmers.

FEATURES

☐ EEPROM SECTION
- 32 words × 8-bit organization for DAC
- 128 words × 8-bit for general purpose memory
- Automatic write cycle time-out with auto-ERASE
- Serial data interface
- 10,000 erase/write cycles
- 10 year data retention

☐ D/A SECTION
- Resolution: 8-bit, 10mV
- 32 channels
- On-chip output buffer amps

☐ 44pin QFP

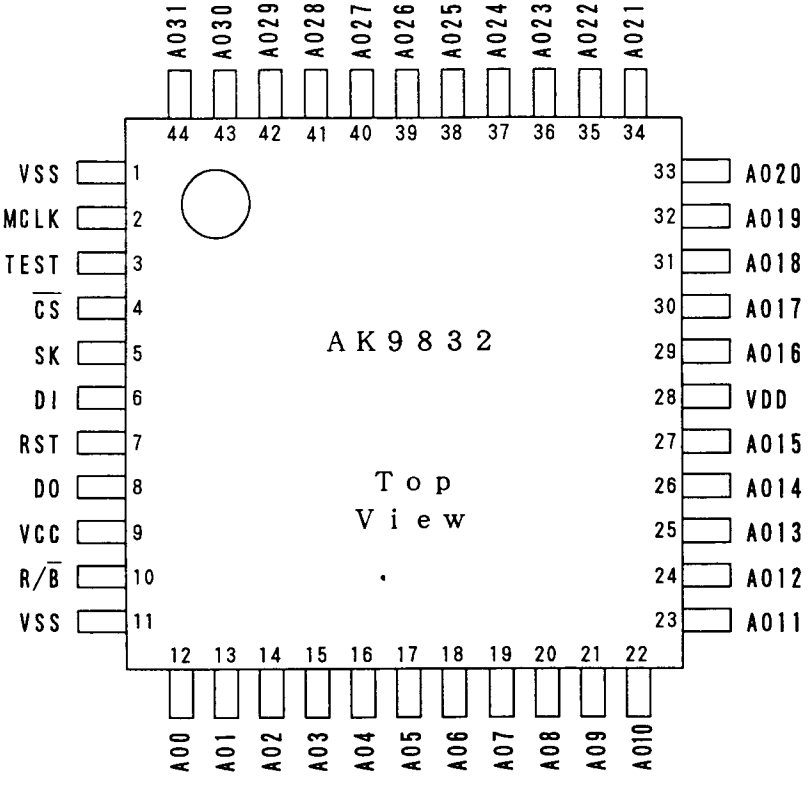


Block Diagram

■ Ordering Guide

AK9832 -10 to 70℃ 44-pin QFP

■ Pin Layout



■ Pin Description

No.	Pin Name	I/O	Function
1 11	VSS	-	Ground Pin, 0V
2	MCK	I	Master Clock Pin
3	TEST	I	Test Pin (with an internal pull-down) Should be normally left open or connected to Ground Pin (VSS)
4	$\overline{CS}$	I	Chip Select Pin
5	SK	I	Serial Clock Pin
6	DI	I	Serial Data Input Pin
7	RST	I	Reset Pin (with an internal pull-down)
8	DO	O	Serial Data Output Pin
9	VCC	-	EEPROM Section Power Supply Pin, +5V
10	R/$\overline{B}$	O	Ready / Busy Pin
28	VDD	-	D/A Section Power Supply Pin, +5V
12 ⋮ 27 29 ⋮ 44	A00 ⋮ A015 A016 ⋮ A031	O	Analog Output Pins (8-bit D/A outputs)

ABSOLUTE MAXIMUM RATINGS

(VSS=0V)

Parameter	Symbol	Condition	Spec.	Units
DC power supplies	VCC	Relative to VSS	-0.3～+6.5	V
	VDD	Relative to VSS	-0.3～+6.5	V
Input Voltage	V_{IO}	Relative to VSS	-0.3～VCC+0.3	V
Ambient Temperature	Ta		-10～+70	℃
Storage Temperature	T_{ST}		-65～+150	℃

RECOMMENDED OPERATING CONDITIONS

(VSS=0V)

Parameter	Symbol	Condition	min	typ	max	Units
DC Power Supplies	VCC	VCC=VDD	4.75	5.0	5.25	V
	VDD		4.75	5.0	5.25	V
Analog Output Load Capacitance	AOC				100	pF

ELECTRICAL CHARACTERISTICS

■ DC Characteristics

1) EEPROM Section

(VCC=VDD=+5V±5% , VSS=0V , Ta=-10～70℃ unless otherwise specified)

Parameter	Symbol	Condition	min	max	Units
Operating Current	ICC	DO=R/$\overline{B}$=open(Note2)			
READ, WREN, WRDS		1/t_{SKP}=1MHz		1	mA
WRITE				6	mA
Standby Current	ICC_{SB}	DO=R/$\overline{B}$=open(Note2)		100	uA
High-Level Input Voltage	V_{IH}				
$\overline{CS}$, SK, MCLK, RST pin			80%VCC		V
DI pin			70%VCC		V
Low-Level Input Voltage	V_{IL}				
$\overline{CS}$, SK, MCLK, RST pin				20%VCC	V
DI pin				30%VCC	V
High-Level Output Voltage	V_{OH}	I_{OH}=-0.4mA	VCC-0.4		V
Low-Level Output Voltage	V_{OL}	I_{OL}=2.1mA		0.4	V
Input Leakage Current	I_{LI}	V_{IN}=VCC (Note3)		10	uA
3 state Leakage Current	I_{OZ}	$\overline{CS}$="H"		±10	uA

Notes: 2. All input pins are connected to either VCC or VSS.

3. For pins TEST and RST, it is Max.30uA since both pins have internal pull-downs.

2) D/A Section

(VCC=VDD=+5V±5% , VSS=0V , Ta=-10～70℃ unless otherwise specified)

Parameter	Symbol	Condition	min	typ	max	Units
Power Supply Current	IDD	No load		7	11	mA
Resolution		Monotonicity			8	bit
Differential Non-Lineality	DNL	1LSB=VDD/512	-1	0	+2	LSB
		C_L=100pF				
Buffer AMP Drive Current	I_{AO}		-500		+500	uA
Analog Output Voltage		(Note4)				
max	A_{MAX}		3.70	3.75		V
min	A_{MIN}			1.25	1.30	V

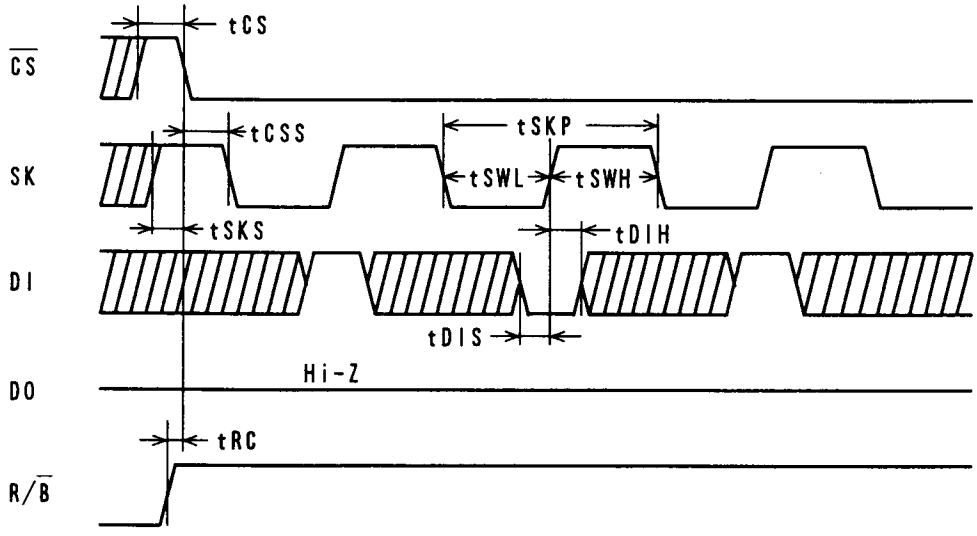
Note 4. Refer to the following section "Instruction and data format" about the relation between input data and output voltage.

■ AC Characteristics

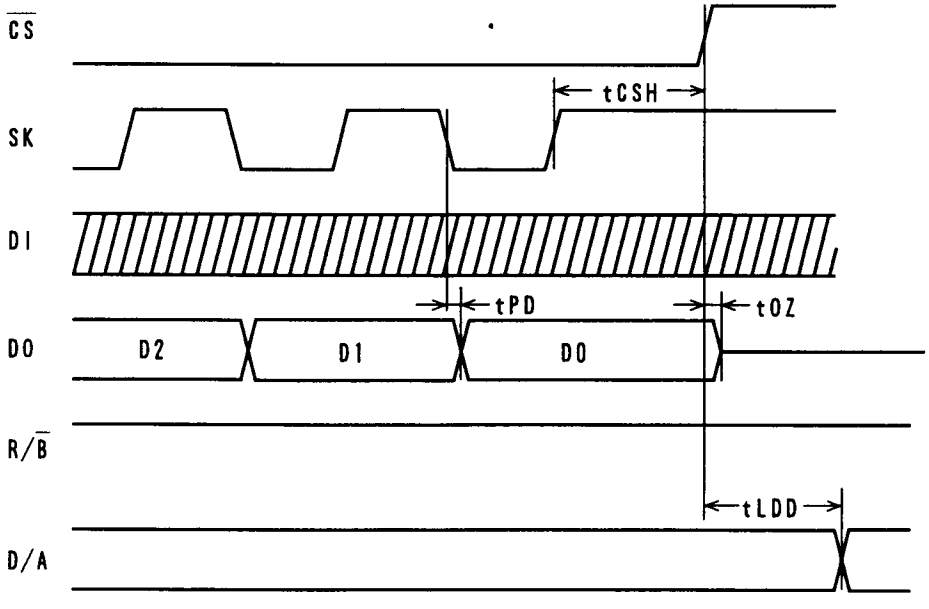
(VCC=VDD=+5V±5% , VSS=0V , Ta=-10～70℃ unless otherwise specified)

Parameter	Symbol	Condition	min	typ	max	Units
MCLK frequency	t_{CLK}		3.5		4.5	MHz
SK Period	t_{SKP}		1.0			us
SK Pulse Width "L" "H"	t_{SWL} t_{SWH}		400 400			ns ns
$\overline{CS}$ Setup Time	t_{CSS}		100			ns
$\overline{CS}$ Hold Time	t_{CSH}		100			ns
SK Setup Time	t_{SKS}		100			ns
RST Setup Time	t_{RSS}		0			ns
RST Hold Time	t_{RSH}		0			ns
Data Setup Time	t_{DIS}		200			ns
Data Hold Time	t_{DIH}		200			ns
DO, R/$\overline{B}$ Data Output Delay	t_{PD}	C_L=100pF			300	ns
Selftimed Program Time	$t_{E/W}$				10	ms
Write Recovery Time	t_{RC}		100			ns
$\overline{CS}$ "H" Time	t_{CS}		1.0			us
Output Float Delay	t_{OZ}				500	ns
DAC Output Setting Time	t_{LDD}	C_L=100pF			1	ms

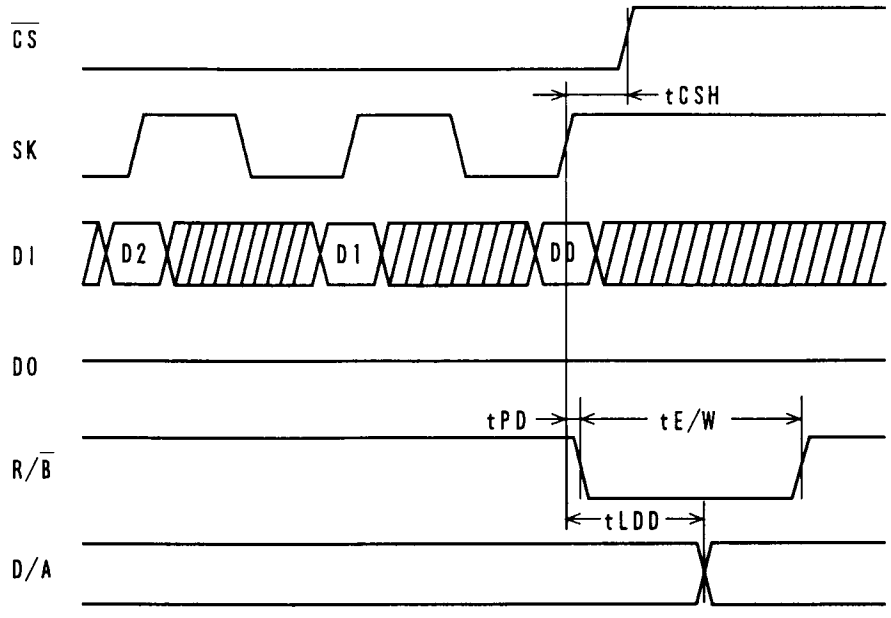
■ Timing Diagram



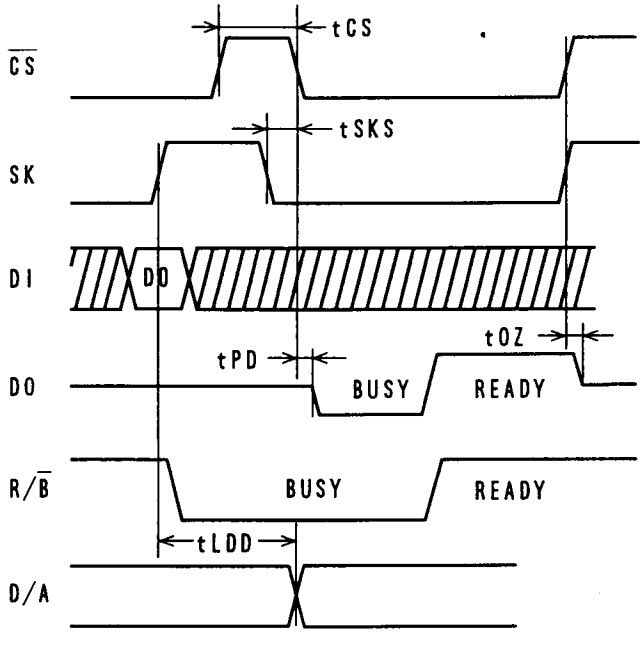
Input Command Timing



Data Latch Timing (READ)



Programming Timing (WRITE)



Status Output Timing (DO pin)

Functional Description

The op-code, address(channel of D/A) and data(outputs of D/A) are clocked into the DI pin on the rising edge of the serial clock(SK). The AK9832 has 4 instructions of READ, WRITE, WREN(Write Enable) and WRDS(Write Disable).
Each instruction consists of start bit, op-code and address. Tables 1 and 2 show the function list and the instruction set respectively. The Do pin is normally in its high-impedance state except when the AK9832 outputs data and $\overline{\text{Busy}}$/Ready signal.

Function	Comments	
READ	The data on EEPROM are output to DO pin by this instruction. The outputs of D/A are also set by the same data.	
WRITE	after WREN	The data are written to EEPROM by this instruction and the outputs of D/A are also set by the same data.
	before WREN or after WRDS	The data are set for the outputs of D/A only, but are not written to EEPROM.

Table 1. Function list

Instruction Set

Instruction	Op-code	Adress	Data	Comments
READ	1 0 1 0 1 0 0 0	A7 A6 A5 A4 A3 A2 A1 A0	D7～D0	READ
WRITE	1 0 1 0 0 1 0 0	A7 A6 A5 A4 A3 A2 A1 A0	D7～D0	WRITE
WREN	1 0 1 0 0 0 1 1	* * * * * * * *	*～	WRITE enable
WRDS	1 0 1 0 0 0 0 0	* * * * * * * *	*～	WRITE disable
TEST	1 0 1 0 0 0 0 1	* * * * * * * *	D7～D0	

*: Don't Care

TEST:TEST is used for testing purpose only. User can't use this instruction.

Table 2. Instruction Set

■ READ

The READ instruction outputs data(8-bits) of the memory at the selected address on the DO pin. When the 17th falling edge of $\overline{SK}$ is received, the Do pin will come out of high-impedance state and shift out the data at the selected address in serial form with D7 fast.

■ Write

The WRITE instruction write the data into the specified address. The AK9832 will be put into the internal programming cycle after the 24th rising edge of $\overline{SK}$ to read DO in. During the internal programming cycle ($\overline{Busy}$ state : $t_{E/W}$) and while entering write instruction the RST pin should be at low level. If the RST pin is set to high level during the internal programming cycle, the AK9832 stops execution of the internal programming and the device returns to ready status. In this case the accessed word data will be incomplete.

When entering the new command after the command is discontinued for the RST pin, $\overline{CS}$ pin should be set to high level. When the RST pin is kept at high level, the write is not executed. This becomes write protection function.

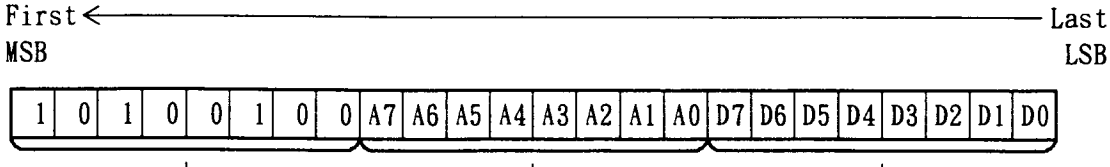
The $\overline{CS}$ pin need not be high level during internal programming cycle.

■ WREN, WRDS

Upon power-up, the AK9832 is in the programming disable (WRDS) state. Programming the EEPROM is disabled until a programming enable (WREN) instruction is executed after power-up or after an WRDS execution. Once an WREN is executed, the programming remains enabled until an WRDS is executed or the power supply is removed from the AK9832. The WRDS is provided to protect against the accidental data disturb. The READ execution is independent of both WREN and WRDS.

■ Instruction and data format

At WRITE execution, the instruction and data set consists of 24-bits as shown below. Op-code(8-bits), address(8-bits) and data(8-bits) are input into the DI pin in order. The data are output from DO pin at READ execution.



Data Bit

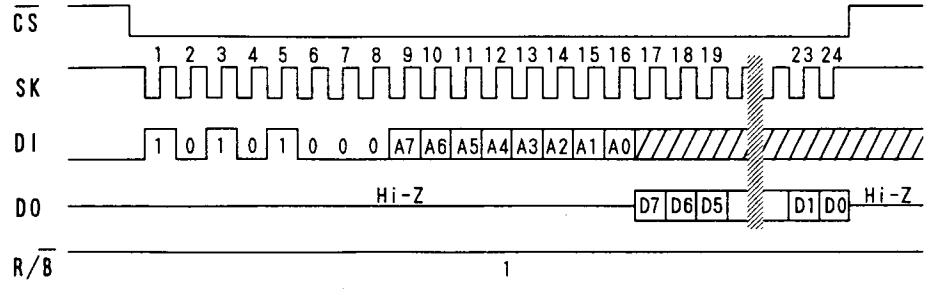
D7	D6	D5	D4	D3	D2	D1	D0	Output Voltage
0	0	0	0	0	0	0	0	≒(VDD/4)+(VDD/512)×1
0	0	0	0	0	0	0	1	≒(VDD/4)+(VDD/512)×2
↵								↵
1	1	1	1	1	1	1	0	≒(VDD/4)+(VDD/512)×255
1	1	1	1	1	1	1	1	≒VDD×3/4

Address Bit

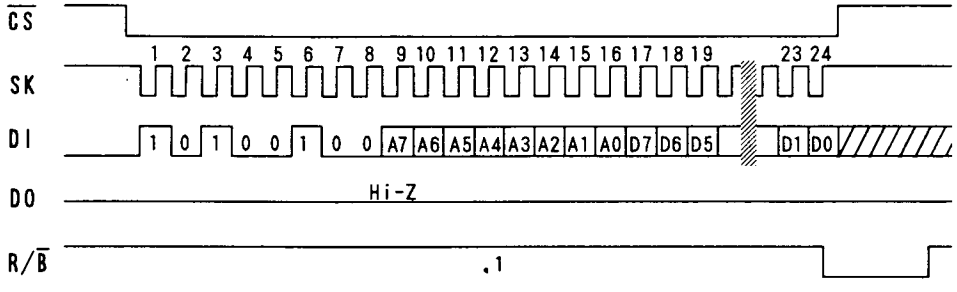
A7	A6	A5	A4	A3	A2	A1	A0	Address / Output Port	
0	0	0	0	0	0	0	0	EEPROM+ D/A	AO0
0	0	0	0	0	0	0	1		AO1
↵									↵
0	0	0	1	1	1	1	0		AO30
0	0	0	1	1	1	1	1		AO31
1	0	0	0	0	0	0	0	EEPROM	128 BOTTOM
1	0	0	0	0	0	0	1		129
↵									↵
1	1	1	1	1	1	1	1		255 TOP

■ Instruction Flow

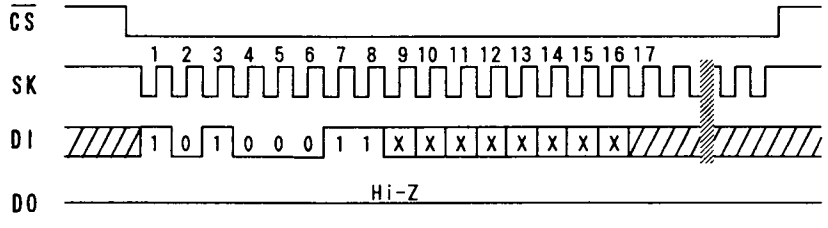
1) READ



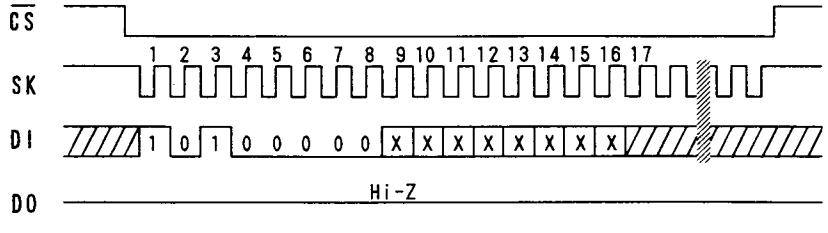
2) WRITE



3) WREN



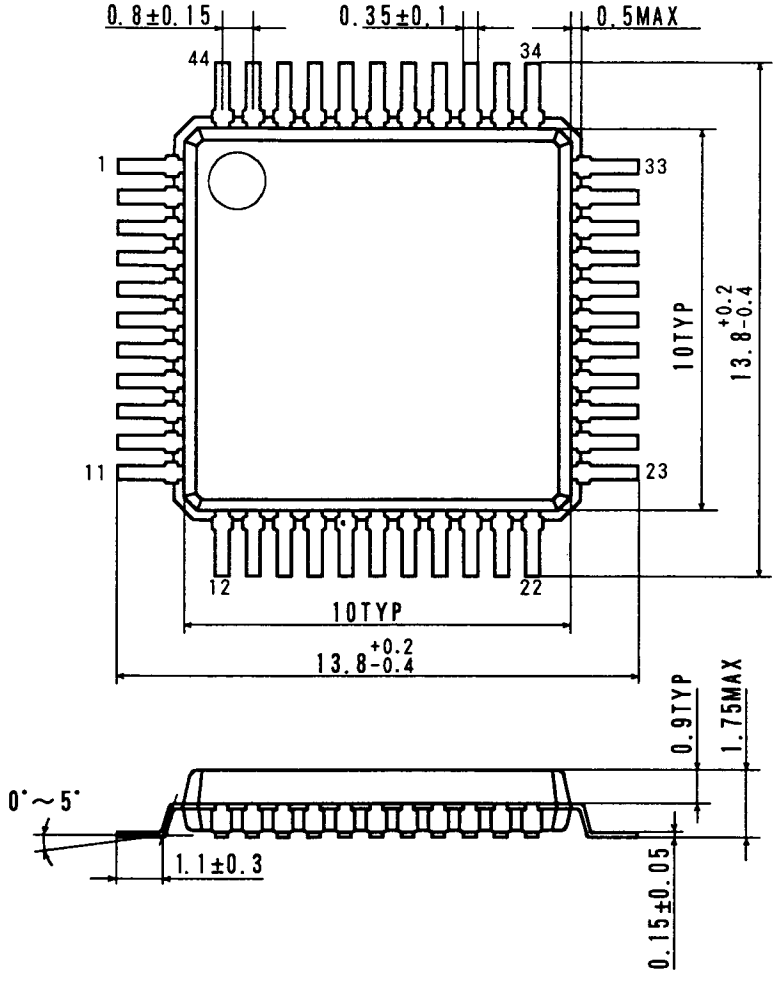
4) WRDS



Package

44pin QFP

UNIT : mm



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