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Quad Unity-Gain Video Buffer

Features

- −3-dB Bandwidth: 120 MHz
- 30-MHz Gain Flatness: 0.1 dB
- High Channel Isolation: 62 dB @ 10 MHz
- Low Differential Gain—0.08%
- Low Differential Phase—0.1°
- Low Power—P_D: 30 mW/Channel
- Fast Settling: 0.1% in 10 ns
- Low Distortion: −58 dBc @ 20 MHz

Benefits

- Flat Frequency Response
- High Color Fidelity
- Improved Transmission Accuracy
- Reduces Power Consumption
- Increases Data Throughput
- Improved Linearity
- Small Size

Applications

- Video Signal Routing
- Telecommunications
- Digital Video
- Broadcast Quality Video Systems
- HDTV Systems

Description

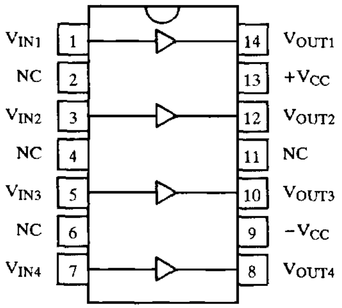
The Si584 is a monolithic closed-loop quad video buffer with a wide −3-dB bandwidth (120 MHz). Its unique design, optimized for high quality video switching, offers a high-performance alternative to conventional discrete, hybrid and open-loop buffers.

The Si584 features wide bandwidth, low power consumption, fast settling (0.1% in 10 ns), without signal degradation. Third harmonic distortion is typically −58 dBc at 20 MHz, gain flatness is typically 0.1 dB from dc to 30 MHz. These performance specifications allow the designer to improve system bandwidth while reducing system power consumption, board space and design complexity. The outputs are protected against short circuits to ground.

The Si584 is built on an advanced complementary bipolar process to achieve excellent high frequency performance. All performance is specified and rated for operation with ±5-V supplies, reducing power consumption compared with traditional ±15-V designs.

Functional Block Diagrams and Pin Configurations

Dual-In-Line and SOIC



Top View

Ordering Information

Temp Range	Package	Part Number
−40 to 85°C	14-Pin Plastic DIP	Si584DJ
	14-Pin Narrow SOIC	Si584DY

Absolute Maximum Ratings

Supply Voltage . . . . ±7 V
Input Voltage Range . . . . V− to V+
Output Current . . . . 35 mA

Storage Temperature . . . . −65 to 150°C
Lead Temperature (Soldering 10s) . . . . 300°C
Junction Temperature: T_J . . . . 175°C

P-32167—Rev. B (11/15/93)

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V− = −5 V R_L = 100 Ω, R_S = 50 Ω	Temp[a]	D Suffix −40 to 85°C Min[c]	 Typ[b]	 Max[c]	Unit
Frequency Domain[g]							
−3 dB Bandwidth[f]	SSBW	V_{OUT} = ≤ 0.5 V_{p-p}	Room Full	135 120	200		MHz
	MSBW	V_{OUT} = 1 V_{p-p}	Room		120		
	LSBW	V_{OUT} = 2 V_{p-p}	Full	70	95		
Gain Flatness Peaking[f]	GFPL	V_{OUT} ≤ 0.5 V_{p-p}, 0.1 to 30 MHz	Room Full		0	0.2 0.3	dB
	GFPH	V_{OUT} ≤ 0.5 V_{p-p}, >30 MHz	Room Full		0	0.4 0.7	
Crosstalk	X_{TALK}	f = 10 MHz	Room		62		
Time Domain[d, g]							
Rise and Fall Time	t_{RS1}	V_{IN} = 0.5 V Step	Room Full		1.8	2.8 3.0	ns
	t_{RS2}	V_{IN} = 2 V Step	Room Full		5	7 8	
Settling Time	t_S	V_{IN} = 2 V Step	Room Full		10	15 20	
Overshoot	OS	V_{IN} = 0.5 V Step	Room Full		3	10 15	%
Slew Rate	SR		Room Full	200 180	450		V/µs
Static, dc							
Small Signal Gain[d]	GA		Room Full	0.96 0.95	0.97		V/V
Integral Endpoint Linearity[d]	I_{LIN}	±1 V Full Scale	Room		0.4	0.6	%
Output Offset Voltage[e]	VIO		Room Full		±0.5	±5 ±8.2	mV
Input Offset Voltage Average Temperature Coefficient[e]	DVIO		Room Full		±9	 ±40	µV/°C
Input Bias Current[e]	I_B		Room Full		±1	±5 ±10	µA
Power Supply Rejection Ratio[e]	PSRR		Room Full	48 46	56		dB
Supply Current, Total[e]	I+	No Load	Room Full		12	16.5 17	mA
Miscellaneous							
Input Resistance	R_{IN}		Room Full	1 0.3	1.5		MΩ
Input Capacitance	C_{IN}		Room Full		1.8	3 3.5	pF
Output Impedance	R_O	At dc	Room Full		2.5	3.5 5	Ω
Output Voltage Range	V_O	No Load	Room Full	±3.8 ±3.6	±4		V
Output Current, per Buffer[d]	I_O		Room Full	±20 ±12	±25		mA
2nd Harmonic Distortion[f]	HD_2	V_{IN} = 2 V_{p-p}, f_{IN} = 20 MHz	Room Full		−50	−38 −36	dBc
3rd Harmonic Distortion[f]	HD_3	V_{IN} = 2 V_{p-p}, f_{IN} = 20 MHz	Room Full		−58	−50 −45	
Equivalent Input Noise Floor[d]	SNF	f >100 kHz, 50 Ω on Input	Room Full		−155	−153 −152	dBm (1 Hz)

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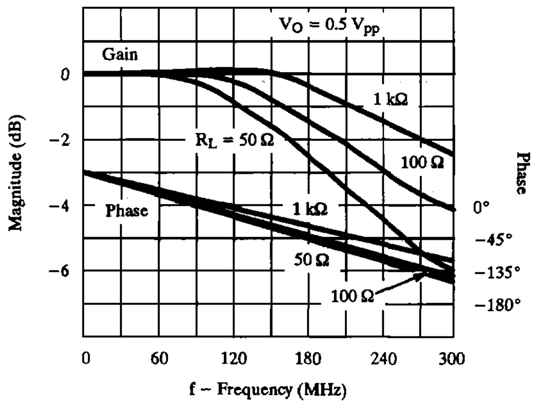
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V− = −5 V R_L = 100 Ω, R_S = 50 Ω		Temp[a]	D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Performance Driving a DG884 Crosspoint Switch[d, g]								
2nd Harmonic Distortion	HD_2	See Test Load See Figure 1	V_{IN} = 2 V_{p-p} f_{IN} = 5 MHz	Room		−60		dBc
3rd Harmonic Distortion	HD_3			Room		−58		
Differential Phase	DP		f = 3.58 or 4.43 MHz	Room		0.1		deg
Differential Gain	DG			Room		0.08		%
Crosstalk (All Hostile)	$X_{TALK(AH)}$		f = 10 MHz	Room		−54		dB

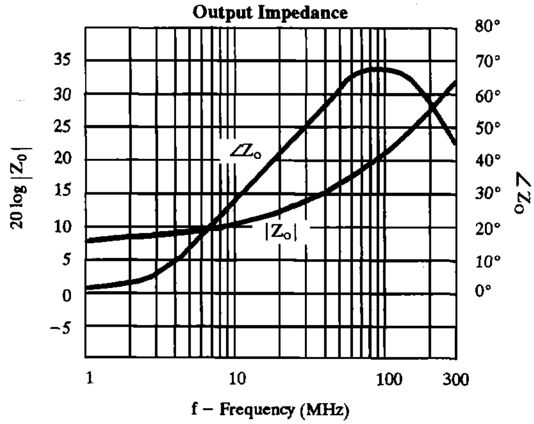
Notes:
a. Room = 25°C, Full = −40 to 85°C.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. Parameter is 100% tested at 25°C and sample tested at 85°C.
f. Parameter is sample tested at 25°C.
g. AC performance is very dependent on layout. Specifications apply only in a 50-Ω microstrip environment.

Typical Characteristics: $T_A = 25°C, V_{CC} = \pm 5\ V, R_L = 100\ \Omega$

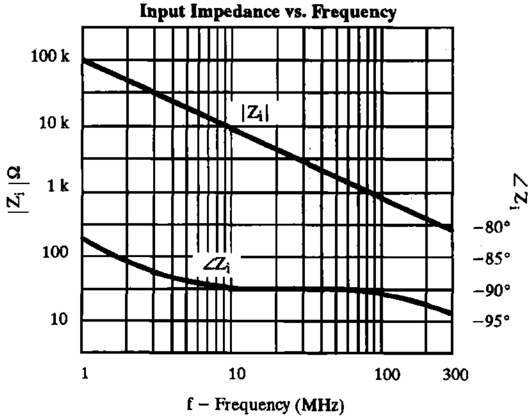
Gain and Phase vs. Load



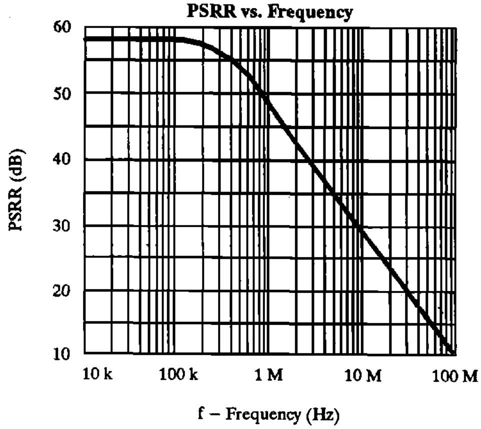
Output Impedance



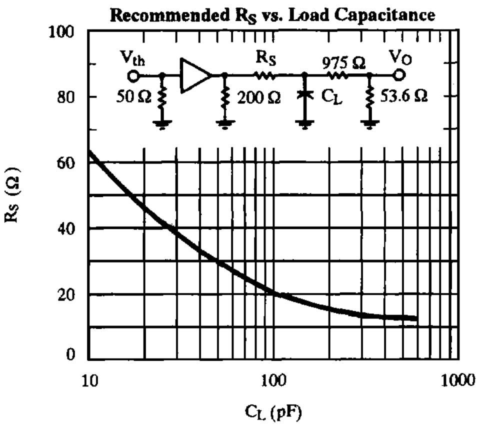
Input Impedance vs. Frequency

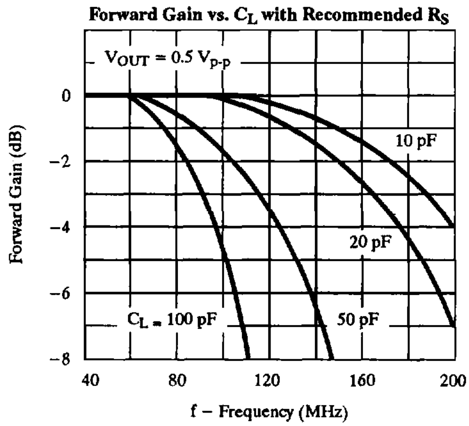


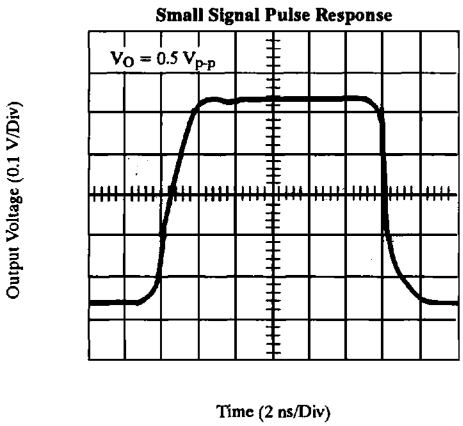
PSRR vs. Frequency

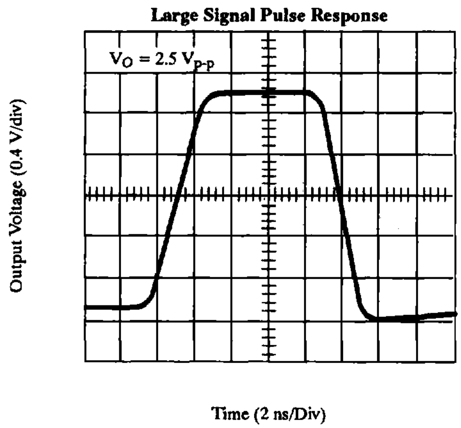


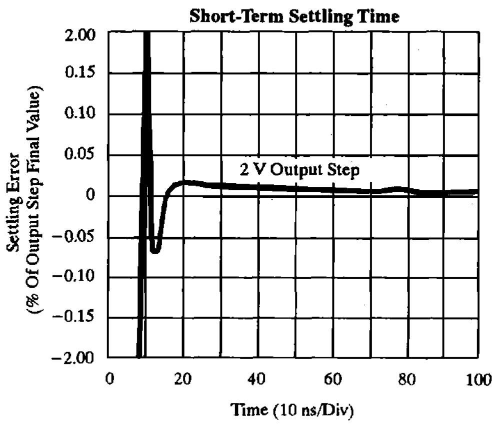
Typical Characteristics: $T_A = 25°C$, $V_{CC} = \pm 5$ V, $R_L = 100\ \Omega$ (Cont'd)

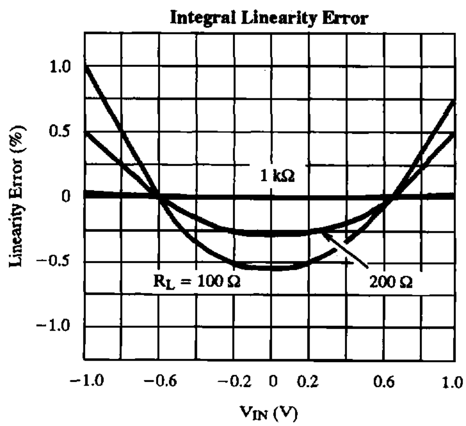












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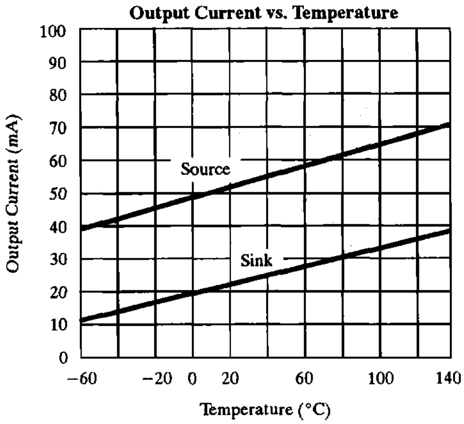
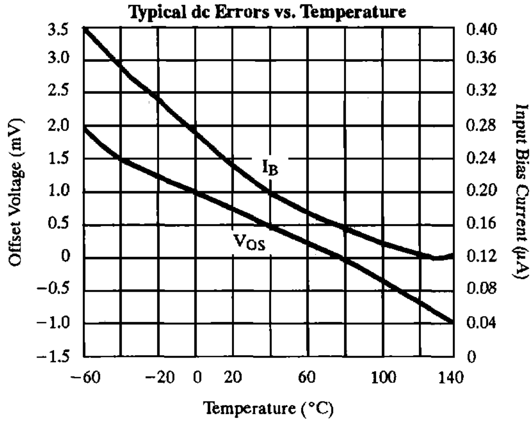
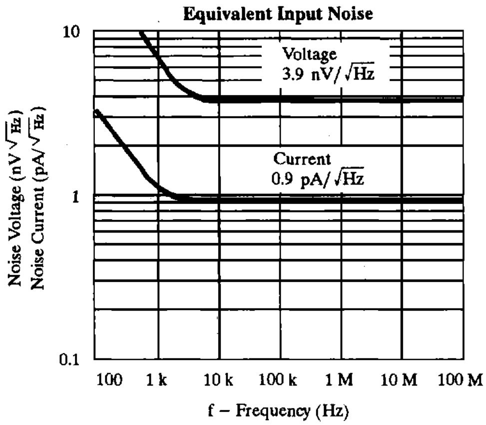
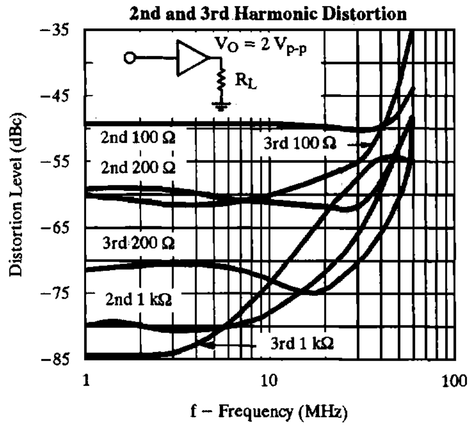
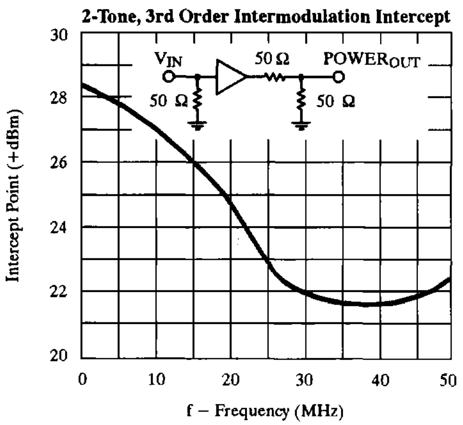
Typical Characteristics: $T_A = 25°C, V_{CC} = \pm5 V, R_L = 100 \Omega$ (Cont'd)

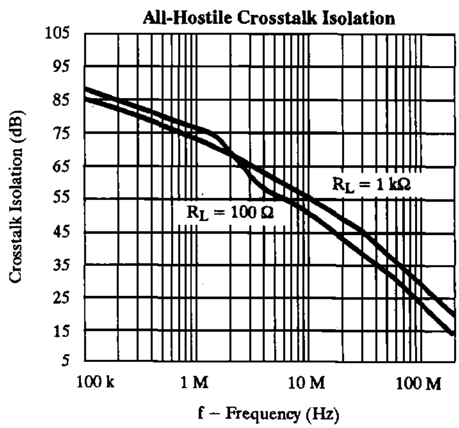












Test Circuit

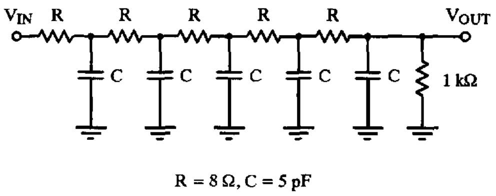


Figure 1. Test Load

Applications

Operation

The Si584 is a quad unity gain buffer that offers high-speed and low-power operation. Its closed loop topology provides higher accuracy than that normally found in open loop designs. The Si584 was designed to optimize differential gain and phase when driving the distributed capacitance of a video multiplexer or crosspoint such as the DG884.

Board Layout and Crosstalk

High frequency designs demand good PC board layout for best performance. A ground plane and power supply bypassing with high-frequency ceramic capacitors adjacent to the power supply pins are essential. Second harmonic distortion can be improved by ensuring equal current return paths for both the positive and negative supplies. This is accomplished by connecting one side of the bypass capacitors at the same point in the ground plane while keeping the supply sides within 0.1" of the Si584 supply pins.

Crosstalk is strongly dependent on board layout. Closely spaced signal traces on the board will degrade crosstalk due to capacitive coupling. A grounded guard trace between signal traces will reduce crosstalk by reducing intertrace capacitance. For this same reason it is recommended that unused pins (2, 4, 6, 11) be connected to the ground plane.

"All-Hostile" crosstalk is measured by driving three of the four buffers simultaneously while observing the fourth, undriven, channel.

Unused Buffers

It is recommended that the inputs of any unused buffers be tied to ground through 50-Ω resistors.

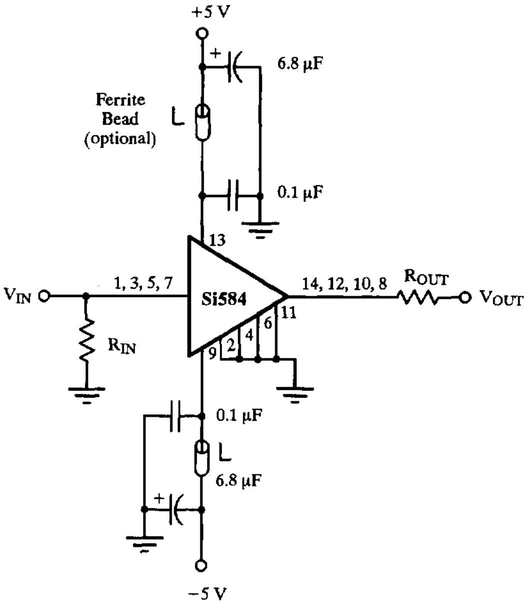


Figure 2. Decoupling the Si584

Minimum Parts Count 80-MHz Video Switcher

Figure 3 illustrates a fully buffered 8 × 4 video switching matrix capable of handling 80-MHz signals with only four ICs. At the heart of this circuit is the DG884 crosspoint. U1 and U2 buffer all eight inputs while U4 can drive a second level of switching elements.

Applications (Cont'd)

It is worth noting that every time a video signal is processed by an active or passive component, its bandwidth is subject to a reduction due to each individual processing element's own bandwidth. That is why, even when switching baseband video, it is better to use a broadband switcher in order to preserve signal quality and fidelity.

For lower bandwidth applications one Si584 output can drive up to four DG884 inputs. This is useful when building larger matrices (8 × 8, 8 × 16, etc.).

Providing the receiving end is properly terminated, the Si584 can also be used as a cable driver for short distances. When driving long cables that may or may not be properly terminated it is better to use a back terminated cable driver with a 6-dB gain. This driving method reduces transmission line reflections. The Si582 is recommended for this type of application.

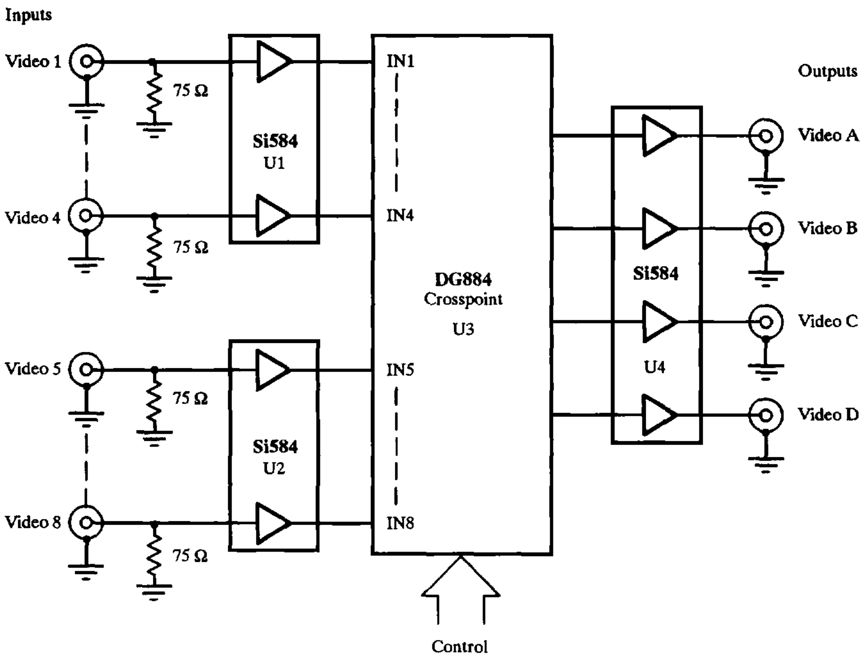


Figure 3. Minimum Parts Count 80 MHz 8 × 4 Video Switching Matrix