NEC

MOS INTEGRATED CIRCUIT
MC-422000FA64FB

2 M-WORD BY 64-BIT DYNAMIC RAM MODULE
HYPER PAGE MODE

Description

The MC-422000FA64FB is a 1,048,576 words by 64 bits dynamic RAM module on which 8 pieces of 16 M DRAM: μPD4218165 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 2,096,152 words by 64 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle Time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-422000FA64-60	60 ns	104 ns	25 ns	3.73 W	357 mW (CMOS level input)
MC-422000FA64-70	70 ns	124 ns	30 ns	3.52 W	

- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

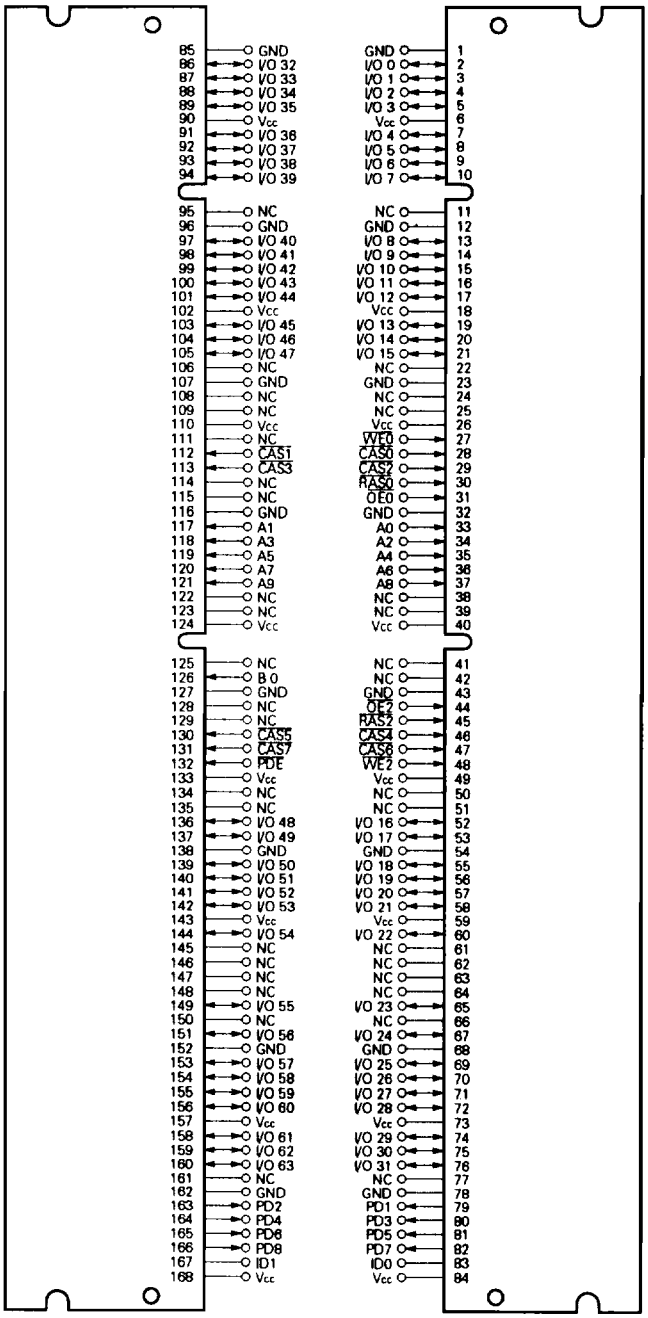
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000FA64FB-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	8 pieces of μPD4218165LE (400 mil SOJ) [Single side]
MC-422000FA64FB-70	70 ns		

Document No. M10559EJ1V0DSU1

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



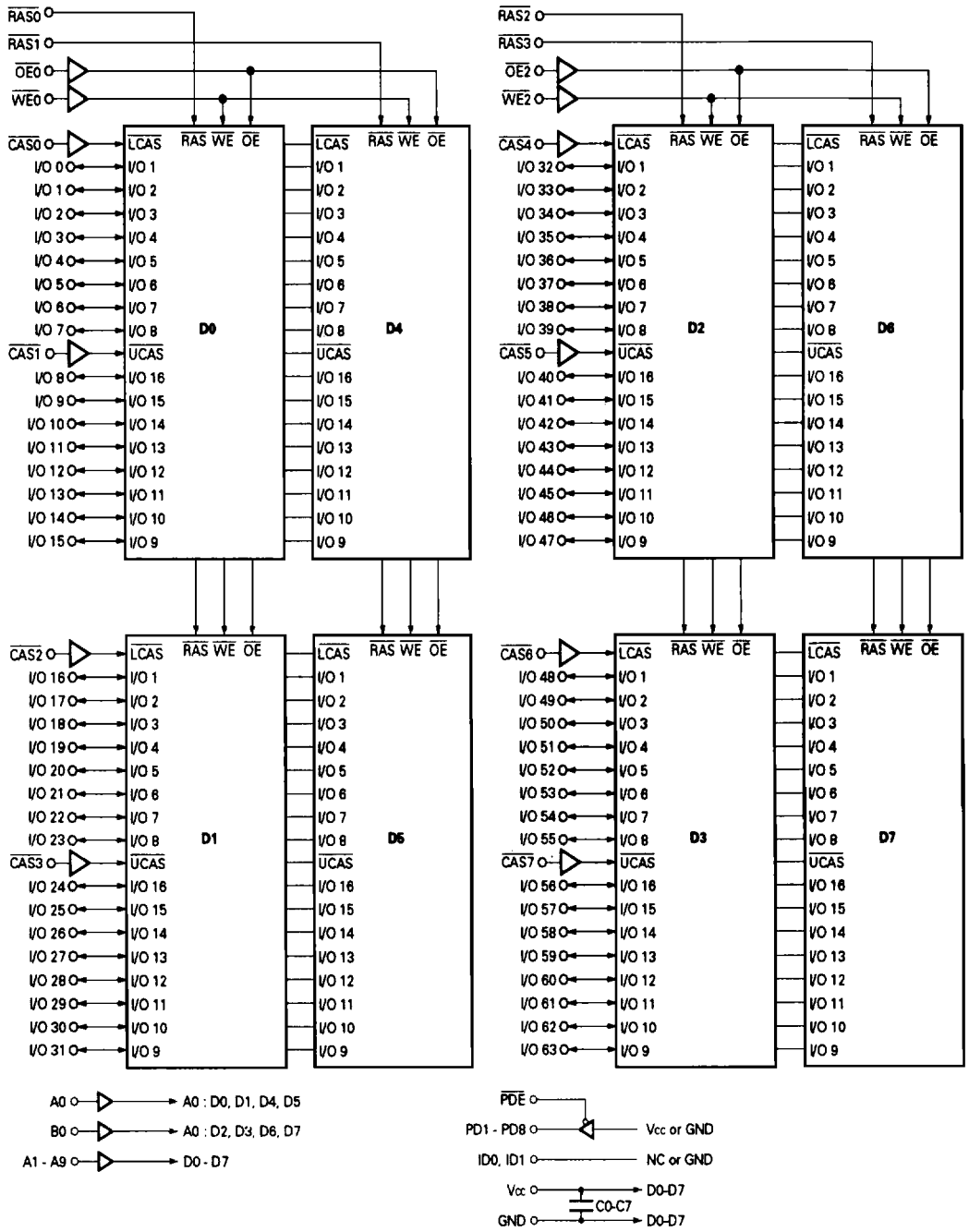
PD and ID Table

Pin Name	Pin No.	Access Time	
		60 ns	70 ns
PD1	79	H	H
PD2	163	L	L
PD3	80	H	H
PD4	164	L	L
PD5	81	H	H
PD6	165	H	L
PD7	82	H	H
PD8	166	H	H
ID0	83	GND	GND
ID1	167	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A9, B0 : Address Inputs
I/O 0 - I/O 63 : Data Inputs/Outputs
$\overline{RAS0}$ - $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D7 : μPD4218165

Electrical Specifications [Notes 1, 2]

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		6	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS2}$			45	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS7}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O63			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

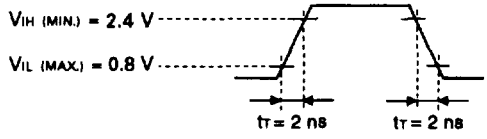
Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			710	mA	1,2,3
			t_{RAC} = 70 ns			670		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH(MIN.)}$, I_O = 0 mA				76	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA				68		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			710	mA	1,2,3,4
			t_{RAC} = 70 ns			670		
Operating current (Hyper page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL(MAX.)}$ $\overline{CAS}$ Cycling $t_{HPC} = t_{HPC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			510	mA	1,2,5
			t_{RAC} = 70 ns			470		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			710	mA	1,2
			t_{RAC} = 70 ns			670		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V all other pins not under test = 0 V		$\overline{RAS}$	–10	+10	μA	
				others	–5	+1		
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)			–10	+10	μA	
High level output voltageLow	V_{OH}	I_O = –2.5 mA			2.4		V	
level output voltage	V_{OL}	I_O = +2.1 mA				0.4	V	

Notes
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).
2. Specified values are obtained with outputs unloaded.
3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL(MAX.)}$ and $\overline{CAS} \geq V_{IH(MIN.)}$.
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

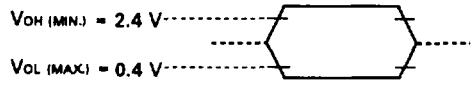
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write Cycle

Parameter	Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	tRC	104	—	124	—	ns	
$\overline{RAS}$ Precharge Time	tRP	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	tCPN	10	—	10	—	ns	
$\overline{RAS}$ Pulse Width	tRAS	60	10 000	70	10 000	ns	
$\overline{CAS}$ Pulse Width	tCAS	10	10 000	12	10 000	ns	
$\overline{RAS}$ Hold Time	tRSH	10	—	12	—	ns	
$\overline{CAS}$ Hold Time	tCSH	40	—	50	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	tRAD	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	—	5	—	ns	2
Row Address Setup Time	tASR	5	—	5	—	ns	
Row Address Hold Time	tRAH	10	—	10	—	ns	
Column Address Setup Time	tASC	0	—	0	—	ns	
Column Address Hold Time	tCAH	10	—	12	—	ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	tOES	0	—	0	—	ns	
$\overline{CAS}$ to Data Setup Time	tCLZ	0	—	0	—	ns	
$\overline{OE}$ to Data Setup Time	tOLZ	0	—	0	—	ns	
$\overline{OE}$ to Data Delay Time	tOED	13	—	15	—	ns	
Masked Byte Write Hold Time Referenced to $\overline{RAS}$	tMRH	0	—	0	—	ns	
Transition Time (Rise and Fall)	tT	1	50	1	50	ns	
Refresh Time	tREF	—	16	—	16	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\,(MAX.)}$ and $t_{RCD} \leq t_{RCD\,(MAX.)}$	$t_{RAC\,(MAX.)}$	$t_{RAC\,(MAX.)}$
$t_{RAD} > t_{RAD\,(MAX.)}$ and $t_{RCD} \leq t_{RCD\,(MAX.)}$	$t_{AA\,(MAX.)}$	$t_{RAD} + t_{AA\,(MAX.)}$
$t_{RCD} > t_{RCD\,(MAX.)}$	$t_{CAC\,(MAX.)}$	$t_{RCD} + t_{CAC\,(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	23	ns	1
Access Time from Column Address	t_{AA}	—	35	—	40	ns	1
Access Time from $\overline{OE}$	t_{OEA}	—	20	—	23	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	—	35	—	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	2
Output buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
$\overline{CAS}$ Hold Time to $\overline{OE}$	t_{CHO}	5	—	5	—	ns	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\,(MAX.)}$ and $t_{RCD} \leq t_{RCD\,(MAX.)}$	$t_{RAC\,(MAX.)}$	$t_{RAC\,(MAX.)}$
$t_{RAD} > t_{RAD\,(MAX.)}$ and $t_{RCD} \leq t_{RCD\,(MAX.)}$	$t_{AA\,(MAX.)}$	$t_{RAD} + t_{AA\,(MAX.)}$
$t_{RCD} > t_{RCD\,(MAX.)}$	$t_{CAC\,(MAX.)}$	$t_{RCD} + t_{CAC\,(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.
3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not refernced V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10	—	10	—	ns	1
$\overline{WE}$ Pulse Width	t_{WP}	10	—	10	—	ns	1
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	15	—	17	—	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	10	—	12	—	ns	
$\overline{WE}$ Setup Time	t_{WCS}	0	—	0	—	ns	2
$\overline{OE}$ Hold Time	t_{OEH}	0	—	0	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	ns	3
Data-in Hold Time	t_{DH}	10	—	10	—	ns	3

Notes 1. $t_{WP(MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH(MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t_{RWC}	133	—	157	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	87	—	99	—	ns	1
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	32	—	37	—	ns	1
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	52	—	59	—	ns	1

Note 1. If $t_{WCS} \geq t_{WCS(MIN.)}$ the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD(MIN.)}$, $t_{CWD} \geq t_{CWD(MIN.)}$, $t_{AWD} \geq t_{AWD(MIN.)}$, and $t_{CPWD} \geq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{HPC}	25	—	30	—	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	60	125 000	70	125 000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	10	10 000	12	10 000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	52	—	59	—	ns	2
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	ns	
Read Modify Write Cycle Time	t_{HPRWC}	66	—	75	—	ns	
Data Output Hold Time	t_{DHC}	5	—	5	—	ns	
$\overline{OE}$ to CAS Hold Time	t_{OCH}	5	—	5	—	ns	
$\overline{OE}$ Precharge Time	t_{OEP}	5	—	5	—	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	3,4
$\overline{WE}$ Pulse Width	t_{WPZ}	10	—	10	—	ns	4
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	3.4
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	3.4

Notes 1. $t_{HPC(MIN.)}$ is applied to access time from $\overline{CAS}$

2. If $t_{WCS} \geq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $t_{RWD} \geq t_{RWD(MIN.)}$, $t_{CWD} \geq t_{CWD(MIN.)}$, $t_{AWD} \geq t_{AWD(MIN.)}$, and $t_{CPWD} \geq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

   (1) $\overline{RAS}$, $\overline{CAS}$: Inactive (at the end of read cycle)

   $\overline{WE}$: inactive, $\overline{OE}$: active

   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.

   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)

   $\overline{WE}$: inactive, $\overline{OE}$: inactive ··· t_{OEZ} is effective.

   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)

   $\overline{WE}$,$\overline{OE}$:active and either t_{RRH} or t_{RCH} must be met··· t_{WEZ}, t_{WPZ} are effective.

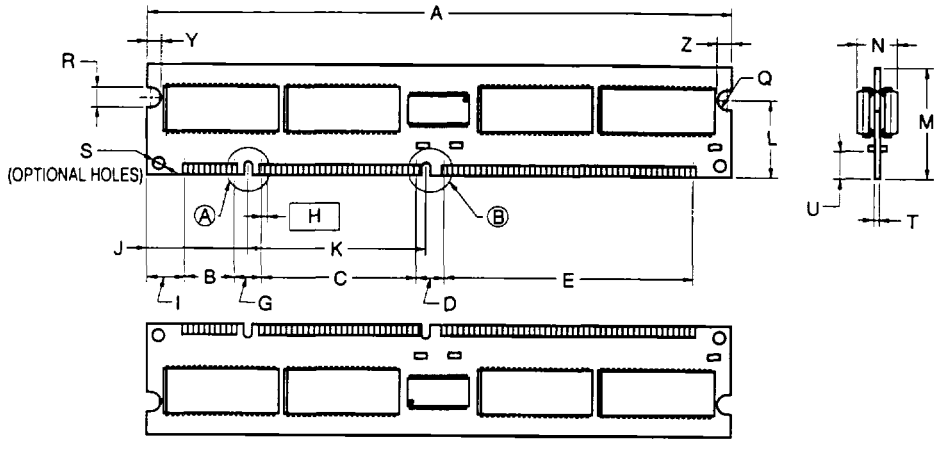
Refresh Cycle

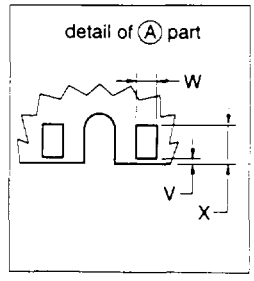
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	—	5	—	ns	
$\overline{WE}$ Hold Time (Hidden Refresh Cycle)	t_{WHR}	15	—	15	—	ns	

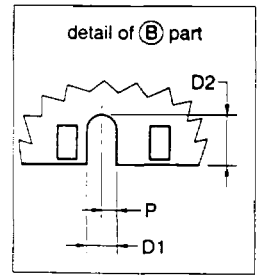
Timing Chart
Please refer to Timing Chart 1, page 365.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.1230
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.05 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.7000
M	25.4±0.13	1.000±0.006
N	9.0 MAX.	0.355 MAX.
P	1.0	0.039
Q	R 2.0	R 0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

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