CRYSTAL OSCILLATOR (SPXO)
OUTPUT : LV-PECL, LVDS

SG3225 / 5032 / 7050EEN
SG3225 / 5032 / 7050VEN

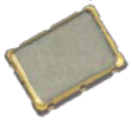
Pb Free RoHS Compliant

Product Number
SG3225EEN: X1G005221xxxx00 (fo ≤ 200 MHz)
X1G005511xxxx00 (fo > 200 MHz)
SG5032EEN: X1G005531xxxx00
SG7050EEN: X1G005131xxxx00 (fo ≤ 200 MHz)
X1G005551xxxx00 (fo > 200 MHz)
SG3225VEN: X1G005351xxxx00 (fo ≤ 200 MHz)
X1G005521xxxx00 (fo > 200 MHz)
SG5032VEN: X1G005541xxxx00
SG7050VEN: X1G005331xxxx00 (fo ≤ 200 MHz)
X1G005561xxxx00 (fo > 200 MHz)

- Frequency range : 25 MHz to 500 MHz
- Supply voltage : 2.5 V Typ. / 3.3 V Typ.
- Output : LV-PECL or LVDS
- Function : Output enable (OE)
- Phase jitter : 50 fs Typ. (fo = 156.25 MHz, LV-PECL)
- Operating temperature : -40 C to +105 C


SG3225EEN
SG3225VEN
(3.2 x 2.5 x 1.05 mm)


SG5032EEN
SG5032VEN
(5.0 x 3.2 x 1.3 mm)


SG7050EEN
SG7050VEN
(7.0 x 5.0 x 1.5 mm)

Specifications (characteristics)

Item	Symbol	Specifications LV-PECL: SG3225EEN / SG5032EEN / SG7050EEN	Specifications LVDS: SG3225VEN / SG5032VEN / SG7050VEN	Conditions / Remarks	
Output frequency range	fo	25 MHz to 500 MHz		Except for SG5032EEN / SG5032VEN	Please contact us for available frequencies.
		200.1 MHz to 500 MHz		SG5032EEN / SG5032VEN	
Supply voltage	V_{CC}	D: 2.5 V ± 0.125 V, C: 3.3 V ± 0.165 V			
Storage temperature	T_stg	-55 C to +125 C			
Operating temperature	T_use	G: -40 C to +85 C, H: -40 C to +105 C			
Frequency tolerance	f_tol	D: ±25 × 10^{-6} Max.		Includes initial frequency tolerance, temperature variation, supply voltage change and 5 years aging (+25 °C)	Refer to figure *1
		J: ±50 × 10^{-6} Max.		Includes initial frequency tolerance, temperature variation, supply voltage change and 10 years aging (+25 °C)	
		L: ±100 × 10^{-6} Max.			
Current consumption	I_{CC}	60 mA Max.	25 mA Max.	OE = V_{CC}, L_ECL = 50 Ω or L_LVDS = 100 Ω	
Disable current	I_dis	25 mA Max.	15 mA Max.	OE = GND	
Symmetry	SYM	45 % to 55 %		At output crossing point	
Output voltage (LV-PECL)	V_{OH}	V_{CC} - 1.1 V Min.	–	DC characteristics	
	V_{OL}	V_{CC} - 1.5 V Max.	–		
Output voltage (LVDS)	V_{OD}	–	250 mV to 450 mV	Differential output voltage, V_{OD1}, V_{OD2}	DC characteristics
	dV_{OD}	–	50 mV Max.	dV_{OD} = | V_{OD1} - V_{OD2} |	
	V_{OS}	–	1.15 V to 1.35 V	Offset voltage, V_{OS1}, V_{OS2}	
	dV_{OS}	–	50 mV Max.	dV_{OS} = | V_{OS1} - V_{OS2} |	
Output load condition	L_ECL	50 Ω	–	Terminated to V_{CC} - 2.0 V	
	L_LVDS	–	100 Ω	Connected between OUT to $\overline{OUT}$	
Input voltage	V_{IH}	70 % V_{CC} Min.		OE terminal	
	V_{IL}	30 % V_{CC} Max.			
Rise/Fall times	tr / tf	0.35 ns Max.	0.3 ns Max.	V_{CC} = 2.5 V, 25 MHz ≤ fo ≤ 200 MHz	LV-PECL: Between 20 % and 80 % of (V_{OH} - V_{OL}) LVDS: Between 20 % and 80 % of Differential Output peak to peak voltage
		0.3 ns Max.		All other	
Startup time	t_str	10 ms Max.		Time at minimum supply voltage to be 0 s	

Phase Jitter

Product Name	100 MHz	125 MHz	156.25 MHz	200 MHz	312.5 MHz	491.52 MHz	Conditions
SG3225EEN / SG5032EEN / SG7050EEN	75 fs Typ.	60 fs Typ.	50 fs Typ.	40 fs Typ.	30 fs Typ.	20 fs Typ.	Offset frequency:
SG3225VEN / SG5032VEN / SG7050VEN	90 fs Typ.	70 fs Typ.	60 fs Typ.	50 fs Typ.	40 fs Typ.	30 fs Typ.	12 kHz to 20 MHz

Product Name (Standard form): SG3225 EEN 156.250000MHz C D G A (⑤⑥: Unavailable code DH, DG and JH at fo > 200 MHz, Refer to figure *1)

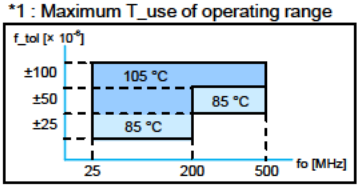
①Model ②Output (E: LV-PECL, V: LVDS) ③Frequency ④Supply voltage
⑤Frequency tolerance ⑥Opera ing temperature ⑦Internal identification code("A" is default)

④Supply voltage	
C	3.3 V Typ.
D	2.5 V Typ.

⑤Frequency tolerance	
D	±25 × 10^{-6}
J	±50 × 10^{-6}
L	±100 × 10^{-6}

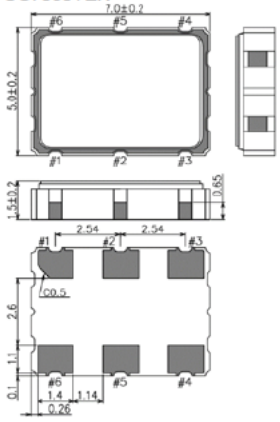
⑥Operating temperature	
G	-40 to +85 C
H	-40 to +105 C

*1 : Maximum T_use of operating range

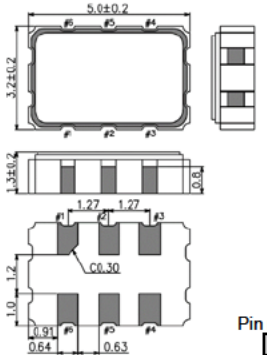


External dimensions (Unit:mm)

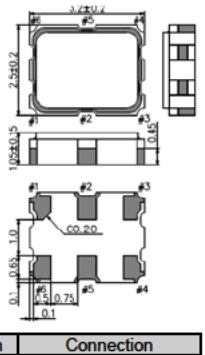
SG7050EEN
SG7050VEN



SG5032EEN
SG5032VEN



SG3225EEN
SG3225VEN

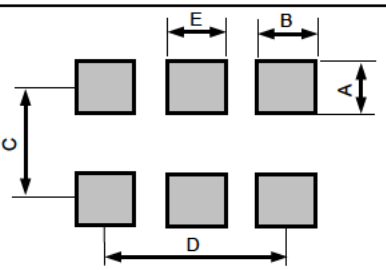


Pin map

Pin	Connection
1	OE
2	N.C. (Open or V_{CC})
3	GND
4	OUT
5	$\overline{OUT}$
6	V_{CC}

Note:
OE pin = HIGH or "Open": Specified frequency output.
OE pin = LOW: Output is high impedance

Footprint (Recommended) (Unit:mm)



	SG3225EEN SG3225VEN	SG5032EEN SG5032VEN	SG7050EEN SG7050VEN
A	1.05	1.60	2.00
B	0.92	0.89	1.80
C	1.85	2.60	4.20
D	2.58	2.54	5.08
E	0.80	0.89	1.80

In order to achieve optimum jitter performance, it is recommended that 0.1 µF and 10 µF bypass capacitors should be connected between V_{CC} and GND and placed as close to the V_{CC} pin as possible.