NEC®

DUAL EXCLUSIVE OR/NOR GATE

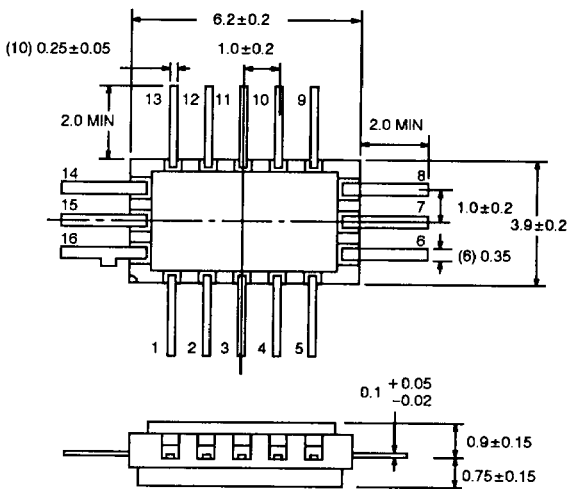
UPG710B
UPG710P

FEATURES

- **LOGIC LEVELS AND SUPPLY VOLTAGES ARE ECL COMPATIBLE**
- **ULTRAHIGH SPEED OPERATION** (Maximum Clock Frequency is typically 2.5 GHz)
- **HERMETICALLY SEALED PACKAGE ASSURES HIGH RELIABILITY**

OUTLINE DIMENSIONS (Units in mm)

OUTLINE H16



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DD}	Supply Voltage	V	+4
V_{SS1}	Supply Voltage	V	V_{DD} −4
V_{SS2}	Supply Voltage	V	−8
V_{IN}	Input Voltage	V	V_{DD} − V_{SS2}
T_{STG}	Storage Temperature	°C	−65 to +175
T_C	Operating Case Temperature	°C	−40 to +125

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

PART NUMBER PACKAGE OUTLINE			UPG710B, UPG710P H16		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
I_{SS2}	Supply Current at V_{DD} = 0 V, V_{SS1} = −2 V, V_{SS2} = −5.2 V	mA		230	
V_{OH}[1]	High Level Output Voltage at V_{DD} = 0 V, V_{SS1} = −2 V, V_{SS2} = −5.2 V	V	−1	−0.8	−0.6
V_{OL}[1]	Low Level Output Voltage at V_{DD} = 0 V, V_{SS1} = −2 V, V_{SS2} = −5.2 V	V	−2	−1.8	−1.6
f_{MAX}	Maximum Clock Frequency at V_{DD} = 0 V, V_{SS1} = −2 V, V_{SS2} = −5.2 V	Gb/s	2	2.5	3
t_{PD}	Propagation Delay at V_{DD} = 0 V, V_{SS1} = −2 V, V_{SS2} = −5.2 V	ps		360	500
t_R[2]	Output Rise Time at V_{DD} = 0 V, V_{SS1} = −2 V, V_{SS2} = −5.2 V	pS		110	200
t_F[2]	Output Fall Time at V_{DD} = 0 V, V_{SS1} = −2 V, V_{SS2} = −5.2 V	pS		110	200

Notes:

1. The V_{OH} and V_{OL} values are measured when the output and V_{TT} are connected with a 50 Ω load to V_{TT}.
2. The time from 20% to 80% (t_R), 80% to 20% (t_F) of the output voltage.

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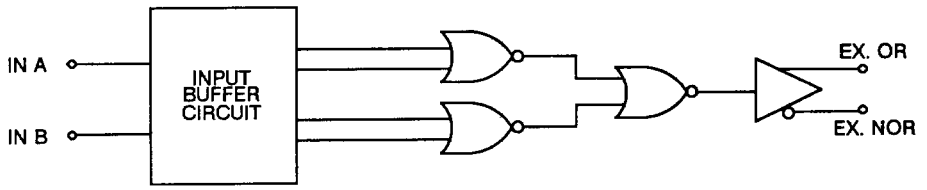
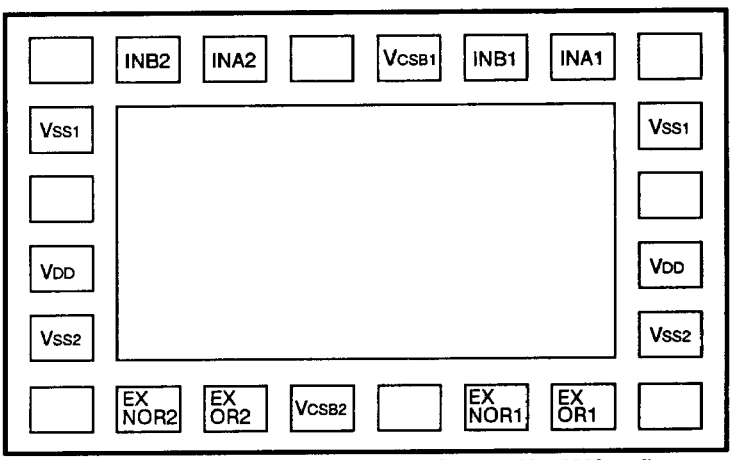
LOGIC DIAGRAM



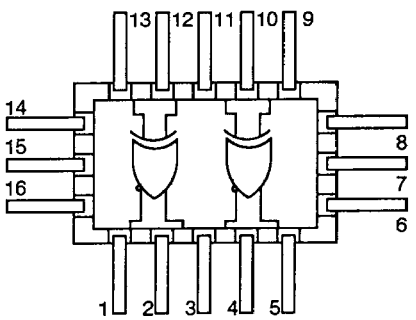
CHIP DIMENSIONS (Units in μm)

UPG710P (CHIP)



Pad Size (100 x 100 μm²) Chip Size (1400 x 2000 μm²)

UPG710B CONNECTION DIAGRAM



PIN NUMBER	CONNECTION	PIN NUMBER	CONNECTION
1	EXNOR2	9	INA1
2	EXOR2	10	INB1
3	V_{CSB2}	11	V_{CSB1}
4	EXNOR1	12	INA2
5	EXOR1	13	INB2
6	V_{SS2}	14	V_{SS1}
7	V_{DD}	15	V_{DD}
8	V_{SS1}	16	V_{SS2}

HANDLING PRECAUTIONS

1) There are multiple power supplies for this device. Careful selection of clean output power supplies is necessary to achieve best performances.

2) The metallized section on the back surface of the package, which used as a heat sink, is shared with VSS2 terminal (VSS = -5.2 normally). Do not ground the metallized section to GND (0 V) in order to prevent short circuit with VDD = 0 V normally on some other terminals.

3) When handling the device a ground strap should be used to prevent Electric Static Discharge (ESD) that can damage the GaAs MES FETs in the IC.