Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Am29C983/Am29C983A

9-Bit x 4-Port Multiple Bus Exchange

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Four bidirectional I/O ports with latches**
  - Replaces several bidirectional latches and transceivers
  - Permits multiple bus communication
  - Allows two independent communication channels
  - TTL compatibility
- **9-bit wide ports to handle byte parity**
- **Two selection inputs per port**
  - Independent port interconnect control
  - Increased flexibility in data routing
- **Matched port decoding**
  - Simplifies external decode logic
  - Easily cascadable for wider buses
- **Latches for incoming and outgoing data**
  - Independent controls permit selective data capture
  - Ideal for stored operation
  - Readback feature for system diagnostics
- **Glitch-free outputs during power-up/down**
  - No power-up sequencing needed
  - Ideal for card-edge interface
- **48 mA output drive**
  - High-capacitance bus driving
- **High-performance CMOS**
  - Low stand-by power consumption
- **Two speeds available**
  Am29C983
  - 9 ns (typical) port-to-port delay
  - 10 ns (typical) select-to-port delay

  Am29C983A
  - 6 ns (typical) port-to-port delay
  - 7 ns (typical) select-to-port delay
- **Available in 68-pin PLCC package and 80-pin PQFP package for commercial applications**
- **Available in 68-pin PGA package for military applications (Am29C983 only)**

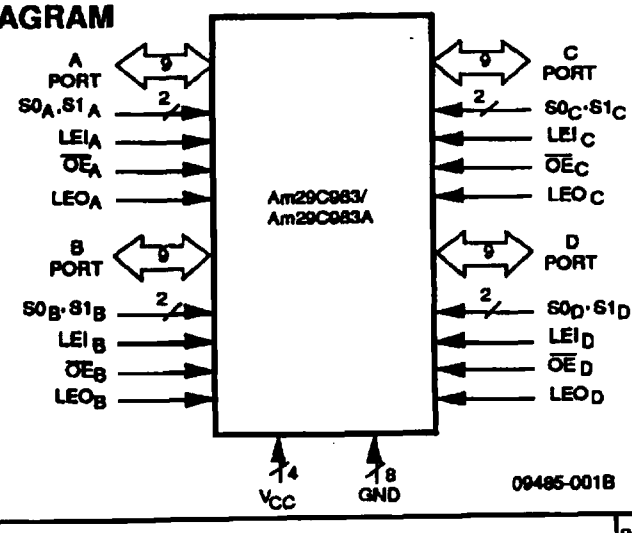
GENERAL DESCRIPTION

The Am29C983/A is a high-speed Multiple Bus Exchange device. It is organized as four 9-bit wide TTL-compatible I/O ports with Output Enable control for each port. Any port can serve either as a source (Input) port or as a destination (Output) port. When the output drivers of a port are disabled (high-impedance state), the port serves as a source port. When the drivers are enabled, the port serves as a destination port. Source port selection is made by two independent Select inputs at each port. This organization offers flexibility in implementing the Am29C983/A as a digital cross-point switch for multiple bus communication in a multiprocessing environment.

Each I/O port has an input latch to capture incoming data and an output latch to capture outgoing data. All input and output latches are independently controlled by active-HIGH Latch Enable inputs. This feature can be used to perform stored operation for byte-word compression and expansion to communicate between buses of different widths.

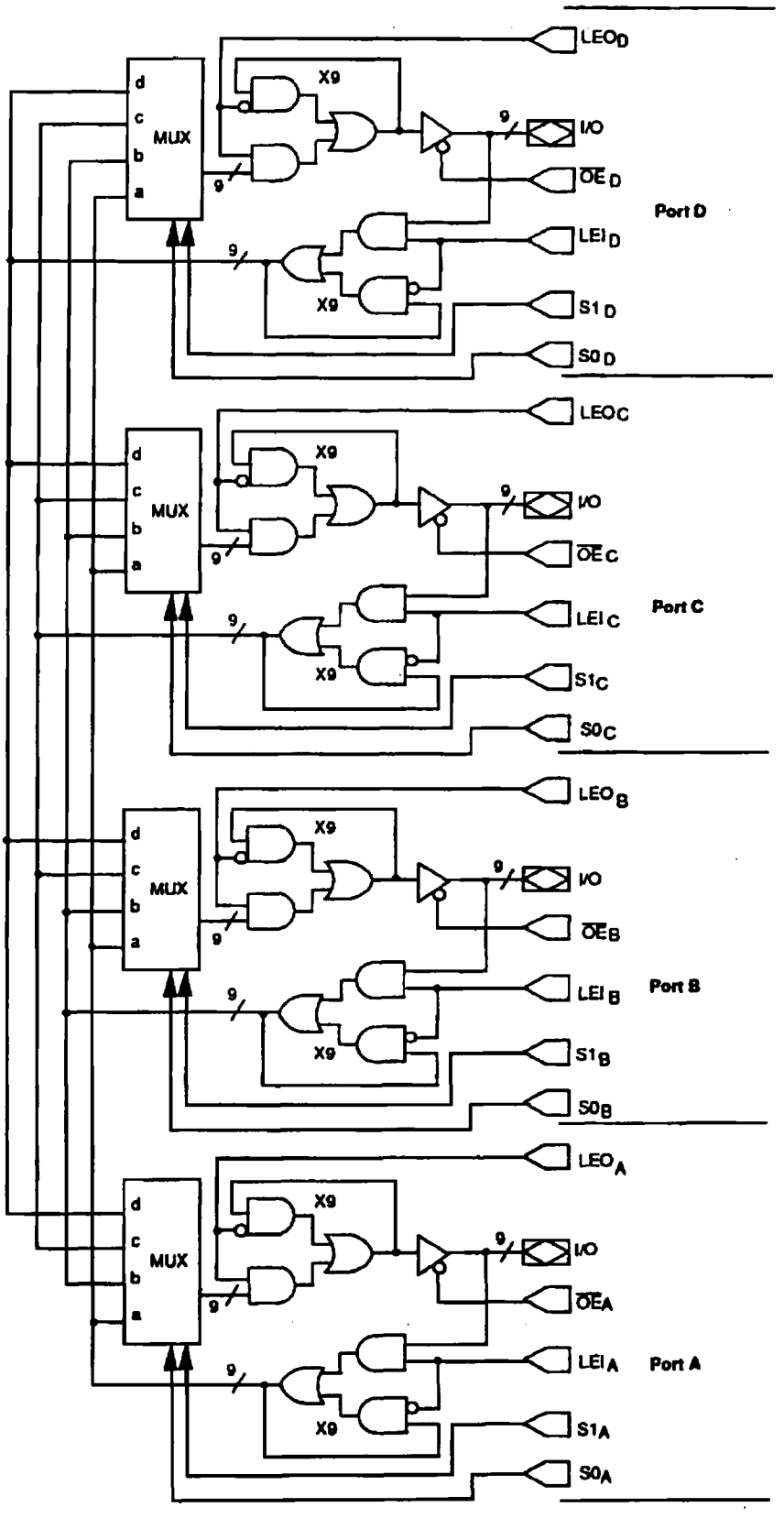
Independent port control permits cascading of Am29C983/As for wider buses. All I/O ports go into high-impedance state upon power-down. This feature makes the device ideally suited for card-edge applications.

SIMPLIFIED BLOCK DIAGRAM



Publication# 09485 Rev. F Amendment /0
Issue Date: June 1992

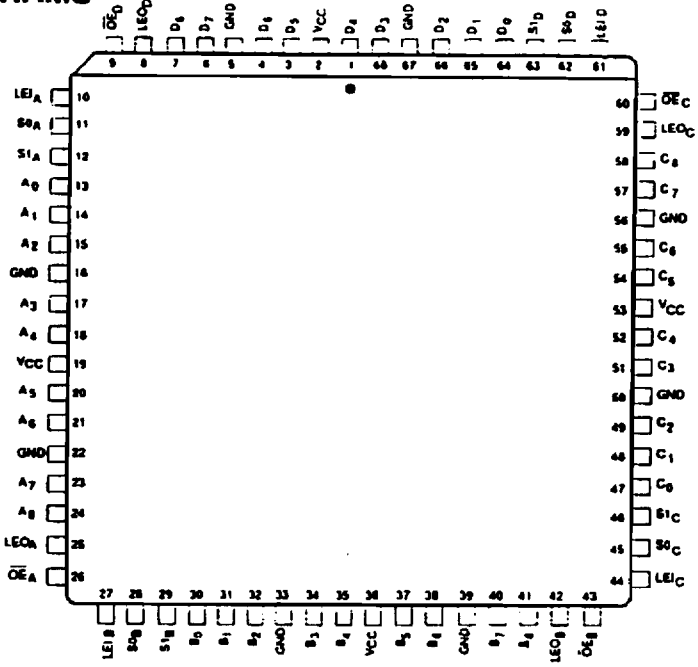
DETAILED BLOCK DIAGRAM



09485E-002C

CONNECTION DIAGRAMS

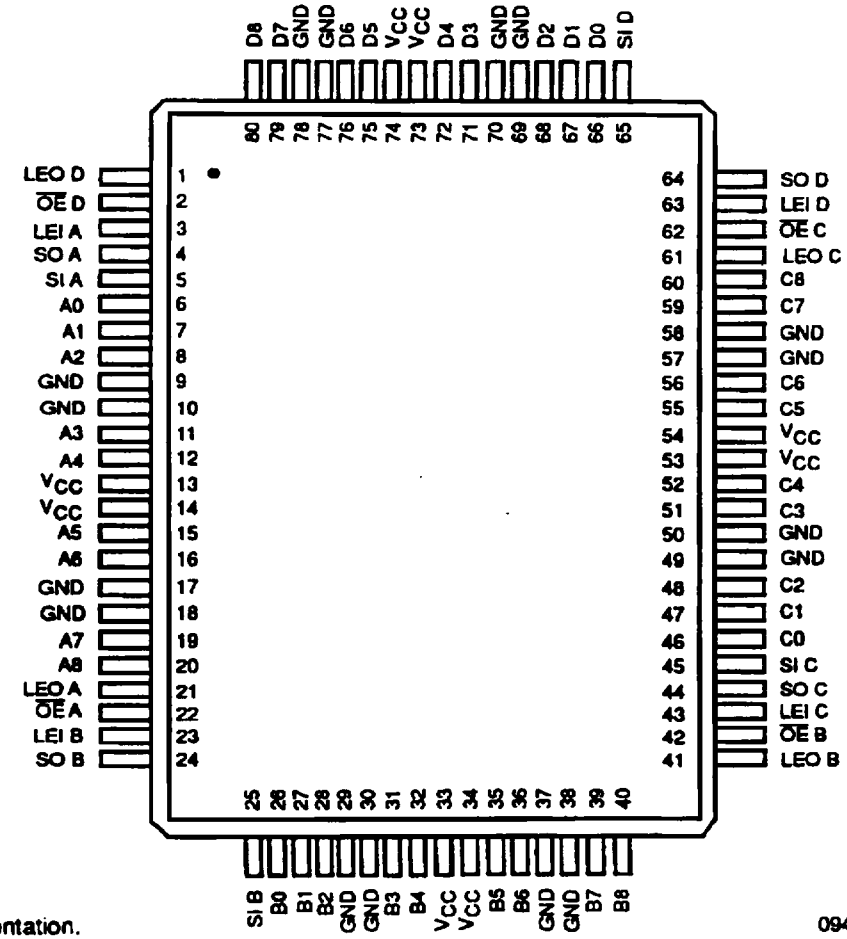
PLCC
(Top View)



Note:
Pin 1 is marked for orientation.

09485-003A

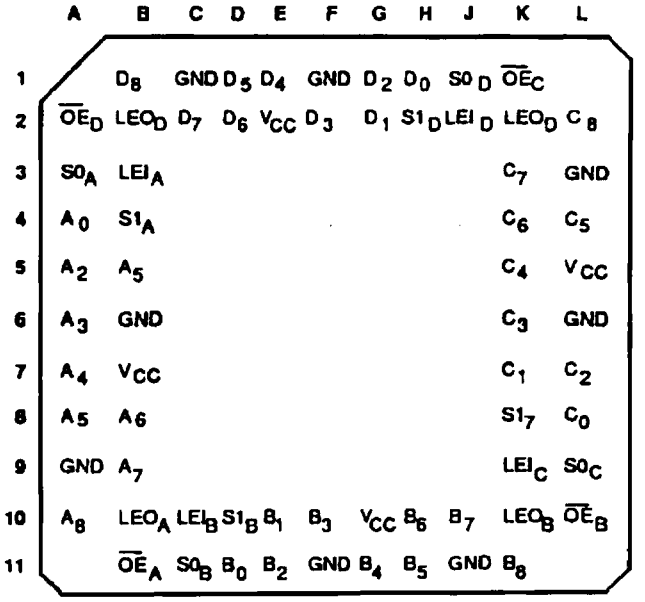
PQFP
(Top View)



Note:
Pin 1 is marked for orientation.

09485-014A

PGA
(Bottom View)



Note:
Notch indicates orientation.

09485-013A

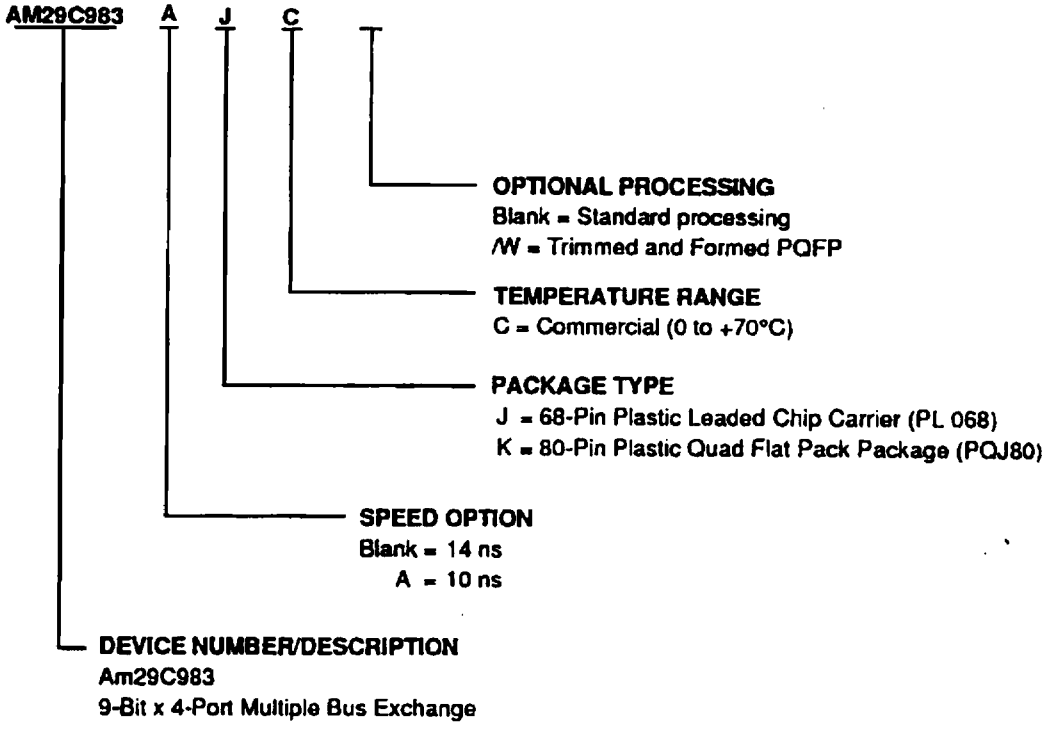
PIN DESIGNATIONS
(Sorted by Pin Number)

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
A-2	$\overline{OE}_D$	B-9	A_7	F-10	B_3	K-4	C_6
A-3	$S0_A$	B-10	LEO_A	F-11	GND	K-5	C_4
A-4	A_0	B-11	$\overline{OE}_A$	G-1	D_2	K-6	C_3
A-5	A_2	C-1	GND	G-2	D_1	K-7	C_1
A-6	A_3	C-2	D_7	G-10	V_{CC}	K-8	$S1_C$
A-7	A_4	C-10	LEI_B	G-11	B_4	K-9	LEI_C
A-8	A_5	C-11	$S0_B$	H-1	D_0	K-10	LEO_B
A-9	GND	D-1	D_3	H-2	$S1_D$	K-11	B_8
A-10	A_6	D-2	D_5	H-10	B_6	L-2	C_8
B-1	D_8	D-10	$S1_B$	H-11	B_5	L-3	GND
B-2	LEO_D	D-11	B_0	J-1	$S0_D$	L-4	C_5
B-3	LEI_A	E-1	D_4	J-2	LEI_D	L-5	V_{CC}
B-4	$S1_A$	E-2	V_{CC}	J-10	B_7	L-6	GND
B-5	A_1	E-10	B_1	J-11	GND	L-7	C_7
B-6	GND	E-11	B_2	K-1	$\overline{OE}_C$	L-8	C_0
B-7	V_{CC}	F-1	GND	K-2	LEO_C	L-9	$S0_C$
B-8	A_8	F-2	D_6	K-3	C_7	L-10	$\overline{OE}_B$

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM29C983	JC
AM29C983A	JC, KC/W

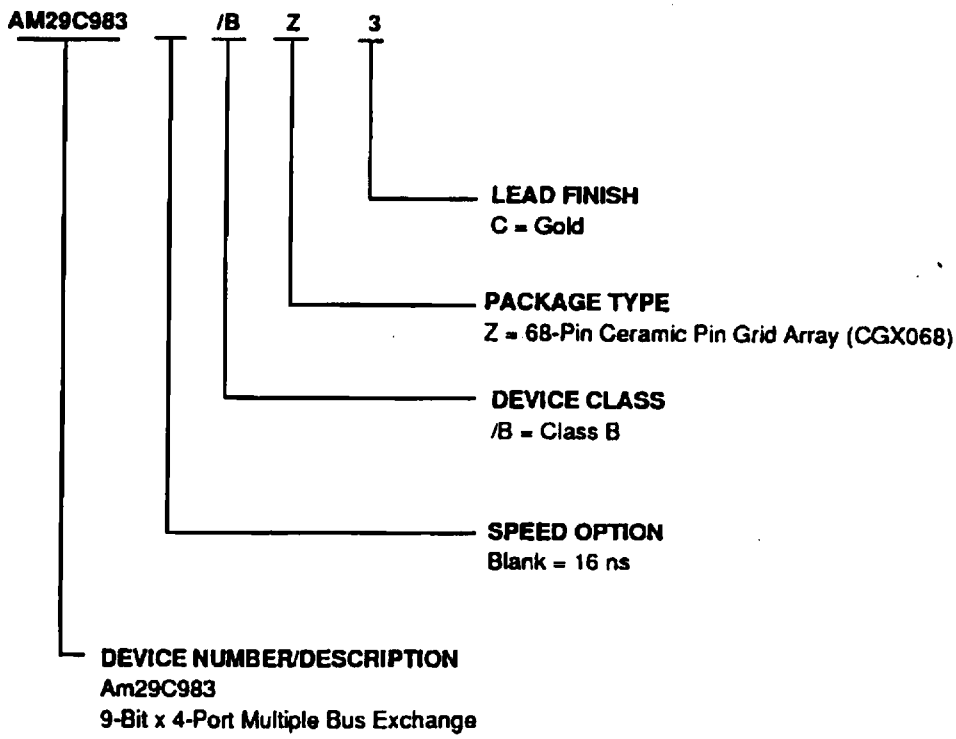
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approve Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM29C983	/BZC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Group A Tests

Group A tests consists of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

A_I, B_I, C_I, AND D_I (I = 0 through 8)
DATA BUS I/O PORTS (INPUT/OUTPUT)

These four groups of nine I/O pins are defined as the A, B, C, and D ports respectively. Each port serves as a source (Input) or as a destination (Output).

SI_A, SI_B, SI_C, and SI_D (I = 0, 1)
SOURCE PORT SELECT (INPUTS)

Each pair of inputs determines the source of data for the corresponding I/O port when used as a destination port.

LEI_A, LEI_B, LEI_C, and LEI_D
INPUT LATCH ENABLE (INPUTS; ACTIVE HIGH)

Each LEI input controls a 9-bit wide latch on the input side of the corresponding I/O port. The latches are transparent when LEI is HIGH and are latched when LEI is LOW.

LEO_A, LEO_B, LEO_C, and LEO_D
OUTPUT LATCH ENABLE (INPUTS; ACTIVE HIGH)

Each LEO input controls a 9-bit wide latch on the output side of the corresponding I/O port. The latches are transparent when LEO is HIGH and are latched when LEO is LOW.

$\overline{OE}_A$, $\overline{OE}_B$, $\overline{OE}_C$, and $\overline{OE}_D$
OUTPUT ENABLE (INPUTS; ACTIVE LOW)

Each $\overline{OE}$ input controls the bus drivers of the corresponding I/O port. When $\overline{OE}$ is LOW, data at the output of the Output latches is passed to the bus. When $\overline{OE}$ is HIGH, the bus outputs are in high-impedance state.

FUNCTIONAL DESCRIPTION

The Am29C983/A Multiple Bus Exchange consists of four 9-bit I/O ports. Each port has a 9-bit Input latch to capture incoming data and a 9-bit Output latch to capture outgoing data. There are five control inputs associated with each port: two Select inputs for source port selection, two Latch Enable inputs (active HIGH) to control Input and Output latches, and an active LOW Output Enable line to control the bus driver at the I/O port.

Port Selection and Control

Each port is independently controlled by means of these five control inputs. If the output drivers of a port are disabled (high-impedance state), that port is an input and can be used as a source port. Incoming data can be captured in the Input latch. At the same time, the data at one of the four internal buses can be transferred to the Output latch under the control of the appropriate Select inputs. If the output drivers are enabled, the port serves as a destination port, transporting the data at the output of its Output latch to the external bus connected to the I/O port. Independent control of Input and Output latches and output drivers permits stored operation at any port.

Multiple Bus Communication

Four internal buses serve as pathways for port-to-port connection. By proper choice of source select codes for the ports, the Am29C983/A can be configured in different modes for multiple bus communication. In one mode of operation, two ports can be selected as source ports and the other two as destination ports; thus, two independent bidirectional communication channels are established. In another mode, one port can be selected as the source, and one or more of the other ports can serve as destination ports. Any port not intended as a destination port can be disabled (high-impedance state) by means of its Output Enable control.

Input and Output Latches

The presence of Input and Output latches offers significant flexibility in using the Am29C983/A. Any port can be chosen as the source port to store incoming data in its Input latch. This can then be connected to one or more destination ports. The outgoing data can be further stored in the Output latches for later use; thus there are two stages of data storage between any two ports. This feature can be used in simple store and forward applications, as well as in more sophisticated applications for byte-word compression and expansion. Moreover, the data stored in the Input latch of a port can be "read back" to the same port by choosing it as the destination (its Output latch is transparent). This feature can be used for diagnostics in multiple bus communication.

TRUTH TABLES

A. Port Source Selection

$S1_n$	$S0_n$	Source
L	L	A Bus
L	H	B Bus
H	L	C Bus
H	H	D Bus

B. Latch Operation

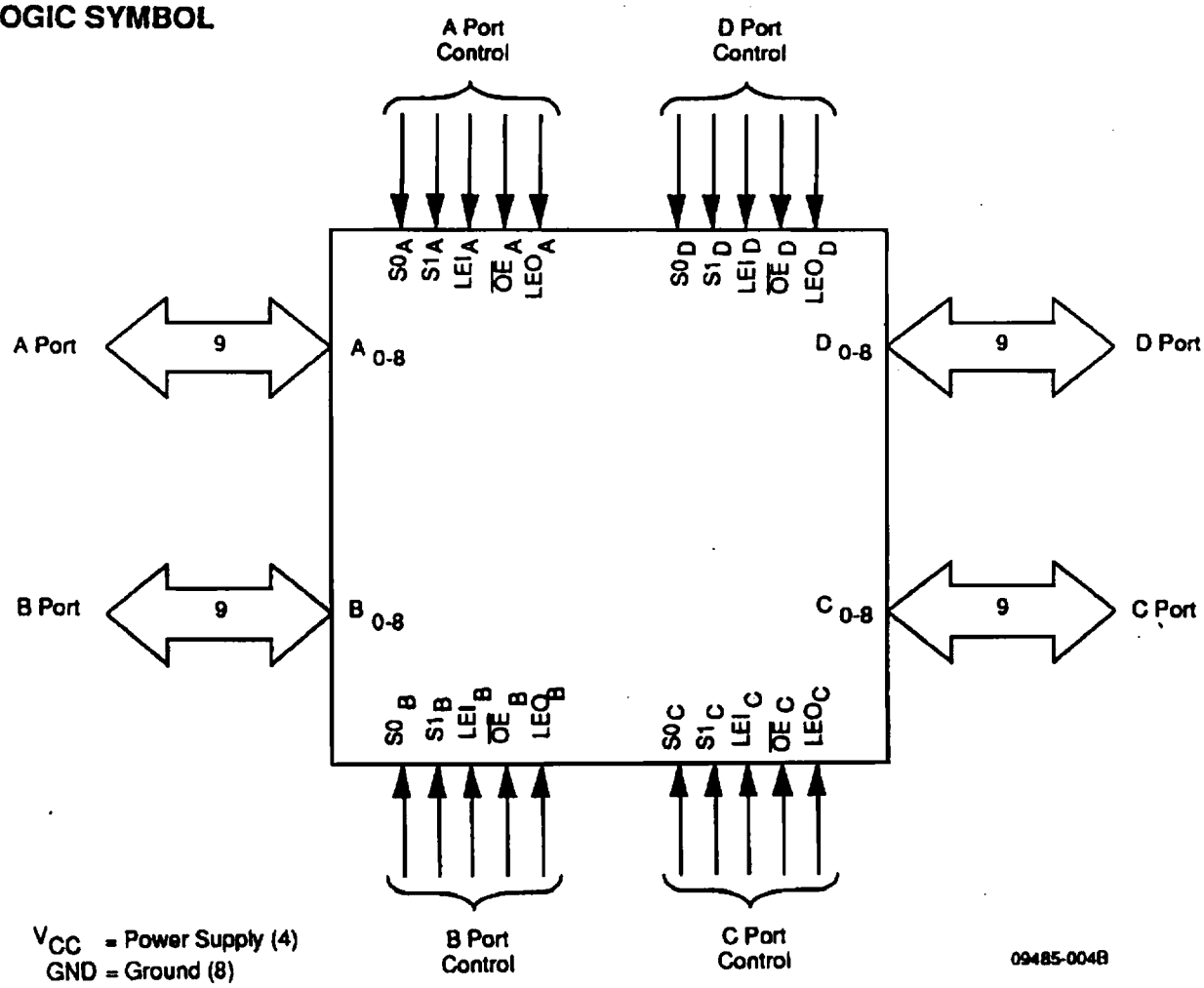
LEI_n or LEO_n	Mode
H	Transparent
L	Latched

C. I/O Port Controls

LEO_n	$\overline{OE}_n$	I/O	Source of Data
L	L	Out	Contents of Output Latch
H	L	Out	Selected Source Port
X	H	In	

Key: n = A, B, C, or D
L = LOW
H = HIGH
X = Don't Care

LOGIC SYMBOL



V_{CC} = Power Supply (4)
GND = Ground (8)

09485-004B

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	–0.5 to 7.0 V
DC Input Diode Current	
(I_{IK}) (V_{IN} < 0 V)	–20 mA
(V_{IN} > V_{CC} if applicable)	+20 mA
DC Input Voltage (V_{IN})	–0.5 to V_{CC} +0.5 V
DC Output Diode Current	
(I_{OK}) (V_{OUT} < 0 V)	–50 mA
(V_{OUT} > V_{CC} if applicable)	+50 mA
DC Output Current per Output Pin:	
I_{SINK}	+70 mA
I_{SOURCE}	–30 mA
DC Output Voltage (V_{OUT})	–0.5 to 7.0 V
Total DC Ground Current (I_{GND})	1750 mA
Total DC V_{CC} Current (I_{CC})	575 mA
Storage Temperature	–65 to +150°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V
Military (M) Devices	
Ambient Temperature (T_A)	-55 to +125°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

(For APL products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

AM29C983

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IL} or V_{IH}	I_{OH} = –15 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IL} or V_{IH}	I_{OL} = 48 mA		0.5	V
V_{IH}	Input HIGH Voltage	(Note 1)		2.0		V
V_{IL}	Input LOW Voltage	(Note 1)			0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = –18 mA			–1.2	V
I_{IL}	Input LOW Current (Select Inputs)	V_{CC} = 5.5 V, V_{IN} = 0 V			–10	µA
I_{IH}	Input HIGH Current (Select Inputs)	V_{CC} = 5.5 V, V_{IN} = 5.5 V			10	µA
I_{OZL}	Off-State Leakage Current (I/O Ports)	V_{CC} = 5.5 V, V_{OUT} = 0 V			–20	µA
I_{OZH}	Off-State Leakage Current (I/O Ports)	V_{CC} = 5.5 V, V_{OUT} = 5.5 V			20	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_{OUT} = 0 V (Note 2)		–60		mA
I_{CCO}	Quiescent Power Supply Current (Note 4)	V_{CC} = 5.5 V, V_{IN} = 5.5 V or GND Outputs Open			1.5	mA

DC CHARACTERISTICS (Continued)

Parameter Symbol	Parameter Description Test Conditions		Min.	Max.	Unit
I_{CCT}	Power Supply Current TTL Input HIGH (Note 4)	V_{CC} = 5.5 V, V_{IN} = 2.4 V Other Inputs at V_{CC} or GND		3.0	mA/ Input
I_{CCD}	Dynamic Power Supply Current (Note 4)	V_{CC} = 5.5 V, Outputs Open One Output Toggling (Note 3)		500	µA/ MHz/Bit

AM29C983A

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V V_{IN} = V_{IL} or V_{IH}	I_{OH} = −15 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V V_{IN} = V_{IL} or V_{IH}	I_{OL} = 48 mA		0.5	V
V_{IH}	Input HIGH Voltage	(Note 1)		2.0		V
V_{IL}	Input LOW Voltage	(Note 1)			0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA			−1.2	V
I_{IL}	Input LOW Current (Select Inputs)	V_{CC} = 5.5 V, V_{IN} = 0 V			−10	µA
I_{IH}	Input HIGH Current (Select Inputs)	V_{CC} = 5.5 V, V_{IN} = 5.5 V			10	µA
I_{OZL}	Off-State Leakage Current (I/O Ports)	V_{CC} = 5.5 V, V_{OUT} = 0 V			−20	µA
I_{OZH}	Off-State Leakage Current (I/O Ports)	V_{CC} = 5.5 V, V_{OUT} = 5.5 V			20	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_{OUT} = 0 V (Note 2)		−60		mA
I_{CCO}	Quiescent Power Supply Current (Note 4)	V_{CC} = 5.5 V, V_{IN} = 5.5 V or GND Outputs Open			1.5	mA
I_{CCT}	Power Supply Current TTL Input HIGH (Note 4)	V_{CC} = 5.5 V, V_{IN} = 2.4 V Other Inputs at V_{CC} or GND			3.0	mA/ Input
I_{CCD}	Dynamic Power Supply Current (Note 4)	V_{CC} = 5.5 V, Outputs Open One Output Toggling (Note 3)			500	µA/ MHz/Bit

Notes:

1. Input thresholds are tested in combination with other DC parameters or by correlation.
2. Not more than one output shorted at a time. Duration of short-circuit test not to exceed 100 milliseconds.
3. Measured at a frequency of < 10 MHz with 50% duty cycle. Unused inputs are at V_{CC} or GND.
4. Calculation of total device I_{CC}: $I_{CC} = I_{CCO} + I_{CCT} \times M_T \times D_H + I_{CCD} \times ((C_L + 91) \div 91) \times f \times N$

   Where C_L = Load Capacitance in pF per output
   f = Frequency in MHz
   N = Average number of outputs switching
   M_T = Number of inputs at logic HIGH
   D_H = Duty cycle for each input HIGH

SWITCHING CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Am29C983						
No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
1	t_{PLH}	Propagation Delay Port to Port	C_L = 50 pF R_1 = 500 Ohms R_2 = 500 Ohms	1.5	14	ns
2	t_{PHL}	LEI = HIGH, LEO = HIGH		1.5	14	ns
3	t_{PLH}	Propagation Delay Select Input to Port LEO = HIGH		1.5	18	ns
4	t_{PHL}			1.5	18	ns
5	t_{PLH}	Propagation Delay LEI to Port		1.5	18	ns
6	t_{PHL}	LEO = HIGH		1.5	18	ns
7	t_{PLH}	Propagation Delay		1.5	14	ns
8	t_{PHL}	LEO to Port		1.5	14	ns
9	t_{PZH}	Output Enable Time		1	14	ns
10	t_{PZL}	$\overline{OE}$ to Port		1	14	ns
11	t_{PHZ}	Output Disable Time		0	12	ns
12	t_{PLZ}	$\overline{OE}$ to Port		0	12	ns
13	t_s	Port to LEI Setup		2		ns
14	t_h	Port to LEI Hold		3		ns
15	t_s	Port to LEO Setup		4.5		ns
16	t_h	Port to LEO Hold		1.5		ns
17	t_s	Select to LEO Setup		6		ns
18	t_h	Select to LEO Hold		0		ns
19	t_s	LEI to LEO Setup		6		ns
20	t_h	LEI to LEO Hold		0		ns
21	t_{PWH}	LEI, LEO Pulse Width HIGH		6		ns

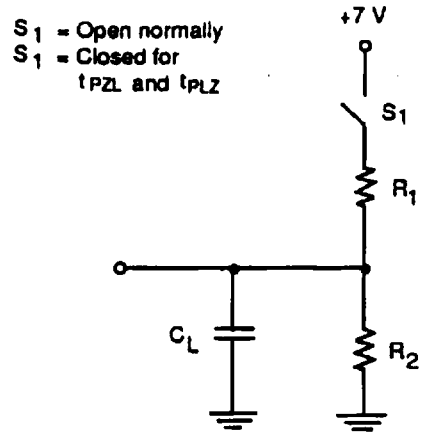
SWITCHING CHARACTERISTICS over MILITARY operating range unless otherwise specified (for APL products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Am29C983				Military		
No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
1	t_{PLH}	Propagation Delay Port to Port	C_L = 50 pF R_1 = 500 Ohms R_2 = 500 Ohms	1.0	16	ns
2	t_{PHL}	LEI = HIGH, LEO = HIGH		1.0	16	ns
3	t_{PLH}	Propagation Delay Select Input to Port LEO = HIGH		1.0	20	ns
4	t_{PHL}			1.0	20	ns
5	t_{PLH}	Propagation Delay LEI to Port		1.0	20	ns
6	t_{PHL}	LEO = HIGH		1.0	20	ns
7	t_{PLH}	Propagation Delay LEO to Port		1.0	16	ns
8	t_{PHL}			1.0	16	ns
9	t_{PZH}	Output Enable Time $\overline{OE}$ to Port		1.5	16	ns
10	t_{PZL}			1.0	16	ns
11	t_{PHZ}	Output Disable Time $\overline{OE}$ to Port		0	14	ns
12	t_{PLZ}			0	14	ns
13	t_s	Port to LEI Setup		3		ns
14	t_h	Port to LEI Hold		4		ns
15	t_s	Port to LEO Setup		5.5		ns
16	t_h	Port to LEO Hold		2.5		ns
17	t_s	Select to LEO Setup		7		ns
18	t_h	Select to LEO Hold		1		ns
19	t_s	LEI to LEO Setup		7		ns
20	t_h	LEI to LEO Hold		1		ns
21	t_{PWH}	LEI, LEO Pulse Width HIGH		7		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

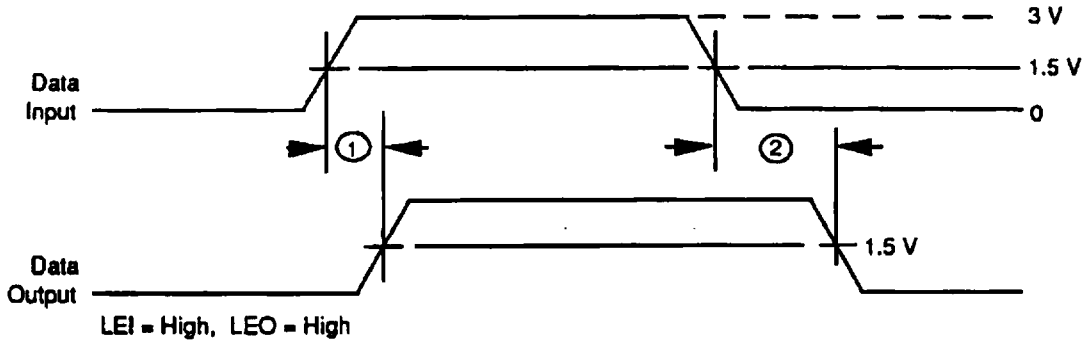
Am29C983A						
No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
1	t_{PLH}	Propagation Delay Port to Port	C_L = 50 pF R_1 = 500 Ohms R_2 = 500 Ohms	1.5	10	ns
2	t_{PHL}	LEI = HIGH, LEO = HIGH		1.5	10	ns
3	t_{PLH}	Propagation Delay Select Input to Port LEO = HIGH		1.5	11	ns
4	t_{PHL}			1.5	11	ns
5	t_{PLH}	Propagation Delay LEI to Port		1.5	12	ns
6	t_{PHL}	LEO = HIGH		1.5	12	ns
7	t_{PLH}	Propagation Delay LEO to Port		1.5	10	ns
8	t_{PHL}			1.5	10	ns
9	t_{PZH}	Output Enable Time $\overline{OE}$ to Port		1	10	ns
10	t_{PZL}			1	10	ns
11	t_{PHZ}	Output Disable Time $\overline{OE}$ to Port		0	9	ns
12	t_{PLZ}			0	9	ns
13	t_s	Port to LEI Setup		2		ns
14	t_h	Port to LEI Hold		3		ns
15	t_s	Port to LEO Setup		4.5		ns
16	t_h	Port to LEO Hold		1.5		ns
17	t_s	Select to LEO Setup		6		ns
18	t_h	Select to LEO Hold		0		ns
19	t_s	LEI to LEO Setup		6		ns
20	t_h	LEI to LEO Hold		0		ns
21	t_{PWH}	LEI, LEO Pulse Width HIGH		6		ns

SWITCHING TEST CIRCUIT



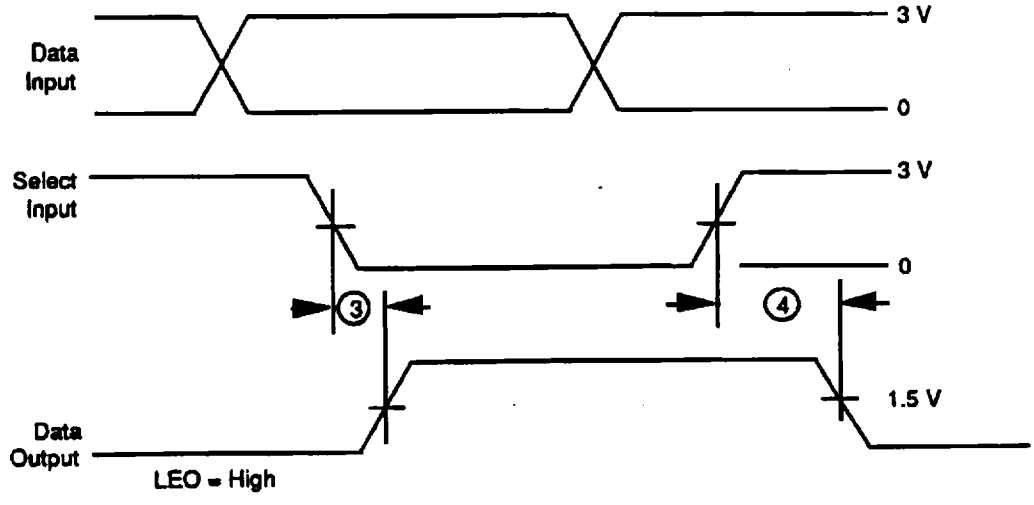
09485-007B

SWITCHING TEST WAVEFORMS



09485-008C

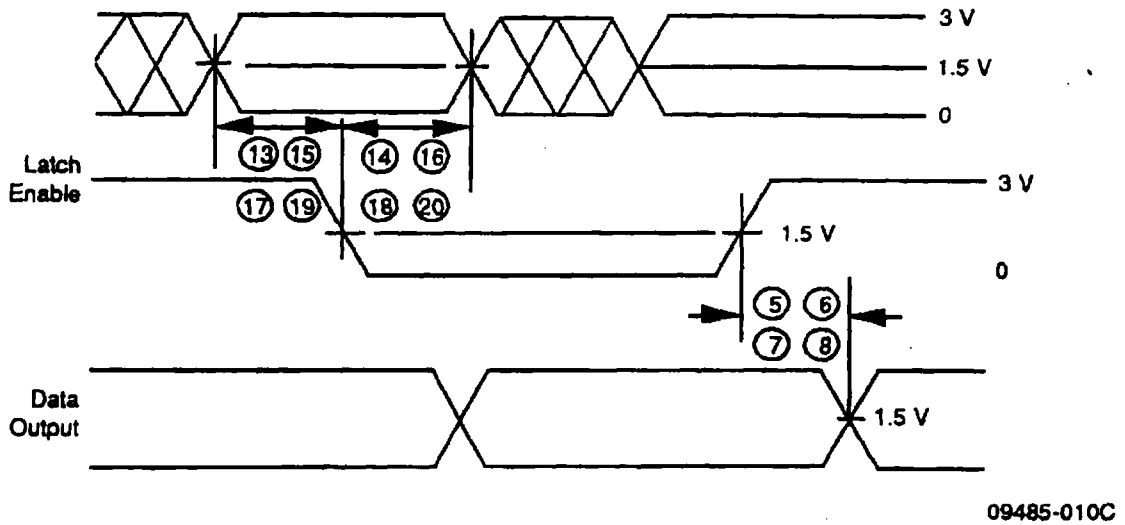
Propagation Delay — Port-to-Port



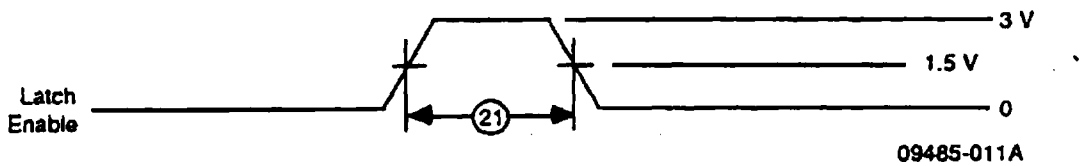
09485-009B

Propagation Delay — Select-to-Port

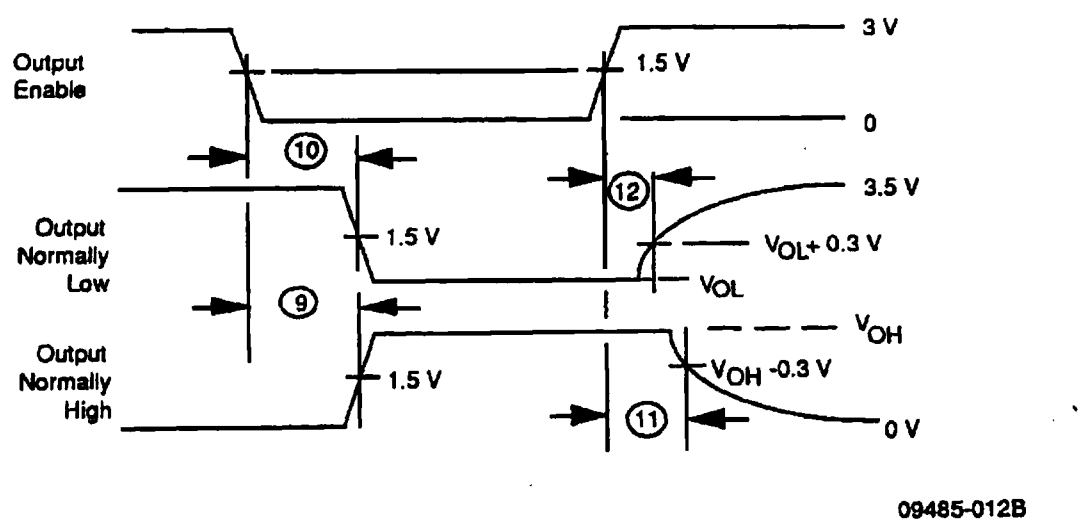
SWITCHING TEST WAVEFORMS (Continued)



Input and Output Latch Propagation Delay, Setup and Hold Times



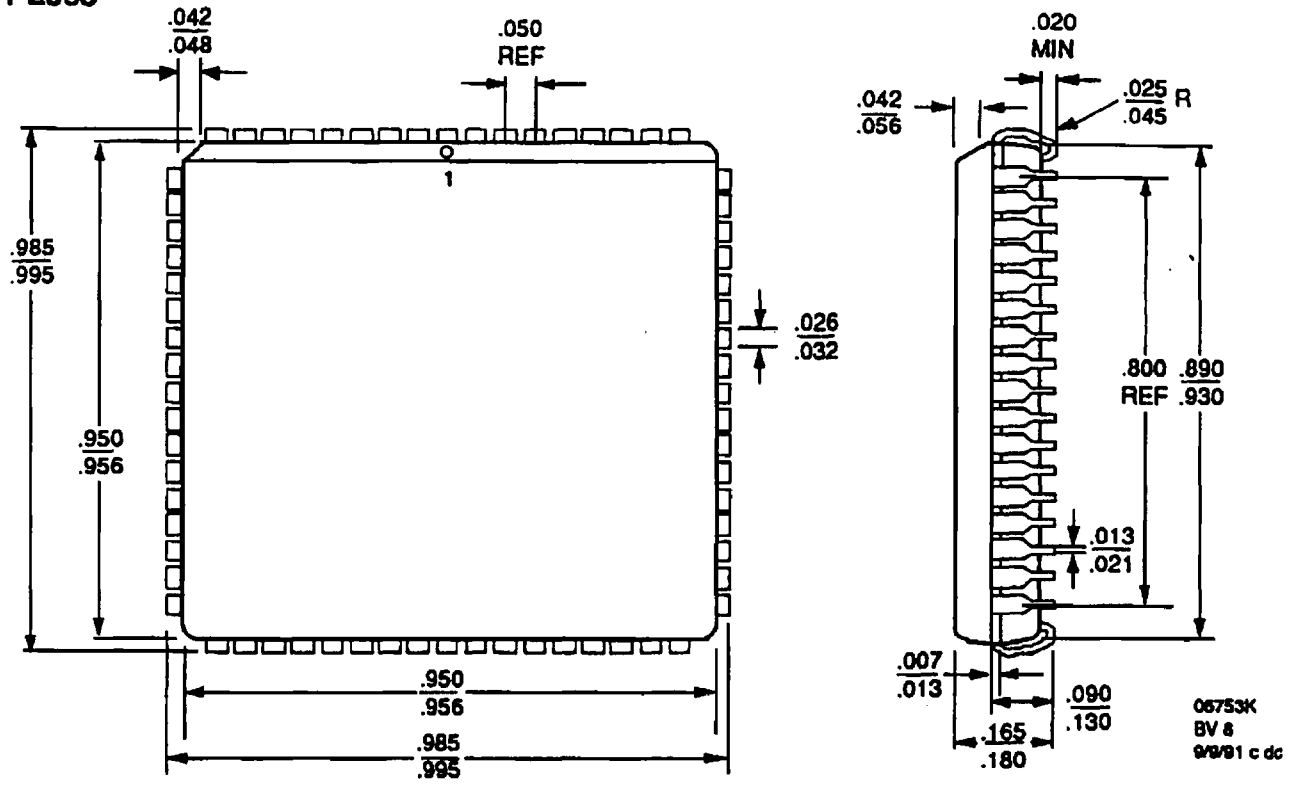
Minimum Latch Enable Pulse Width



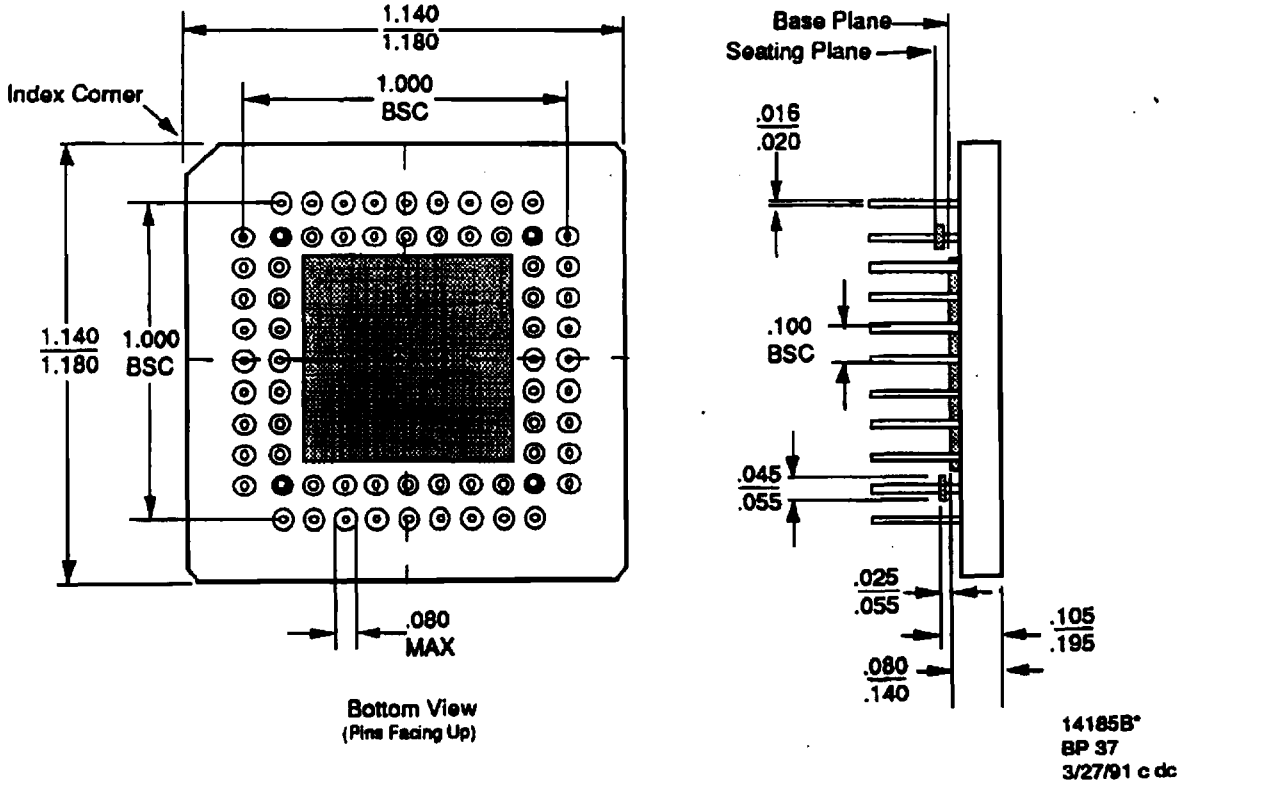
Enable and Disable Times

PHYSICAL DIMENSIONS*

PL068

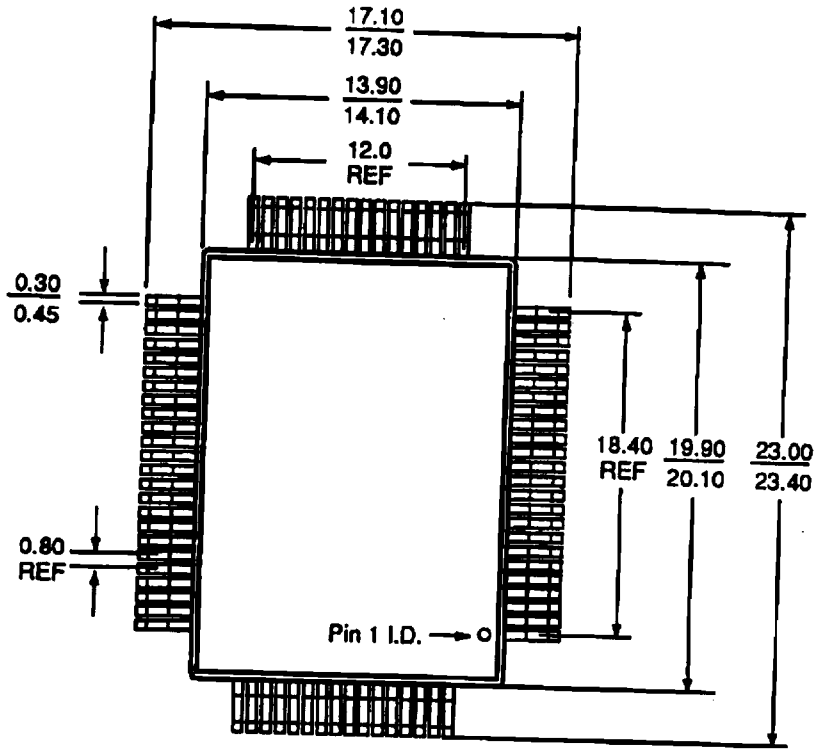


CGX068

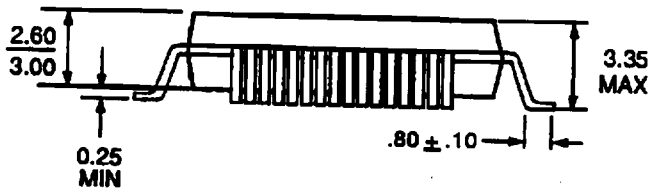


*For reference only. All dimensions are measured in inches unless otherwise specified. BSC is an ANSI standard for Basic Space Centering.

PHYSICAL DIMENSIONS*
PQJ80



TOP VIEW



SIDE VIEW

14635C
BX 44
5/7/92 SG