

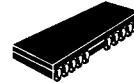
*Advance Information*  
**4M x 1 CMOS Dynamic RAM**  
**Nibble Mode**

The MCM54101A is a 0.7μ CMOS high-speed dynamic random access memory. It is organized as 4,194,304 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost. The fast nibble mode feature allows high-speed serial access of up to 4 bits of data.

The MCM54101A requires only 11 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300 mil small outline package, a 300 mil thin-small-outline package (TSOP), and a 100 mil zig-zag in-line package (ZIP).

- Three-State Data Output
- Nibble Mode
- Test Mode
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$ -Only Refresh
- $\overline{CAS}$  Before  $\overline{RAS}$  Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM54101A = 16 ms
- Fast Access Time ( $t_{RAC}$ ):
  - MCM54101A-60 = 60 ns (Max)
  - MCM54101A-70 = 70 ns (Max)
  - MCM54101A-80 = 80 ns (Max)
- Low Active Power:
  - MCM54101A-60 = 660 mW (Max)
  - MCM54101A-70 = 550 mW (Max)
  - MCM54101A-80 = 468 mW (Max)
- Low Standby Power Dissipation:
  - MCM54101A = 11 mW (Max, TTL Levels)
  - = 5.5 mW (Max, CMOS Levels)

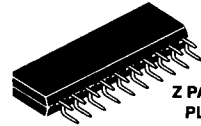
**MCM54101A**



**N PACKAGE**  
**300 MIL SOJ**  
**CASE 822-03**



**T PACKAGE**  
**300 MIL TSOP**  
**CASE 892-01**



**Z PACKAGE**  
**PLASTIC**  
**ZIG-ZAG IN-LINE**  
**CASE 836-02**

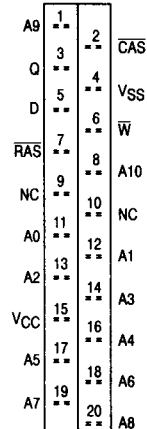
**3**

**PIN NAMES**

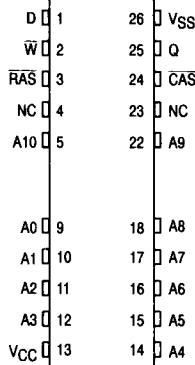
A0 - A10	.....	Address Input
D	.....	Data Input
Q	.....	Data Output
W	.....	Read/Write Input
$\overline{RAS}$	.....	Row Address Strobe
$\overline{CAS}$	.....	Column Address Strobe
VCC	.....	Power Supply (+ 5 V)
VSS	.....	Ground
NC	.....	No Connection

**PIN ASSIGNMENTS**

**100 MIL ZIP**

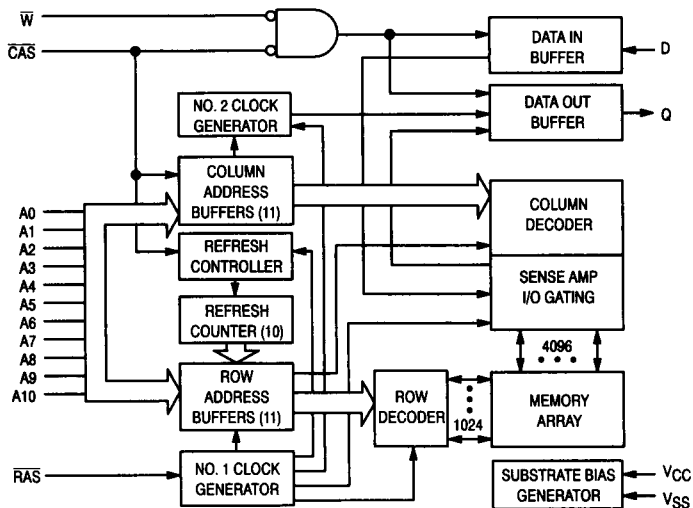


**300 MIL SOJ/TSOP**



This document contains information on a new product. Specifications and information herein are subject to change without notice.

**BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS** (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V <sub>CC</sub>	- 1 to + 7	V
Voltage Relative to V <sub>SS</sub> for Any Pin Except V <sub>CC</sub>	V <sub>in</sub> , V <sub>out</sub>	- 1 to + 7	V
Data Out Current	I <sub>out</sub>	50	mA
Power Dissipation	P <sub>D</sub>	700	mW
Operating Temperature Range	T <sub>A</sub>	0 to + 70	°C
Storage Temperature Range	T <sub>stg</sub>	- 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $T_A = 0 \text{ to } +70^\circ\text{C}$ , Unless Otherwise Noted)

### RECOMMENDED OPERATING CONDITIONS (All voltages referenced to $V_{SS}$ )

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	
Logic High Voltage, All Inputs	$V_{IH}$	2.4	—	6.5	V
Logic Low Voltage, All Inputs	$V_{IL}$	-1.0	—	0.8	V

### DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
$V_{CC}$ Power Supply Current MCM54101A-60, $t_{RC} = 110 \text{ ns}$ MCM54101A-70, $t_{RC} = 130 \text{ ns}$ MCM54101A-80, $t_{RC} = 150 \text{ ns}$	$I_{CC1}$	—	120 100 85	mA	1, 2
$V_{CC}$ Power Supply Current (Standby) ( $\overline{RAS} = \overline{CAS} = V_{IH}$ )	$I_{CC2}$	—	2.0	mA	
$V_{CC}$ Power Supply Current During $\overline{RAS}$ -Only Refresh Cycles ( $\overline{CAS} = V_{IH}$ ) MCM54101A-60, $t_{RC} = 110 \text{ ns}$ MCM54101A-70, $t_{RC} = 130 \text{ ns}$ MCM54101A-80, $t_{RC} = 150 \text{ ns}$	$I_{CC3}$	—	120 100 85	mA	1, 2
$V_{CC}$ Power Supply Current During Fast Page Mode Cycle ( $\overline{RAS} = V_{IL}$ ) MCM54101A-60, $t_{NC} = 40 \text{ ns}$ MCM54101A-70, $t_{NC} = 40 \text{ ns}$ MCM54101A-80, $t_{NC} = 40 \text{ ns}$	$I_{CC4}$	—	50 50 50	mA	1, 2
$V_{CC}$ Power Supply Current (Standby) ( $\overline{RAS} = \overline{CAS} = V_{CC} - 0.2 \text{ V}$ )	$I_{CC5}$	—	1.0	mA	
$V_{CC}$ Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM54101A-60, $t_{RC} = 110 \text{ ns}$ MCM54101A-70, $t_{RC} = 130 \text{ ns}$ MCM54101A-80, $t_{RC} = 150 \text{ ns}$	$I_{CC6}$	—	120 100 85	mA	1
Input Leakage Current ( $0 \text{ V} \leq V_{in} \leq 5.5 \text{ V}$ )	$I_{lkg(I)}$	-10	10	$\mu\text{A}$	
Output Leakage Current ( $\overline{CAS} = V_{IH}$ , $0 \text{ V} \leq V_{out} \leq 5.5 \text{ V}$ )	$I_{lkg(O)}$	-10	10	$\mu\text{A}$	
Output High Voltage ( $I_{OH} = -5 \text{ mA}$ )	$V_{OH}$	2.4	—	V	
Output Low Voltage ( $I_{OL} = 4.2 \text{ mA}$ )	$V_{OL}$	—	0.4	V	

#### NOTES:

- Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
- Column address can be changed once or less while  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$ .

### CAPACITANCE ( $f = 1.0 \text{ MHz}$ , $T_A = 25^\circ\text{C}$ , $V_{CC} = 5 \text{ V}$ , Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	A0 - A10, D	5	$\mu\text{F}$
	$\overline{RAS}$ , $\overline{CAS}$ , W	7	
I/O Capacitance ( $\overline{CAS} = V_{IH}$ to Disable Output)	Q	7	$\mu\text{F}$

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation:  $C = 1 \Delta t / \Delta V$ .

### AC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $T_A = 0$  to  $70^\circ\text{C}$ , Unless Otherwise Noted)

#### READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM54101A-60		MCM54101A-70		MCM54101A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	$t_{RELREL}$	$t_{RC}$	110	—	130	—	150	—	ns	5
Read-Write Cycle Time	$t_{RELREL}$	$t_{RWC}$	135	—	155	—	175	—	ns	5
Nibble Mode Cycle Time	$t_{CEHCEH}$	$t_{NC}$	40	—	40	—	40	—	ns	
Nibble Mode Read-Write Cycle Time	$t_{CELCEL}$	$t_{NRWC}$	65	—	65	—	65	—	ns	
Access Time from $\overline{RAS}$	$t_{RELOV}$	$t_{RAC}$	—	60	—	70	—	80	ns	6, 7
Access Time from $\overline{CAS}$	$t_{CELOV}$	$t_{CAC}$	—	20	—	20	—	20	ns	6, 8
Access Time from Column Address	$t_{AVQV}$	$t_{AA}$	—	30	—	35	—	40	ns	6, 9
Nibble Mode Access Time	$t_{CELOV}$	$t_{NCAC}$	—	20	—	20	—	20	ns	6
$\overline{CAS}$ to Output in Low-Z	$t_{CELOX}$	$t_{CLZ}$	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	$t_{CEHQZ}$	$t_{OFF}$	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	$t_T$	$t_T$	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	$t_{REHREL}$	$t_{RP}$	40	—	50	—	60	—	ns	
$\overline{RAS}$ Pulse Width	$t_{RELREH}$	$t_{RAS}$	60	10 k	70	10 k	80	10 k	ns	
$\overline{RAS}$ Hold Time	$t_{CELREH}$	$t_{RSH}$	20	—	20	—	20	—	ns	
$\overline{CAS}$ Hold Time	$t_{RELCEH}$	$t_{CSH}$	60	—	70	—	80	—	ns	
$\overline{CAS}$ Pulse Width	$t_{CELCEH}$	$t_{CAS}$	20	10 k	20	10 k	20	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	$t_{RELCEL}$	$t_{RCD}$	20	40	20	50	20	60	ns	11
$\overline{RAS}$ to Column Address Delay Time	$t_{RELAV}$	$t_{RAD}$	15	30	15	35	15	40	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	$t_{CEHREL}$	$t_{CRP}$	5	—	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time	$t_{CEHCEL}$	$t_{CP}$	10	—	10	—	10	—	ns	
Row Address Setup Time	$t_{AVREL}$	$t_{ASR}$	0	—	0	—	0	—	ns	
Row Address Hold Time	$t_{RELAX}$	$t_{RAH}$	10	—	10	—	10	—	ns	
Column Address Setup Time	$t_{AVCEL}$	$t_{ASC}$	0	—	0	—	0	—	ns	
Column Address Hold Time	$t_{CELAX}$	$t_{CAH}$	15	—	15	—	15	—	ns	
Column Address to $\overline{RAS}$ Lead Time	$t_{AVREH}$	$t_{RAL}$	30	—	35	—	40	—	ns	
Read Command Setup Time	$t_{WHCEL}$	$t_{RCS}$	0	—	0	—	0	—	ns	

#### NOTES:

(continued)

- $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- An initial pause of 200  $\mu\text{s}$  is required after power-up followed by 8  $\overline{RAS}$  cycles before proper device operation is guaranteed.
- The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
- AC measurements  $t_T = 5.0\text{ ns}$ .
- The specifications for  $t_{RC}$  (min) and  $t_{RWC}$  (min) are used only to indicate cycle time at which proper operation over the full temperature range ( $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ) is assured.
- Measured with a current load equivalent to 2 TTL ( $-200\ \mu\text{A}$ ,  $+4\ \text{mA}$ ) loads and 100 pF with the data output trip points set at  $V_{OH} = 2.0\ \text{V}$  and  $V_{OL} = 0.8\ \text{V}$ .
- Assumes that  $t_{RCD} \leq t_{RCD}(\text{max})$ .
- Assumes that  $t_{RCD} \geq t_{RCD}(\text{max})$ .
- Assumes that  $t_{RAD} \geq t_{RAD}(\text{max})$ .
- $t_{OFF}$  (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- Operation within the  $t_{RCD}(\text{max})$  limit ensures that  $t_{RAC}(\text{max})$  can be met.  $t_{RCD}(\text{max})$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
- Operation within the  $t_{RAD}(\text{max})$  limit ensures that  $t_{RAC}(\text{max})$  can be met.  $t_{RAD}(\text{max})$  is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{AA}$ .

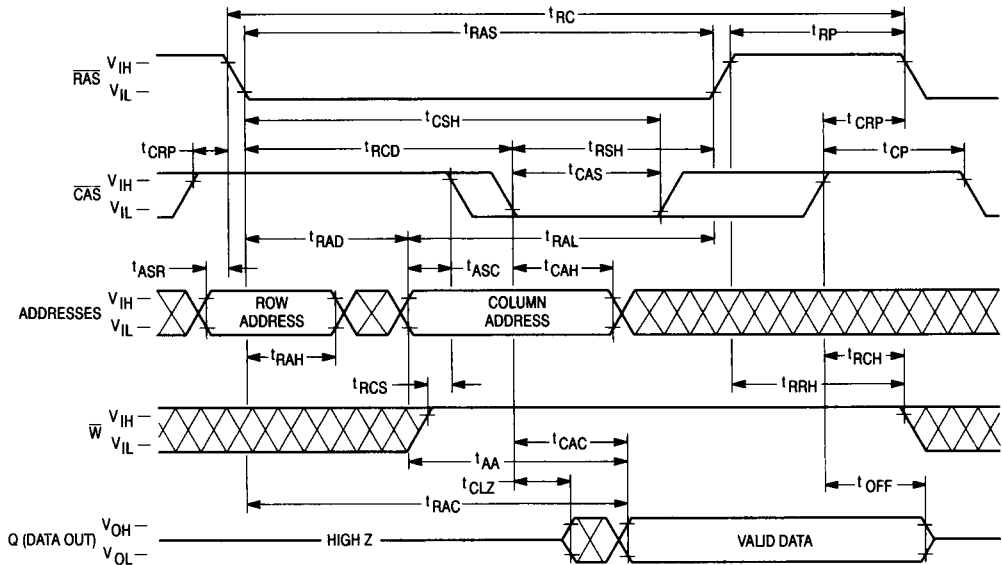
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM54101A-60		MCM54101A-70		MCM54101A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Read Command Hold Time Referenced to CAS	t <sub>CEHWX</sub>	t <sub>RCH</sub>	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to RAS	t <sub>REHWX</sub>	t <sub>RRH</sub>	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to CAS	t <sub>CELWH</sub>	t <sub>WCH</sub>	10	—	15	—	15	—	ns	
Write Command Pulse Width	t <sub>WLWH</sub>	t <sub>WTP</sub>	10	—	15	—	15	—	ns	
Write Command to RAS Lead Time	t <sub>WLREH</sub>	t <sub>RWL</sub>	20	—	20	—	20	—	ns	
Write Command to CAS Lead Time	t <sub>WLCEH</sub>	t <sub>CWL</sub>	20	—	20	—	20	—	ns	
Data in Setup Time	t <sub>DVCEL</sub>	t <sub>DS</sub>	0	—	0	—	0	—	ns	14
Data in Hold Time	t <sub>CELDX</sub>	t <sub>DH</sub>	15	—	15	—	15	—	ns	14
Refresh Period	t <sub>RVRV</sub>	t <sub>RFSH</sub>	—	16	—	16	—	16	ms	
Write Command Setup Time	t <sub>WLCEL</sub>	t <sub>WCS</sub>	0	—	0	—	0	—	ns	15
CAS to Write Delay	t <sub>CELWL</sub>	t <sub>CWD</sub>	20	—	20	—	20	—	ns	15
RAS to Write Delay	t <sub>RELWL</sub>	t <sub>RWD</sub>	60	—	70	—	80	—	ns	15
Column Address to Write Delay Time	t <sub>AWWL</sub>	t <sub>AWD</sub>	30	—	35	—	45	—	ns	15
CAS Setup Time for CAS Before RAS Refresh	t <sub>RELCEL</sub>	t <sub>CSR</sub>	5	—	5	—	5	—	ns	
CAS Hold Time for CAS Before RAS Refresh	t <sub>RELCEH</sub>	t <sub>CHR</sub>	15	—	15	—	15	—	ns	
RAS Precharge to CAS Active Time	t <sub>REHCEL</sub>	t <sub>RPC</sub>	0	—	0	—	0	—	ns	
CAS Precharge Time for CAS Before RAS Counter Test	t <sub>CEHCEL</sub>	t <sub>CPT</sub>	30	—	40	—	40	—	ns	
Nibble Mode Pulse Width	t <sub>CELCEH</sub>	t <sub>NCAS</sub>	20	—	20	—	20	—	ns	
Nibble Mode CAS Precharge Time	t <sub>CEHCEL</sub>	t <sub>NCP</sub>	10	—	10	—	10	—	ns	
Nibble Mode RAS Hold Time	t <sub>CELREH</sub>	t <sub>NRSH</sub>	20	—	20	—	20	—	ns	
Nibble Mode CAS to Write Delay Time	t <sub>CELWL</sub>	t <sub>NCWD</sub>	20	—	20	—	20	—	ns	
Nibble Mode Write Command to RAS Lead Time	t <sub>WLREH</sub>	t <sub>NRWL</sub>	20	—	20	—	20	—	ns	
Nibble Mode Write Command to CAS Lead Time	t <sub>WLCEH</sub>	t <sub>NCWL</sub>	20	—	20	—	20	—	ns	
Write Command Setup Time (Test Mode)	t <sub>WLREL</sub>	t <sub>WTS</sub>	10	—	10	—	10	—	ns	
Write Command Hold Time (Test Mode)	t <sub>RELWH</sub>	t <sub>WTH</sub>	10	—	10	—	10	—	ns	
Write to RAS Precharge Time (CAS Before RAS Refresh)	t <sub>WHREL</sub>	t <sub>WRP</sub>	10	—	10	—	10	—	ns	
Write to RAS Hold Time (CAS Before RAS Refresh)	t <sub>RELWL</sub>	t <sub>WRH</sub>	10	—	10	—	10	—	ns	

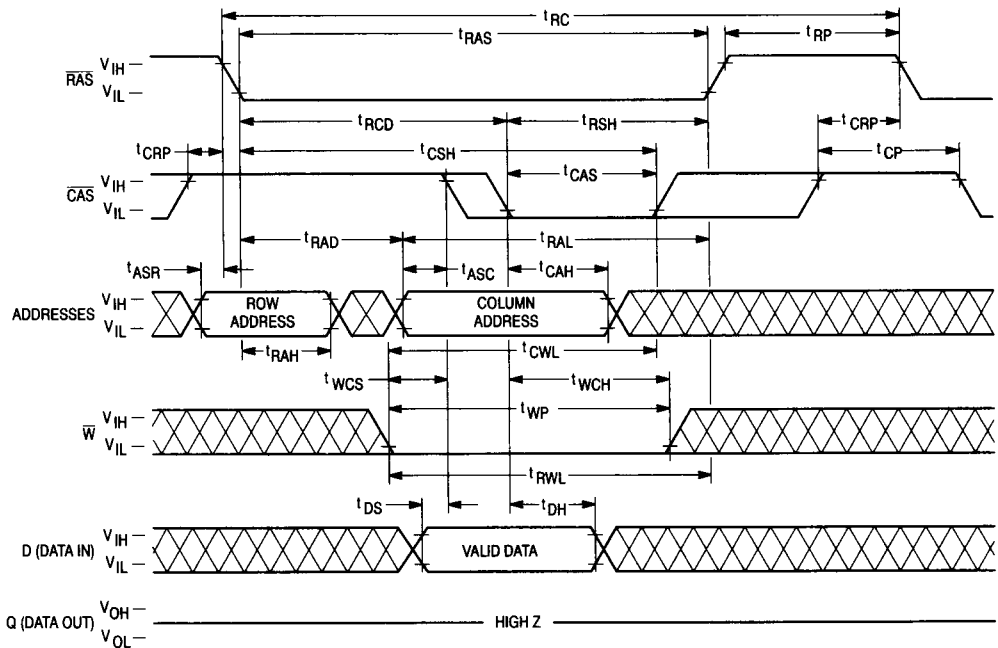
NOTES:

13. Either t<sub>RRH</sub> or t<sub>RCH</sub> must be satisfied for a read cycle.
14. These parameters are referenced to CAS leading edge in early write cycles and to  $\bar{W}$  leading edge in read-write cycles.
15. t<sub>WCS</sub>, t<sub>RWD</sub>, t<sub>CWD</sub>, t<sub>AWD</sub>, and t<sub>CPWD</sub> are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if t<sub>WCS</sub> ≥ t<sub>WCS</sub> (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if t<sub>CWD</sub> ≥ t<sub>CWD</sub> (min), t<sub>RWD</sub> ≥ t<sub>RWD</sub> (min), t<sub>AWD</sub> ≥ t<sub>AWD</sub> (min), and t<sub>CPWD</sub> ≥ t<sub>CPWD</sub> (min) (page mode), the cycle is a read write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

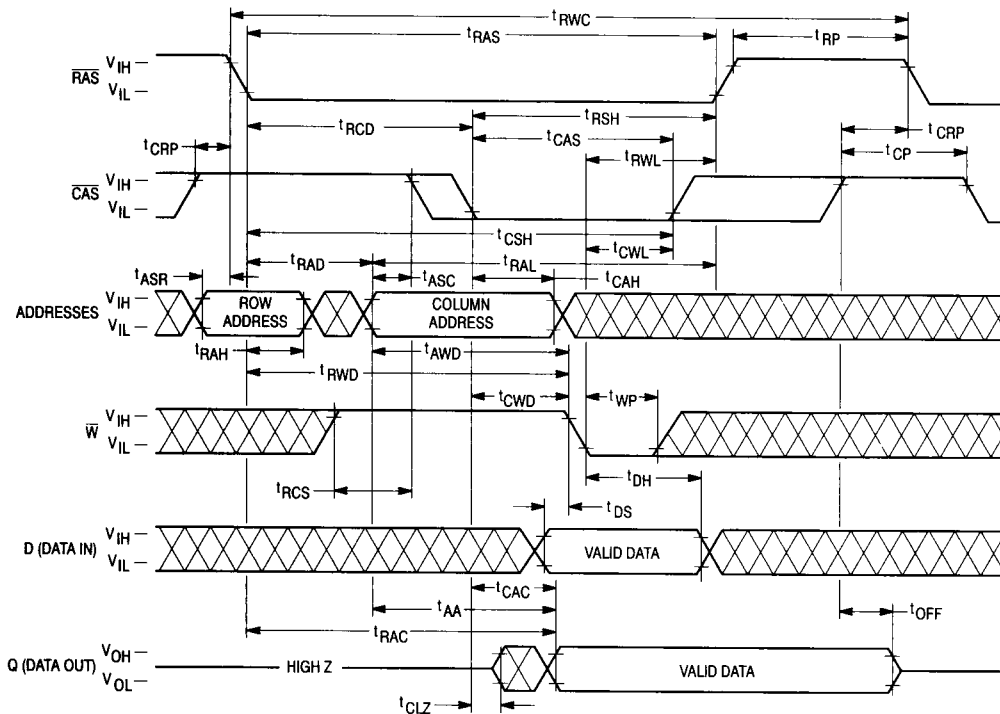
## READ CYCLE



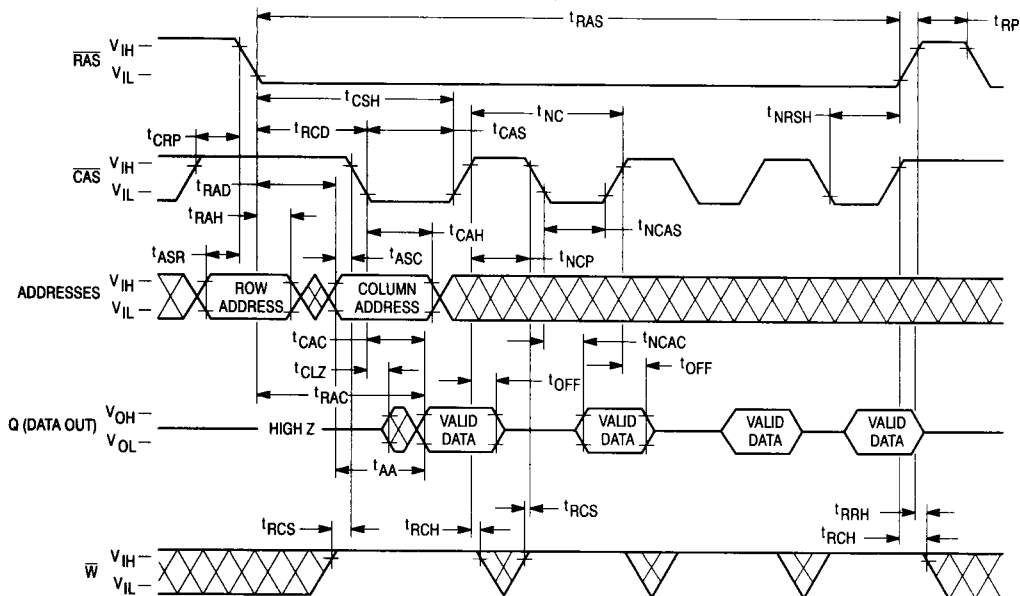
## EARLY WRITE CYCLE



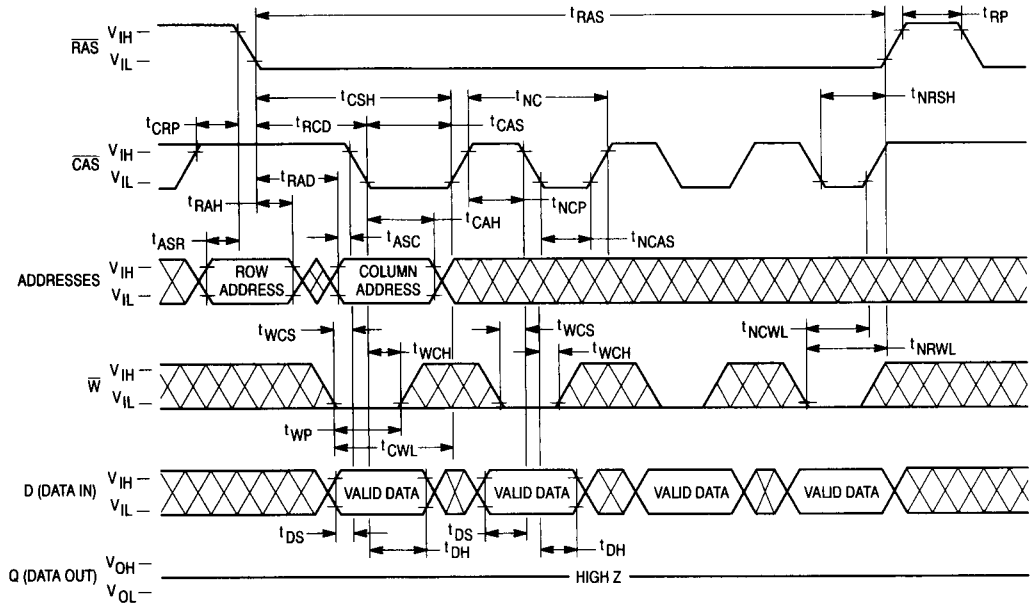
READ-WRITE CYCLE



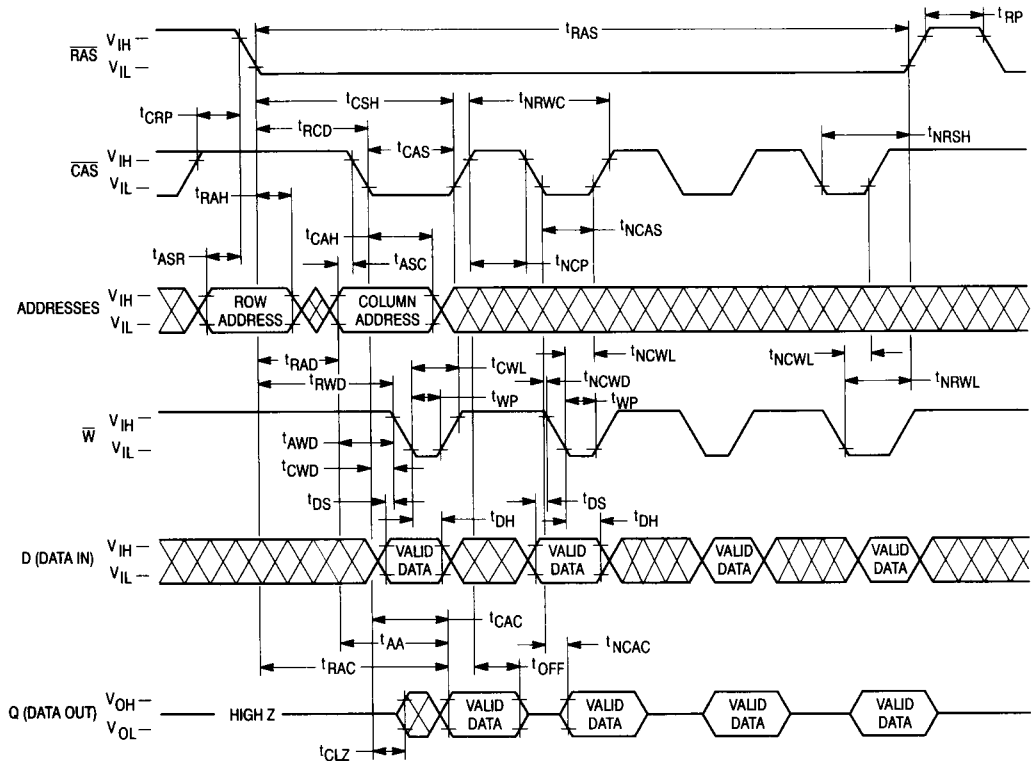
NIBBLE MODE READ CYCLE



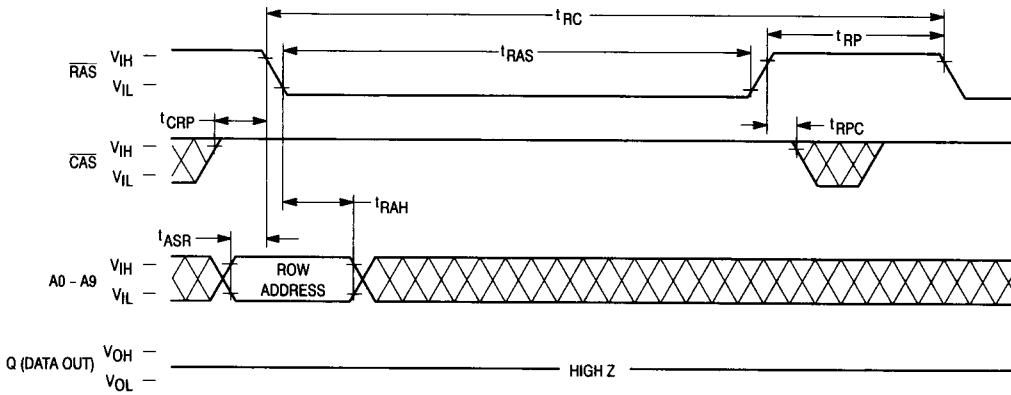
### NIBBLE MODE EARLY WRITE CYCLE



### NIBBLE MODE READ-WRITE CYCLE

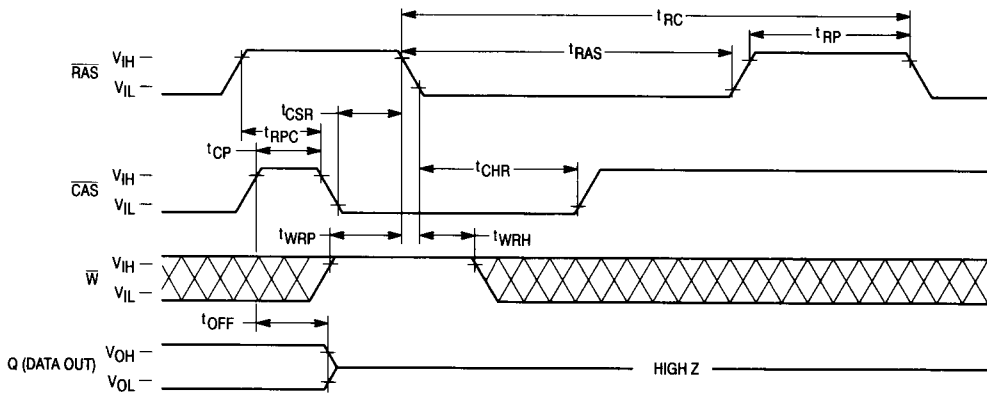


**RAS-ONLY REFRESH CYCLE**  
 (W and A10 are Don't Care)

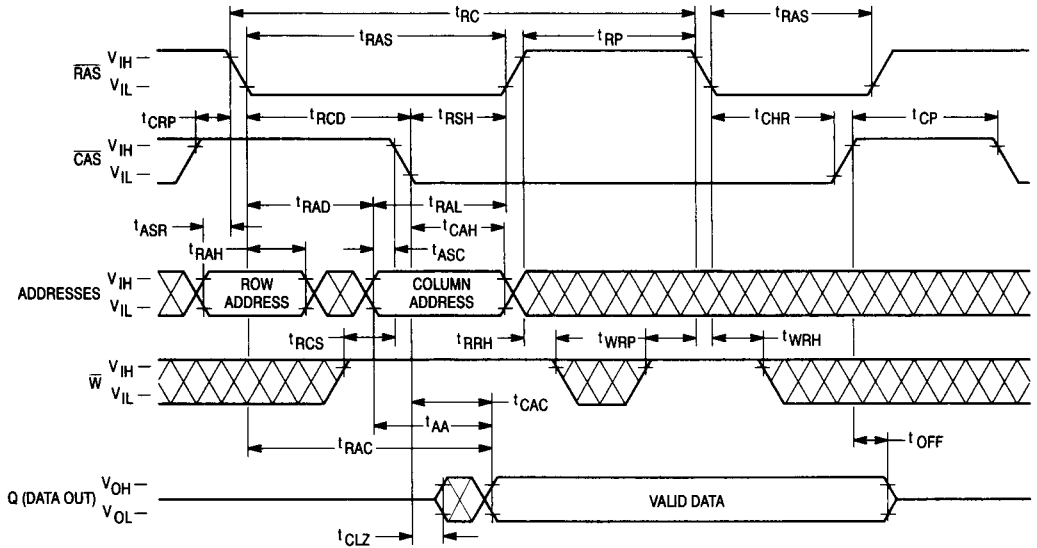


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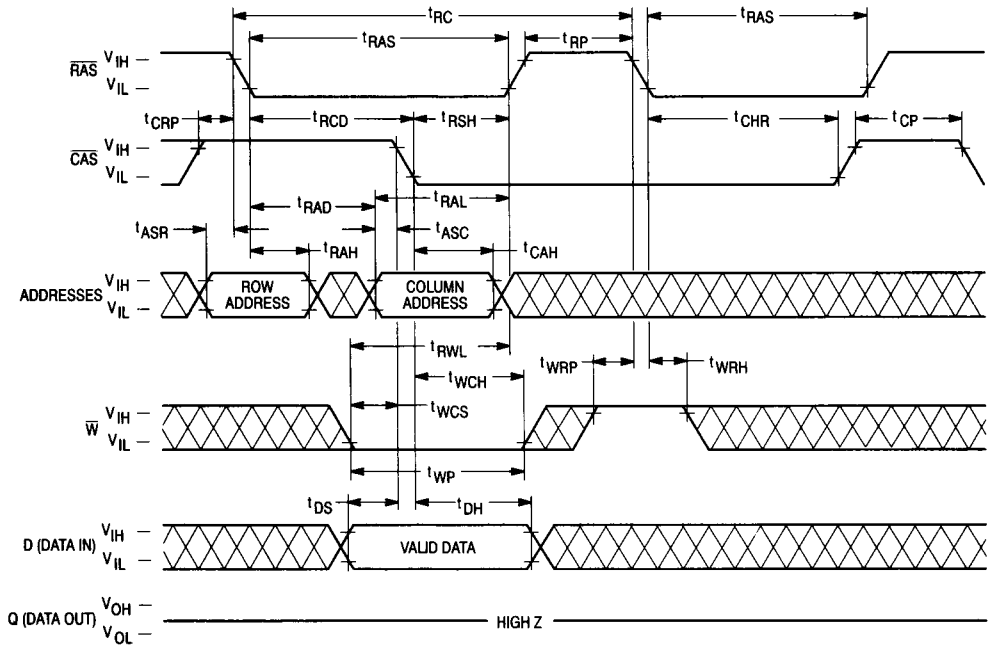
**CAS BEFORE RAS REFRESH CYCLE**  
 (A0 - A10 are Don't Care)



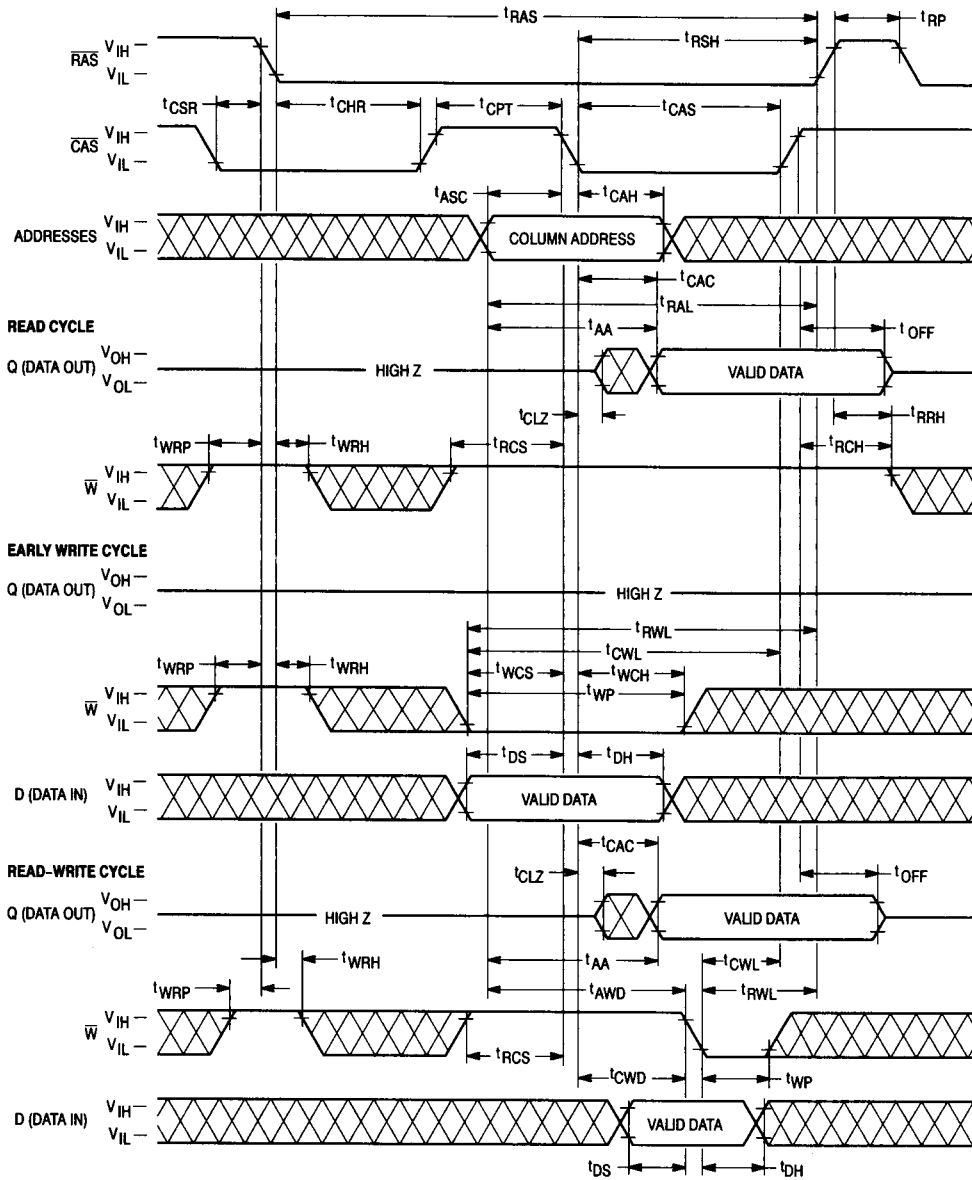
### HIDDEN REFRESH CYCLE (READ)



### HIDDEN REFRESH CYCLE (EARLY WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



## DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds or 128 milliseconds in case of low power device, with the device powered up), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

## ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ( $\overline{\text{RAS}}$ ) and column address strobe ( $\overline{\text{CAS}}$ ), into two separate 11-bit address fields. A total of twenty-two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 bit locations in the device.  $\overline{\text{RAS}}$  active transition is followed by  $\overline{\text{CAS}}$  active transition (active =  $V_{\text{IL}}$ ,  $t_{\text{RCD}}$  minimum) for all read or write cycles. The delay between  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external  $\overline{\text{CAS}}$  signal is ignored until an internal  $\overline{\text{RAS}}$  signal is available. This "gate" feature on the external  $\overline{\text{CAS}}$  clock enables the internal  $\overline{\text{CAS}}$  line as soon as the row address hold time ( $t_{\text{RAH}}$ ) specification is met (and defines  $t_{\text{RCD}}$  minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the  $\overline{\text{CAS}}$  clock.

There are three other variations in addressing the 4M RAM:  **$\overline{\text{RAS}}$ -only refresh cycle**,  **$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle**, and **nibble mode**. All three are discussed in separate sections that follow.

## READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, nibble mode read cycle, read-write cycle, and nibble mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  active transitions latching the desired bit location. The write ( $\overline{\text{W}}$ ) input level must be high ( $V_{\text{IH}}$ ),  $t_{\text{RCS}}$  (minimum) before the  $\overline{\text{CAS}}$  active transition, to enable read mode.

Both the  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window; however,  $\overline{\text{CAS}}$  must be active before or at  $t_{\text{RCD}}$  maximum to guarantee valid data out (Q) at  $t_{\text{RAC}}$  (access time from  $\overline{\text{RAS}}$  active transition). If the  $t_{\text{RCD}}$  maximum is exceeded, read access time is determined by the  $\overline{\text{CAS}}$  clock active transition ( $t_{\text{CAC}}$ ).

The  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  clocks must remain active for minimum times of  $t_{\text{RAS}}$  and  $t_{\text{CAS}}$ , respectively, to complete the read cycle.  $\overline{\text{W}}$  must remain high throughout the cycle, and for time  $t_{\text{RRH}}$  or  $t_{\text{RCH}}$  after  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$  inactive transition, respectively, to maintain the data at that bit location. Once  $\overline{\text{RAS}}$  transitions to inactive, it must remain inactive for a minimum time of  $t_{\text{RP}}$  to precharge the internal device

circuitry for the next active cycle. Q is valid, but not latched, as long as the  $\overline{\text{CAS}}$  clock is active. When the  $\overline{\text{CAS}}$  clock transitions to inactive, the output will switch to High Z (three-state).

## WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, nibble mode early write, and nibble mode read-write. Early and late write modes are discussed here, while nibble mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of  $\overline{\text{W}}$  to active ( $V_{\text{IL}}$ ). Early and late write modes are distinguished by the active transition of  $\overline{\text{W}}$ , with respect to  $\overline{\text{CAS}}$ . Minimum active time  $t_{\text{RAS}}$  and  $t_{\text{CAS}}$ , and precharge time  $t_{\text{RP}}$  apply to write mode, as in the read mode.

An early write cycle is characterized by  $\overline{\text{W}}$  active transition at minimum time  $t_{\text{WCS}}$  before  $\overline{\text{CAS}}$  active transition. Data in (D) is referenced to  $\overline{\text{CAS}}$  in an early write cycle.  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  clocks must stay active for  $t_{\text{RWL}}$  and  $t_{\text{CWL}}$ , respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because  $\overline{\text{W}}$  active transition precedes or coincides with  $\overline{\text{CAS}}$  active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when  $\overline{\text{W}}$  active transition is made after  $\overline{\text{CAS}}$  active transition.  $\overline{\text{W}}$  active transition could be delayed for almost 10 microseconds after  $\overline{\text{CAS}}$  active transition, ( $t_{\text{RCD}} + t_{\text{CWD}} + t_{\text{RWL}} + 2t_{\text{T}} \leq t_{\text{RAS}}$ , if other timing minimums ( $t_{\text{RCD}}$ ,  $t_{\text{RWL}}$ , and  $t_{\text{T}}$ ) are maintained. D is referenced to  $\overline{\text{W}}$  active transition in a late write cycle. Output buffers are enabled by  $\overline{\text{CAS}}$  active transition but Q may be indeterminate — see note 15 of AC Operating Conditions table.  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  must remain active for  $t_{\text{RWL}}$  and  $t_{\text{CWL}}$ , respectively, after  $\overline{\text{W}}$  active transition to complete the write cycle.

## READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except  $\overline{\text{W}}$  must remain high for  $t_{\text{CWD}}$  minimum after the  $\overline{\text{CAS}}$  active transition, to guarantee valid Q before writing the bit.

## NIBBLE MODE CYCLES

Nibble mode allows fast successive serial data operations at two, three, or four bits of the 4M dynamic RAM. Read access time in nibble mode ( $t_{\text{NCAC}}$ ) is considerably faster than the regular  $\overline{\text{RAS}}$  clock access time,  $t_{\text{RAC}}$ . Nibble mode operation consists of keeping  $\overline{\text{RAS}}$  active while toggling  $\overline{\text{CAS}}$  between  $V_{\text{IH}}$  and  $V_{\text{IL}}$ . The address of the first nibble bit is latched by  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  active transitions. Each subsequent  $\overline{\text{CAS}}$  active transition increments the row and column addresses internally to access the next bit in binary fashion. After the fourth bit is accessed, the nibble pattern repeats itself (0,0) (0,1) (1,0) (1,1) (0,0) (0,1) (1,0) (1,1). . . . The A10 address determines the starting point of the 4-bit nibble, with row address A10 the least significant of the (column, row)

ordered pair. External addresses are ignored after the first nibble bit is selected.

A nibble mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met,  $\overline{\text{CAS}}$  transitions to inactive for minimum of  $t_{\text{NCP}}$ , while  $\overline{\text{RAS}}$  remains low ( $V_{\text{IL}}$ ). The second  $\overline{\text{CAS}}$  active transition while  $\overline{\text{RAS}}$  is low initiates the first nibble mode cycle ( $t_{\text{NC}}$  or  $t_{\text{NRWC}}$ ). Either a read, write, or read-write operation can be performed in a nibble mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive nibble mode cycles and performed in any order. The maximum number of consecutive nibble mode cycles is limited by  $t_{\text{RAS}}$ . Nibble mode operation ends when  $\overline{\text{RAS}}$  transitions to inactive, coincident with or following a  $\overline{\text{CAS}}$  inactive transition.

## REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM54101A require refresh every 16 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM54101A. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM54101A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decoded. Three other methods of refresh,  **$\overline{\text{RAS}}$ -only refresh**,  **$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh**, and **hidden refresh** are available on this device for greater system flexibility.

### $\overline{\text{RAS}}$ -Only Refresh

$\overline{\text{RAS}}$ -only refresh consists of  $\overline{\text{RAS}}$  transition to active, latching the row address to be refreshed, while  $\overline{\text{CAS}}$  remains high ( $V_{\text{IH}}$ ) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

### $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh is enabled by bringing  $\overline{\text{CAS}}$  active before  $\overline{\text{RAS}}$ . This clock order activates an internal

refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle.

The output buffer remains at the same state it was in during the previous cycle (hidden refresh).  $\overline{\text{W}}$  must be inactive for time  $t_{\text{WRP}}$  before and time  $t_{\text{WRH}}$  after  $\overline{\text{RAS}}$  active transition to prevent switching the device into **test mode**.

### Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding  $\overline{\text{CAS}}$  active at the end of a read or write cycle, while  $\overline{\text{RAS}}$  cycles inactive  $t_{\text{RP}}$  and back to active, starts the hidden refresh. This is essentially the execution of a  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh from a cycle in progress (see Figure 1).  $\overline{\text{W}}$  is subject to the same conditions with respect to  $\overline{\text{RAS}}$  active transition (to prevent test mode) as in  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh.

### $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Counter Test

The internal refresh counter of this device can be tested with a  **$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See  **$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh counter test cycle timing diagram**.

The test can be performed after a minimum of 8  **$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$**  initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the  **$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the  **$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

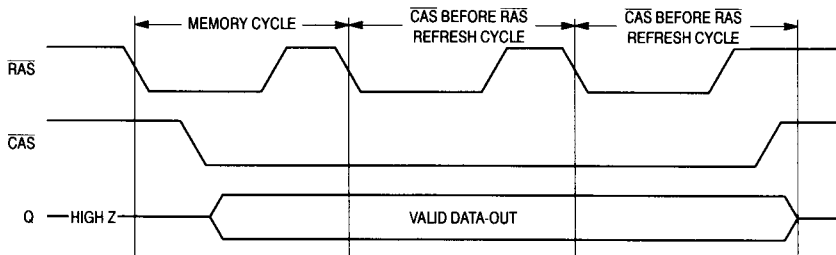


Figure 1. Hidden Refresh Cycle

## TEST MODE

The internal organization of this device (512K x 8) allows it to be tested as if it were a 512K x 1 DRAM. Nineteen of the twenty-two addresses are used when operating the device in test mode. Row address A10, and column addresses A0 and A10 are ignored by the device in test mode. A test mode cycle reads and/or writes data to a bit in each of eight 512K blocks (B0 – B7) in parallel. External data out is determined

by the internal test mode logic of the device. See the following truth table and test mode block diagram.

$\overline{W}$ ,  $\overline{CAS}$  before  $\overline{RAS}$  timing puts the device in **Test Mode** as shown in the test mode timing diagram. A **CAS before RAS** or a **RAS-only refresh cycle** puts the device back into normal mode. Refresh is performed in test mode by using a  **$\overline{W}$ ,  $\overline{CAS}$  before  $\overline{RAS}$  refresh cycle** which uses internal refresh address counter.

TEST MODE TRUTH TABLE

D	B0	B1	B2	B3	B4	B5	B6	B7	Q
0	0	0	0	0	0	0	0	0	1
1	1	1	1	1	1	1	1	1	1
—	Any Other								0

## TEST MODE

### AC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $T_A = 0$  to  $70^\circ\text{C}$ , Unless Otherwise Noted)

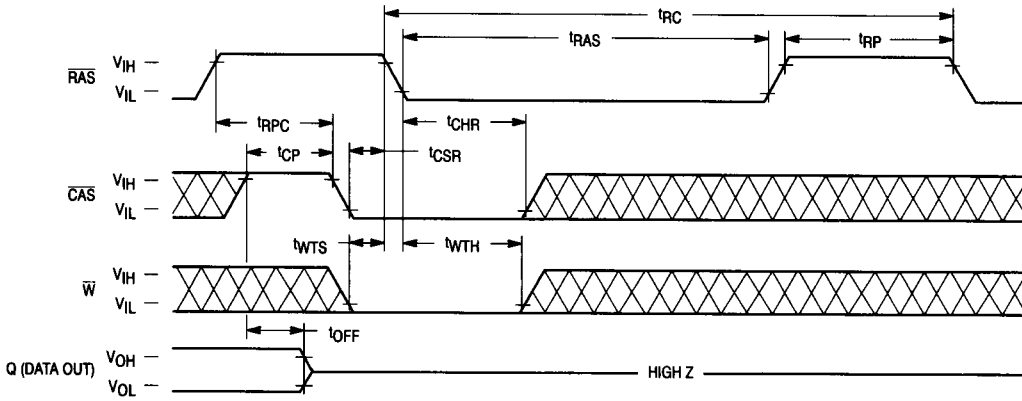
#### READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM54101A-60		MCM54101A-70		MCM54101A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	$t_{RELREL}$	$t_{RC}$	115	—	135	—	155	—	ns	5
Access Time from $\overline{RAS}$	$t_{RELQV}$	$t_{RAC}$	—	65	—	75	—	85	ns	6, 7
Access Time from $\overline{CAS}$	$t_{CELQV}$	$t_{CAC}$	—	25	—	25	—	25	ns	6, 8
Access Time from Column Address	$t_{AVQV}$	$t_{AA}$	—	35	—	40	—	45	ns	6, 9
RAS Pulse Width	$t_{RELREH}$	$t_{RAS}$	65	10 k	75	10 k	85	10 k	ns	
RAS Hold Time	$t_{CELREH}$	$t_{RSH}$	25	—	25	—	25	—	ns	
CAS Hold Time	$t_{RELCEH}$	$t_{CSH}$	65	—	75	—	85	—	ns	
CAS Pulse Width	$t_{CELCEH}$	$t_{CAS}$	25	10 k	25	10 k	25	10 k	ns	
Column Address to $\overline{RAS}$ Lead Time	$t_{AVREH}$	$t_{RAL}$	35	—	40	—	45	—	ns	

#### NOTES:

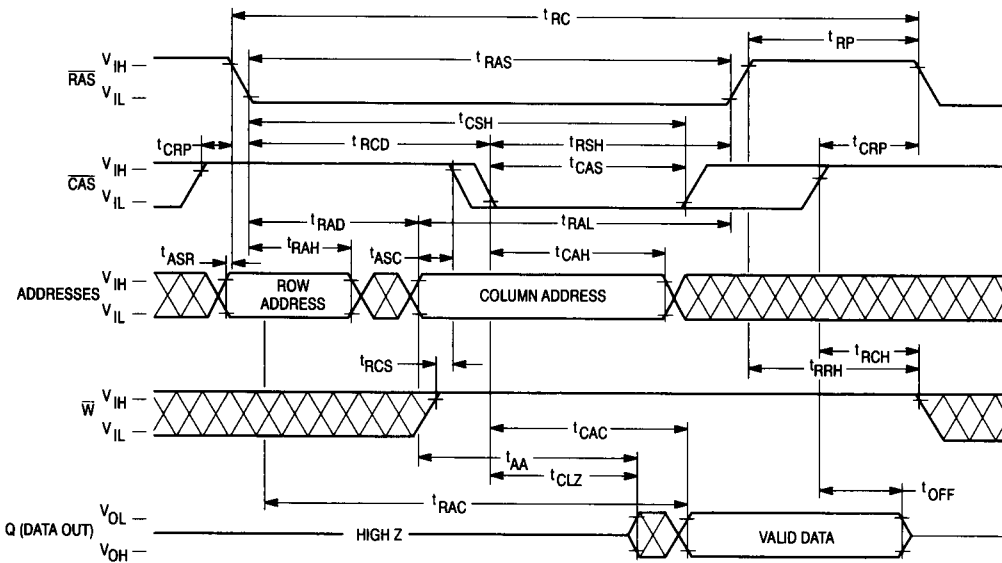
1.  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
2. An initial pause of 200  $\mu\text{s}$  is required after power-up followed by 8  $\overline{RAS}$  cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
4. AC measurements  $t_T = 5.0 \text{ ns}$ .
5. The specifications for  $t_{RC}$  (min) and  $t_{RWC}$  (min) are used only to indicate cycle time at which proper operation over the full temperature range ( $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ) is ensured.
6. Measured with a current load equivalent to 2 TTL ( $-200 \mu\text{A}$ ,  $+4 \text{ mA}$ ) loads and 100 pF with the data output trip points set at  $V_{OH} = 2.0 \text{ V}$  and  $V_{OL} = 0.8 \text{ V}$ .
7. Assumes that  $t_{RCD} \leq t_{RCD}(\text{max})$ .
8. Assumes that  $t_{RCD} \geq t_{RCD}(\text{max})$ .
9. Assumes that  $t_{RAD} \geq t_{RAD}(\text{max})$ .

**W, CAS BEFORE RAS REFRESH CYCLE (TEST MODE ENTRY)**  
 (D and A0 - A10 are Don't Care)

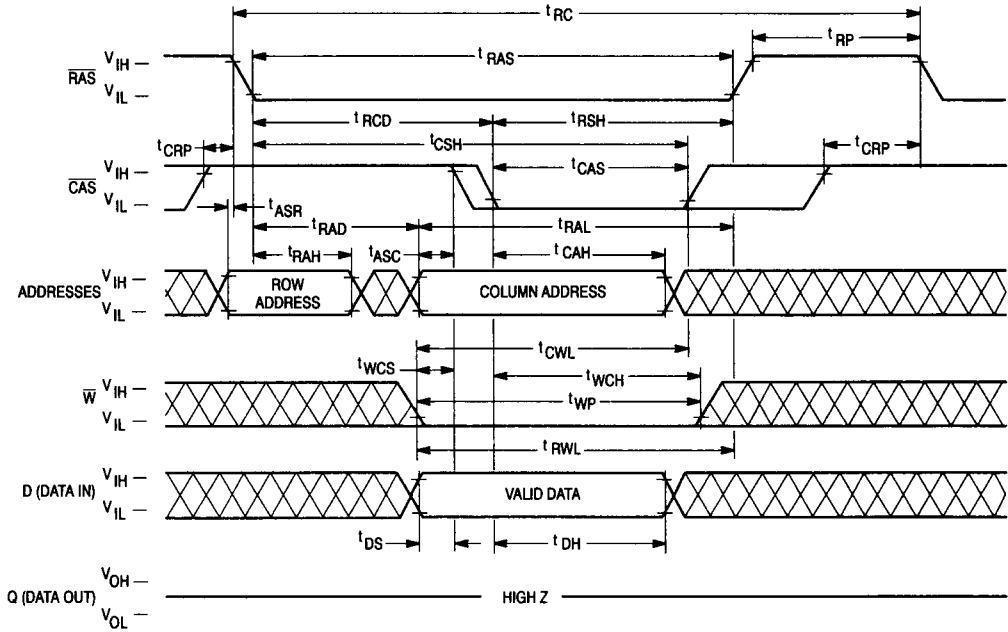


3

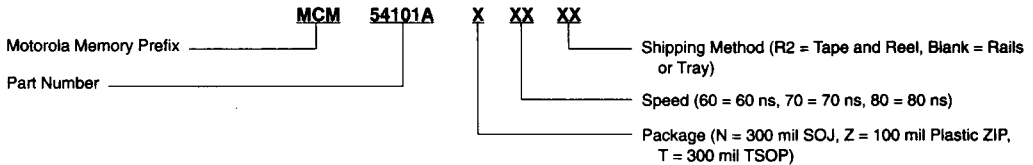
**TEST MODE — READ CYCLE**



### TEST MODE — EARLY WRITE CYCLE



### ORDERING INFORMATION (Order by Full Part Number)



Full Part Numbers —	MCM54101AN60	MCM54101AN60R2	MCM54101AZ60	MCM54101AT60
	MCM54101AN70	MCM54101AN70R2	MCM54101AZ70	MCM54101AT70
	MCM54101AN80	MCM54101AN80R2	MCM54101AZ80	MCM54101AT80

NOTE: For mechanical data, please see Chapter 10.

TEST MODE BLOCK DIAGRAM

