# CMOS EXPANDABLE 4-WIDE, 2-INPUT AND-OR INVERT GATE

## FEATURES

- Medium-speed operation – $t_{PHL}$ = 90 ns; $t_{PLH}$ = 140 ns (typ.) at 10 V
- INHIBIT and ENABLE inputs
- Buffered outputs
- 100% tested for quiescent current at 15 V
- Maximum input leakage current of 1μA over full package-temperature range; 100 nA at 15 V and 25° C
- Noise margin (over full package temperature range):
  1 V at $V_{DD}$ = 5 V
  2 V at $V_{DD}$ = 10 V
  2.5 V at $V_{DD}$ = 15 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

## DESCRIPTION

The 4086B contains one 4-wide 2-input AND-OR-INVERT gate with an INHIBIT/$\overline{EXP}$ input and an ENABLE/EXP input. For a 4-wide A-O-I-function INHIBIT/EXP is tied to $V_{SS}$ and ENABLE/EXP to $V_{DD}$. See Fig. 2 and its associated explanation for applications where a capability greater than 4-wide is required.

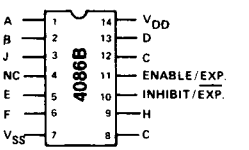
The 4086B is supplied in 14-lead dual-in-line ceramic packages (D and C suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packs (F suffix), and in chip form (H suffix).

## RECOMMENDED OPERATING CONDITIONS

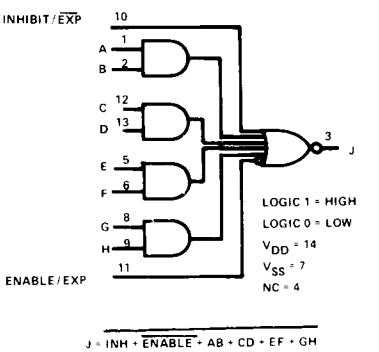
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | Min. | Max. | |
| Supply Voltage Range (For $T_A$ = Full Package Temperature Range) | 3 | 18 | V |

CONNECTION DIAGRAM




TOPVIEW




FUNCTIONAL DIAGRAM

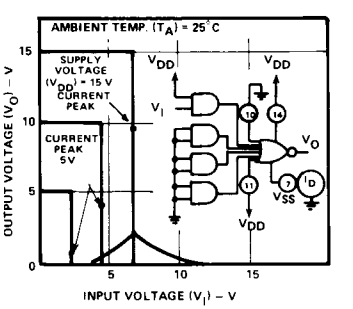



FIGURE 1
TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

# ELECTRICAL CHARACTERISTICS

## STATIC CHARACTERISTICS [1]

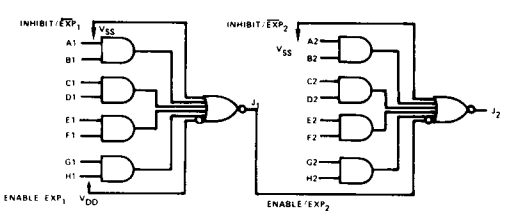
| PARAMETER | | $V_{DD}$ (Vdc) | CONDITIONS | $T_{LOW}$ [2] | | +25°C | | | $T_{HIGH}$ [2] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Typ. | Max. | Min. | Max. | |
| QUIESCENT DEVICE CURRENT | $I_{DD}$ | 5 | $V_{IN}$ = $V_{SS}$ or $V_{DD}$ | – | 0.05 | – | 0.0005 | 0.05 | – | 1.5 | μAdc |
| | | 10 | All valid input | – | 0.10 | – | 0.001 | 0.10 | – | 3.0 | |
| | | 15 | combinations | – | 0.20 | – | 0.002 | 0.20 | – | 6.0 | |

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] $T_{LOW}$ = -55°C for C, D, F, H device.
= -40°C for E device.
$T_{HIGH}$ = +125°C for C, D, F, H device.
= + 85°C for E device.

## ABSOLUTE MAXIMUM RATINGS

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
(Voltages referenced to $V_{SS}$ Terminal) . . . . . −0.5 to + 18 V
INPUT VOLTAGE RANGE,
ALL INPUTS . . . . . −0.5 to $V_{DD}$ +0.5 V
DC INPUT CURRENT,
ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = −40 to +60° C
(PACKAGE TYPE E) . . . . . 500 mW
For $T_A$ = +60 to +85° C
(PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/° C to 200 mW
For $T_A$ = −55 to +100° C
(PACKAGE TYPES D, C, F) . . . . 500 mW
For $T_A$ = +100 to +125° C
(PACKAGE TYPES D, C, F) . . . . . Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION
PER OUTPUT TRANSISTOR
For $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types). . . . 100 mW
OPERATING TEMPERATURE RANGE ($T_A$):
PACKAGE TYPES D, F, C, H −55 to +125° C
PACKAGE TYPE E −40 to +85° C
STORAGE TEMPERATURE
RANGE ($T_{stg}$) . . . . . −65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265° C

Fig. 3 shows two 4086's utilized to obtain an 8-wide 2-input A·O·I function. The output (J1) of one 4086 is fed directly to the ENABLE/EXP2 line of the second 4086. In a similar fashion, any NAND gate output can be fed directly into the ENABLE/EXP input to obtain a 5-wide A·O·I function. In addition, any AND gate output can be fed directly into the INHIBIT/$\overline{EXP}$ input with the same result.



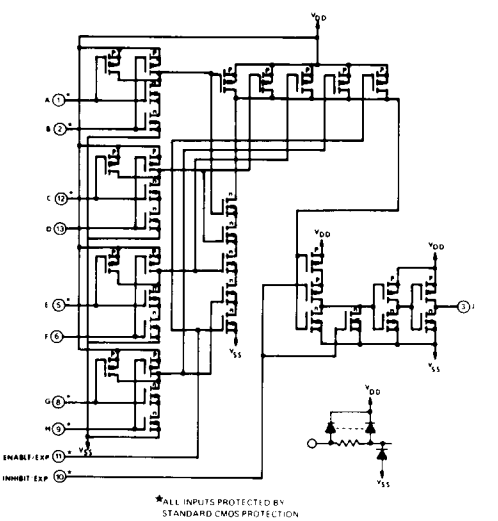

$J2 = \overline{A1 \cdot B1 \cdot C1 \cdot D1 \cdot E1 \cdot F1 \cdot G1 \cdot H1 + A2 \cdot B2 \cdot C2 \cdot D2 \cdot E2 \cdot F2 \cdot H2}$

TWO 4086B'S CONNECTED
AS AN 8 WIDE 2 INPUT A.O.I GATE

## DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A$ = 25°C; Input $t_r$, $t_f$ = 20ns, $C_L$ = 50pF, $R_L$ = 200KΩ)

| CHARACTERISTIC | CONDITIONS | LIMITS | | UNITS |
|---|---|---|---|---|
| | $V_{DD}$ (V) | TYP. | MAX. | |
| Propagation Delay Time (Data) High-to-Low Level, $t_{PHL}$ | 5 | 225 | 450 | ns |
| | 10 | 90 | 180 | |
| | 15 | 60 | 120 | |
| Low-to-High Level, $t_{PLH}$ | 5 | 350 | 700 | ns |
| | 10 | 140 | 280 | |
| | 15 | 100 | 200 | |
| Propagation Delay Time (Inhibit) High to Low Level, $t_{PHL(INH)}$ | 5 | 150 | 300 | ns |
| | 10 | 60 | 120 | |
| | 15 | 40 | 80 | |
| Low to High Level, $t_{PLH(INH)}$ | 5 | 250 | 500 | ns |
| | 10 | 100 | 200 | |
| | 15 | 70 | 140 | |
| Transition Time, $t_{THL}$, $t_{TLH}$ | 5 | 100 | 200 | ns |
| | 10 | 50 | 100 | |
| | 15 | 40 | 80 | |
| Input Capacitance $C_{IN}$ | Any Input | 5 | 7.5 | pF |




*ALL INPUTS PROTECTED BY STANDARD CMOS PROTECTION NETWORK