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A TDK Group Company

SSI 78Q2250
155 Mbit/s ATM Line Transceiver

Preliminary Data

March 1996

DESCRIPTION

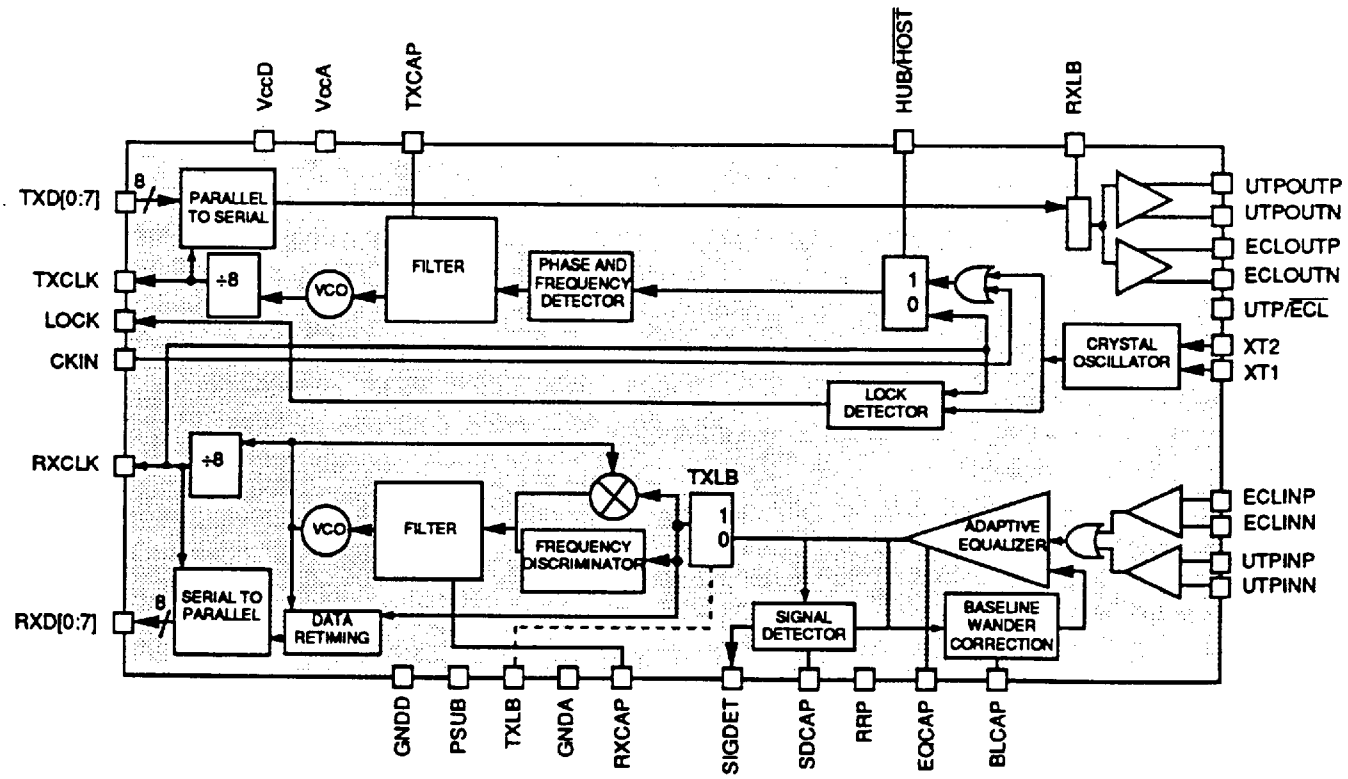
The SSI 78Q2250 is a high-speed line transceiver integrated circuit intended for use in Asynchronous Transfer Mode (ATM) applications. It is used at the interface to Category 5 Unshielded Twisted-Pair (UTP) cabling and is connected to the line via isolation transformers. Optionally, a PECL interface is provided for use with an optical interface device. Interface to digital framer circuits is accomplished via 8-bit parallel CMOS I/O running at 19.44 Mbit/s.

The IC provides full transmit and receive line interface functions with minimum external components required. The receiver provides adaptive equalization for accurate clock and data recovery. The 78Q2250 is built in a BiCMOS technology for highest performance and low power operation, and is housed in a 48-Pin TQFP package.

FEATURES

- **155.52 Mbit/s Interface for Category 5 Unshielded Twisted Pair (UTP) cable**
- **Compliant with ATM PMD Interface specification for 155.52 Mbit/s over Twisted Pair Cable**
- **Parallel CMOS logic interface at 19.44 Mbit/s**
- **PECL interfaces for connection to fiber optic receive and transmit modules**
- **Automatic gain adaptive equalization**
- **Baseline wander correction**
- **Receive clock and data recovery**
- **Advanced BICMOS processing**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The SSI 78Q2250 is an ATM line transceiver IC that contains all the necessary transmit and receive circuitry for connection between 155 Mbit/s line signals and digital Framer/Deframer ICs. The device provides connection to up to 100 meters of category 5 UTP via isolating transformers. The receiver includes adaptive equalization, baseline wander correction, clock and data recovery and serial-to-parallel conversion. The transmitter includes parallel-to-serial conversion, signal clocking from either a crystal or recovered clock and line driver.

TRANSMITTER OPERATION

The transmitter section accepts 8-bit parallel data at 19.44 MHz, serializes it into a 155.52 Mbit/s data signal, and generates an analog signal for transmission through a transformer onto the UTP cable. Clocks for the parallel and serial data signals are generated from a crystal oscillator using a PLL which phase locks a high frequency VCO to the crystal reference frequency via an 8x frequency divider.

Transmitter operation is affected by various mode signals. The HUB/$\overline{\text{HOST}}$ input changes the reference signal for the clock generator. In the hub mode, the transmit clock reference is derived from either the crystal oscillator or CKIN, as described below. In host mode, the transmit clock reference is derived from the receiver recovered clock.

The UTP/$\overline{\text{ECL}}$ input selects the output interface to be used. In UTP mode, the pins UTPOUTP/N are active and connect the chip to the UTP cable through a transformer and a matching resistor as shown in Figure 2. In UTP mode, ECLOUTP/N are inoperative and should be left open. In ECL mode, the UTP pins are inoperative and should be left open and the output data signal comes from pins ECLOUTP/N as differential ECL as illustrated in Figure 3. This allows the chip to drive an optical transceiver.

An external clock signal (CMOS) at CKIN may be substituted for a crystal as the reference frequency for the chip. In this mode, XT1 and XT2 must be configured as shown in Figure 3. Note that the chip can be in either ECL or UTP mode when using either an external clock or a crystal for the reference. CKIN should be tied to Vcc when using a crystal as shown in Figure 2.

RECEIVER OPERATION

The receiver section accepts serial NRZ data at 155.52 Mbit/s either from the UTP or the ECL inputs, equalizes it for cable dispersion, corrects it for baseline wander, recovers a 155.52 MHz clock signal, and converts the data to an 8-bit parallel signal with a corresponding 19.44 MHz clock. When operating the receiver in ECL mode, the UTPINP/N should be left open and, when operating in UTP mode, the ECLINP/N pins should be left open.

In UTP mode, the inputs UTPINP/N receive the 155.52 MHz input signal from Category 5 UTP cable (100 meters maximum length) which is transformer-coupled to the chip as shown in Figure 2. The output SIGDET goes high when the signal detect circuitry determines that a signal is present.

The signal is equalized for the dispersive effects of the cable by the adaptive equalizer section, which searches for a particular signal level and adds a filtered version of the input signal until it detects the right level.

The signal is also corrected for the baseline wander. This is a condition where the effects of the data pattern and the droop of the transformers cause the input data signal to have a non-zero DC component or "baseline." The baseline wander correction circuit analyzes the positive and negative pulse levels as they emerge from the adaptive equalizer and adjusts the DC component of the equalizer's input signal. The detection scheme of the baseline wander circuit and the difference in the time constants between it and the adaptive equalizer prevent the two control loops from contending.

The receive PLL recovers a 155.52 MHz clock signal from the equalized data signal. The NRZ data signal is rectified and filtered to generate a 155.52 MHz tone and then it goes into a multiplier-type phase detector.

The loop uses a VCO similar to the one in the transmitter. Frequency acquisition is performed by a quadricorrelator circuit which forces the VCO to a frequency close enough for the loop to self-acquire. A lock detector compares the frequency of the output of the receive PLL to that of the crystal (or the external clock reference). When the frequencies are close enough, its output, LOCK, is asserted indicating that the receive PLL is frequency-locked.

Once the equalized data signal is re-timed with the recovered clock, it is converted to 8 parallel bits and sent off-chip with a 19.44 MHz clock.

LOOPBACK OPERATION

The 78Q2250 is capable of performing signal loopback in two directions. The RXLB pin selects the receive loopback mode. In this mode, the received signal is "looped back" and sent out of transmitter in place of the transmit input signal. The TXLB pin selects the transmit loopback mode, and causes the receiver to use the transmitter output signal as its input. In this case both sets of receive input signals (UTP and ECL) are ignored. Note, the chip should not be in TXLB and HOST mode at the same time.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
TXD [7-0]	I,C	Transmit Data Input. The parallel transmit data is converted to serial, bit 7 first.
TXCLK	O,C	Transmit clock output. 19.44 MHz.
CKIN	I,C	Optional 19.44 MHz input for the reference clock. The crystal oscillator external components should be configured as in Figure 3.
ECLOUTP, ECLOUTN	O,E	Active transmit outputs when the chip is in ECL mode. See Figure 3. These outputs are Pseudo ECL, referenced to Vcc.
UTPOUTP, UTPOUTN	O	Active transmit output in UTP mode. See Figure 2.
TXCAP	-	Auxiliary transmit PLL loop filter capacitor.
RXLB	I, C	Loopback receiver input to transmitter output.
UPTINP UTPINN	I	Active receiver inputs in UTP mode. See Figure 2.
ECLINP, ECLINN	I,E	Active receiver inputs in ECL mode. See Figure 3. These inputs are Pseudo ECL, referenced to Vcc.
RXCLK	O,C	Recovered receive clock. 19.44 MHz.
RXD[7-0]	O,C	Receive data. The first bit in the serial stream appears on bit 7.
RXCAP	-	Auxiliary loop filter capacitor for clock recovery PLL.
TXLB	I,C	Loopback transmitter input to receiver output.
SIGDET	O,C	High when an active receive input is detected.
LOCK	O,C	High when the receive PLL is locked.
HUB/$\overline{\text{HOST}}$	I,C	Configures the circuit in Hub (input high) or Host mode (input low).
UTP/$\overline{\text{ECL}}$	I,C	Selects UPT (input high) or ECL (input low) modes.
RRP	-	External reference resistor 10 kΩ ± 1%.
XT1, XT2	-	Crystal Oscillator Inputs. 19.44 MHz crystal.
VccA, VccD	S	Supply Voltage.
GNDD, PSUB, GNDA	S	Ground.
SDCAP	-	Auxiliary signal detector capacitor.
EQCAP	-	Auxiliary equalizer capacitor.
BLCAP	-	Auxiliary baseline wander capacitor.
EQOUT	-	Test pin used by factory, leave open.

NOTES: Pin Type: I - Input; O - Output; S - Supply; C - CMOS digital; E - Differential ECL

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation of the IC beyond these limits may result in damage.

PARAMETER		RATING
Ambient Temperature		-40 to 85°C
Junction Temperature	θja = 70°C/W	-40 to 100°C
Lead Temperature	Soldering, 10 sec.	235°C (IR)
Supply Voltage		6V
Power Dissipation	Ta = 85°C, Tj = 125°C	350 mW
Pin Voltage		-0.3 to Vcc + 0.3V
Pin Current		100 mA

POWER SUPPLY

The following specifications are met for the conditions: 0°C < Ta < 70°C and 3.0 < Vcc < 5.5

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Supply Current	(UTP Mode)			65	85	mA
Supply Voltage	(ECL Mode)			65	85	mA

DIGITAL INTERFACE

The following specifications refer to the CMOS interface pins: RXD[7-0], RXCLK, TXD[7-0], TXCLK, CKIN, LOCK, TXLB, RXLB, SIGDET, HUB/$\overline{\text{HOST}}$, UTP/$\overline{\text{ECL}}$.

V_{IL}	3.0 ≤ Vcc ≤ 5.5			Vcc • 0.2	V
V_{IH}	3.0 ≤ Vcc ≤ 5.5	Vcc • 0.8			V
I_{IL}		-100		100	µA
I_{IH}		-100		100	µA
Input Capacitance			10		pF
V_{OL}	I = 100 µA			200	mV
V_{OH}	I = -100 µA	Vcc - 0.2			V

ELECTRICAL SPECIFICATIONS (continued)

EXTERNAL COMPONENTS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
External Reference Resistor	R_{RP}	1% Tolerance		10		kΩ
Crystal				19.44		MHz
Crystal Capacitor	C_{XT}			27		pF
TX Loop Filter Capacitor	C_{TX}			TBD		
RX Loop Filter Capacitor	C_{RX}			TBD		
Line Transformer Turns Ratio	T_L			1:1		
TX Termination Resistor	R_{TT}			50		Ω
RX Termination Resistor	R_{TR}			100		Ω
Signal Detector Capacitor	C_{SD}			TBD		
Equalizer Capacitor	C_{EQ}			TBD		
Baseline Wander Capacitor	C_{BL}			TBD		

TRANSMITTER

The following are the specifications for the Transmitter section. They assume use of the external components as listed in this data sheet and up to 100 meters of Category 5 Unshielded Twisted Pair (UTP) Cable.

TXD Setup Time	T_{SU}	Refer to figure 1	20			ns
TXD Hold Time	T_H	Refer to figure 1	20			ns
TXCLK Period	T_{PER}	Refer to figure 1		52.6		ns
TXCLK Duty Cycle	T_{DC}	Refer to figure 1	40		60	%
Output Voltage		Peak-to-peak differential	0.94	1	1.06	V
Output Voltage Overshoot		Beyond final output voltage value			10	%
Output Voltage Setting		To final output voltage			3.2	ns
Output Jitter		Peak-to-peak			2	ns
NRZ Pulse Duty Cycle		0101 Pattern best fit to a 6.43 ns grid	-0.25		0.25	ns
Rise/ Fall Time		10-90%	1.5		3.5	ns
Rise/ Fall Imbalance					0.5	ns
Baseline Wander		100 Consecutive bits of logical ones		10		%

ECL TRANSMITTER OUTPUTS

Voh	Relative to Vcc		-0.8	-0.7	V
Vol	Relative to Vcc	-1.9	-1.8		V
Rise Time			1		ns
Fall Time			2.5		ns

RECEIVER

The following are the specifications for the Receiver section. They assume use of the external components as listed in this data sheet and up to 100 meters of Category 5 Unshielded Twisted Pair (UTP) Cable.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
RXCLK Period RPER	Refer to figure 1		52.6		ns
RXCLK Duty Cycle RDC	Refer to figure 1	40		60	%
RXCLK to Data Propagation Delay, R_{prop}	Refer to figure 1		2		ns
Baseline Wander Tolerance			10		%
Maximum Cable Length	Category 5 UTP		100		m
Bit Error-rate	100m Cat. 5 UTP		10^{-10}		
Input Voltage at UPT Inputs				1.06	V
Maximum Output Jitter	Random data, 100m cable			2	ns

ECL RECEIVER INPUTS

Vil	Relative to Vcc	-1.8			V
Vih	Relative to Vcc			-1	V
Duty Cycle		40		60	%

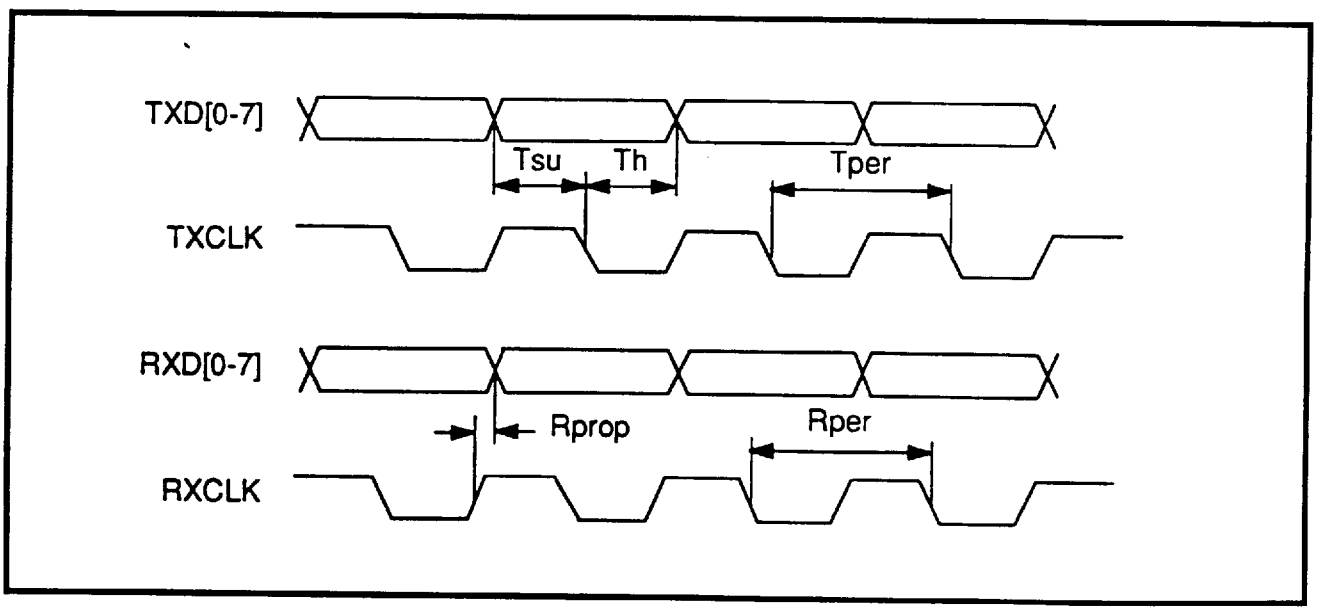
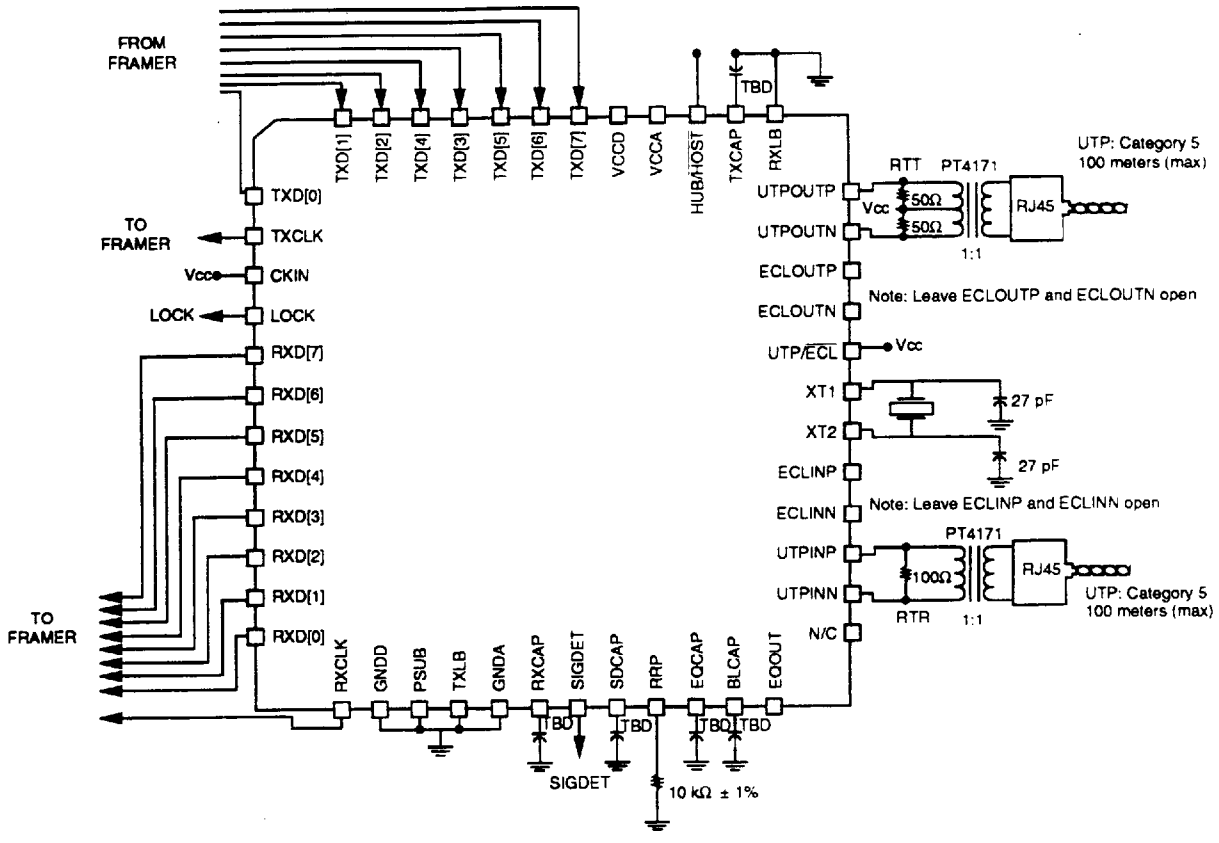
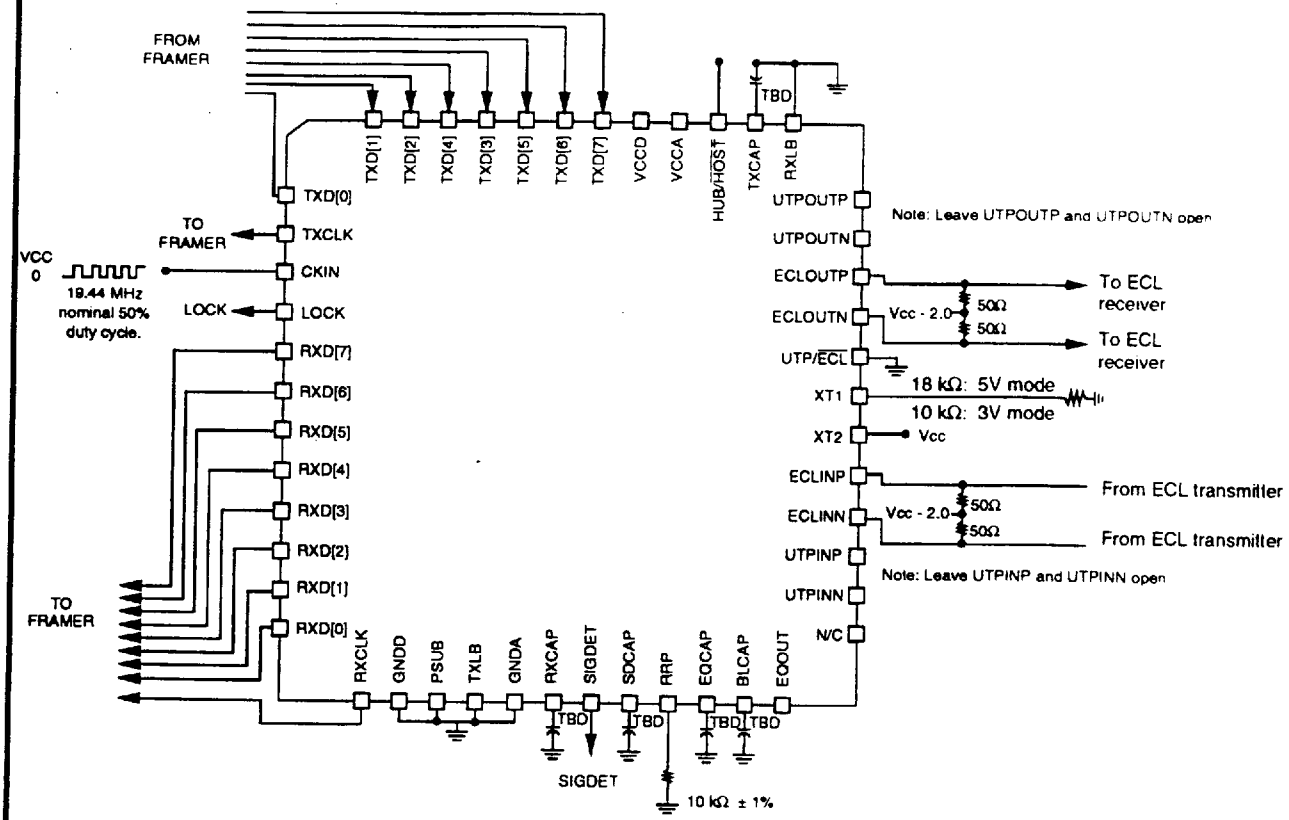


FIGURE: 1 Timing for CMOS I/O



NOTE: UTP mode may also be configured with external clock reference as shown in Figure 3

FIGURE: 2 Circuit Configuration for UTP Mode with Crystal Oscillator Reference

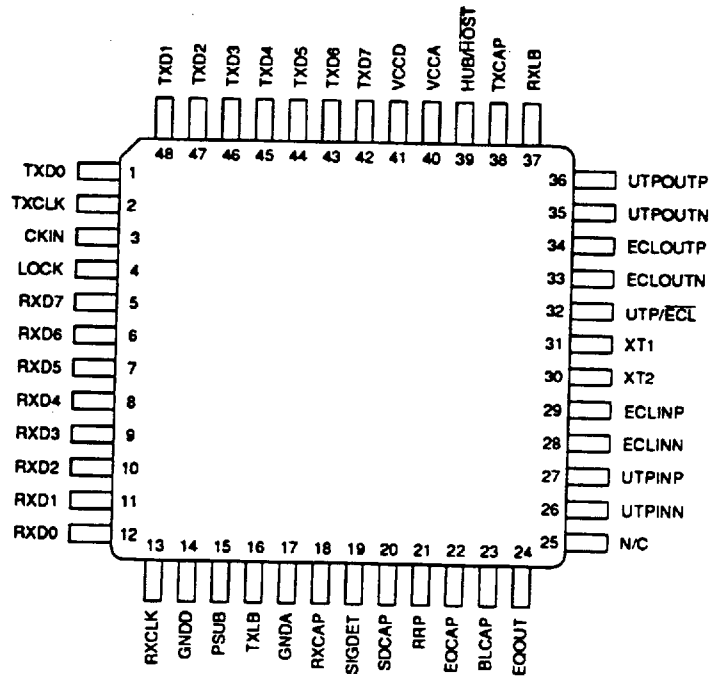


NOTE: ECL mode may also be configured with crystal oscillator reference as shown in Figure 2

FIGURE: 3 Circuit Configuration for ECL Mode with External Clock Reference

PACKAGE PIN DESIGNATIONS

(Top View)



48-Lead TQFP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 78Q2250 155 Mbit/s ATM Transceiver 48-Pin TQFP	78Q2250-CGT	78Q2250-CGT

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