

## 16M x 4 12/12 EDO DRAM

### Features

- 16,777,216 word by 4 bit organization
- Single 3.3 ± 0.3V power supply
- Extended Data Out
- $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  Refresh
  - 4096 cycles/Retention Time
- $\overline{\text{RAS}}$  only Refresh
  - 4096 cycles/Retention Time
- 64ms Standard Power (SP) Retention Time
- 256ms Low Power (LP) Retention Time
- Hidden Refresh
- Self Refresh (400µA) - LP Version Only

- Read-Modify-Write
- Performance:

|                  |                                     | -50  | -60   |
|------------------|-------------------------------------|------|-------|
| $t_{\text{RAC}}$ | $\overline{\text{RAS}}$ Access Time | 50ns | 60ns  |
| $t_{\text{CAC}}$ | $\overline{\text{CAS}}$ Access Time | 13ns | 15ns  |
| $t_{\text{AA}}$  | Column Address Access Time          | 25ns | 30ns  |
| $t_{\text{RC}}$  | Cycle Time                          | 84ns | 104ns |
| $t_{\text{HPC}}$ | EDO (Hyper Page) Mode Cycle Time    | 20ns | 25ns  |

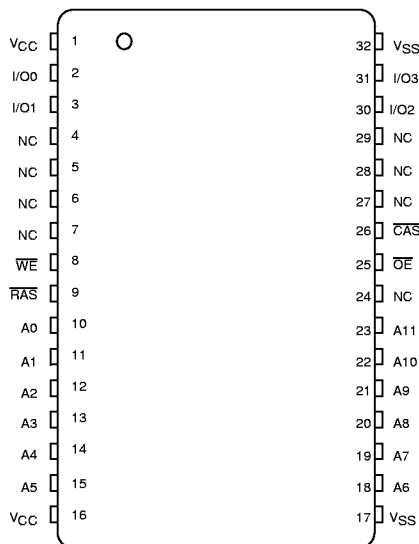
- Max. Power Dissipation (-50)
  - Active: 504mW
  - Standby (SP version): 2.0mA
  - Standby (LP version): 0.2 mA
- Package: SOJ-32 (400mil), TSOP-32 (400mil)

### Description

The IBM0165405B/P is a dynamic RAM organized 16,777,216 words by 4 bits. This device is fabricated in IBM's most advanced CMOS silicon gate process technology. The circuit and process design allow this DRAM to achieve high performance and low power dissipation. The IBM0165405B/P operates with a single 3.3 ± 0.3V power supply, and interfaces directly with either TTL or CMOS levels. The 24 addresses required to access any bit of data are

multiplexed (12 are strobed with  $\overline{\text{RAS}}$ , 12 are strobed with  $\overline{\text{CAS}}$ ). They are packaged in a 32 pin plastic SOJ (400mil×825mil), and a 32 pin plastic TSOP type II (400mil×825mil). The IBM0165405P parts are low power devices supporting Self Refresh and a 256ms retention time.

### Pin Assignments (Top View)



### Pin Description

|                         |                       |
|-------------------------|-----------------------|
| $\overline{\text{RAS}}$ | Row Address Strobe    |
| $\overline{\text{CAS}}$ | Column Address Strobe |
| $\overline{\text{WE}}$  | Read/write Input      |
| A0 - A11                | Address Inputs        |
| $\overline{\text{OE}}$  | Output Enable         |
| I/O0 - I/O3             | Data Input/output     |
| $V_{\text{CC}}$         | Power (+3.3V)         |
| $V_{\text{SS}}$         | Ground                |

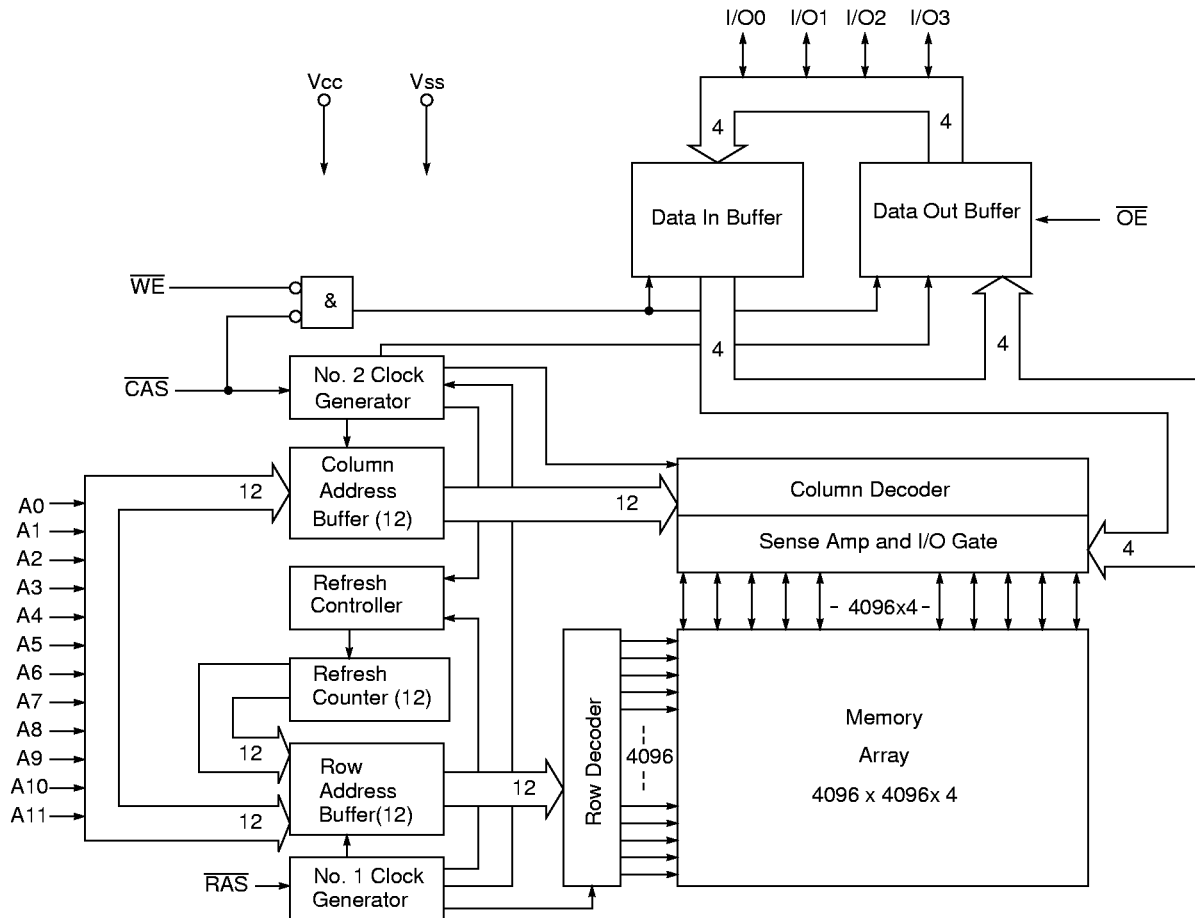


### Ordering Information

| Part Number       | Power | Self Refresh | Power Supply | Speed | Package        | Notes |
|-------------------|-------|--------------|--------------|-------|----------------|-------|
| IBM0165405BJ3C-50 | SP    | No           | 3.3V         | 50ns  | 400mil SOJ 32  | 1     |
| IBM0165405BJ3C-60 | SP    | No           | 3.3V         | 60ns  | 400mil SOJ 32  | 1     |
| IBM0165405BT3C-50 | SP    | No           | 3.3V         | 50ns  | 400mil TSOP 32 | 1     |
| IBM0165405BT3C-60 | SP    | No           | 3.3V         | 60ns  | 400mil TSOP 32 | 1     |
| IBM0165405PT3C-50 | LP    | Yes          | 3.3V         | 50ns  | 400mil TSOP 32 | 1     |
| IBM0165405PT3C-60 | LP    | Yes          | 3.3V         | 60ns  | 400mil TSOP 32 | 1     |

1. SP = Standard Power version (IBM0165405B); LP = Low Power version (IBM0165405P)

### Block Diagram





## Truth Table

| Function   |           | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | $\overline{OE}$ | Row Address | Column Address | I/O0 - I/O3       |
|--|-----------|------------------|------------------|-----------------|-----------------|-------------|----------------|-------------------|
| Standby  |           | H                | H→X              | X               | X               | X           | X              | High Impedance    |
| Read   |           | L                | L                | H               | L               | Row         | Col.           | Data Out          |
| Early-Write  |           | L                | L                | L               | X               | Row         | Col.           | Data In           |
| Delayed-Write                                      |           | L                | L                | H→L             | H               | Row         | Col.           | Data In           |
| Read-Modify-Write                                  |           | L                | L                | H→L             | L→H             | Row         | Col.           | Data Out, Data In |
| EDO (Hyper Page) Mode Read                         | 1st Cycle | L                | H→L              | H               | L               | Row         | Col.           | Data Out          |
|  | 2nd Cycle | L                | H→L              | H               | L               | N/A         | Col.           | Data Out          |
| EDO (Hyper Page) Mode Write                        | 1st Cycle | L                | H→L              | L               | X               | Row         | Col.           | Data In           |
|  | 2nd Cycle | L                | H→L              | L               | X               | N/A         | Col.           | Data In           |
| EDO (Hyper Page) Mode Read-Modify-Write            | 1st Cycle | L                | H→L              | H→L             | L→H             | Row         | Col.           | Data Out, Data In |
|  | 2nd Cycle | L                | H→L              | H→L             | L→H             | N/A         | Col.           | Data Out, Data In |
| $\overline{RAS}$ -Only Refresh                     |           | L                | H                | X               | X               | Row         | N/A            | High Impedance    |
| $\overline{CAS}$ -Before- $\overline{RAS}$ Refresh |           | H→L              | L                | H               | X               | X           | N/A            | High Impedance    |
| Hidden Refresh                                     | Read      | L→H→L            | L                | H               | L               | Row         | Col.           | Data Out          |
|  | Write     | L→H→L            | L                | L→H             | X               | Row         | Col.           | Data In           |
| Self Refresh (LP version only)                     |           | H→L              | L                | H               | X               | X           | X              | High Impedance    |



## Absolute Maximum Ratings

| Symbol    | Parameter                    | Rating                            | Units | Notes |
|-----------|------------------------------|-----------------------------------|-------|-------|
| $V_{CC}$  | Power Supply Voltage         | -0.5 to 4.6                       | V     | 1     |
| $V_{IN}$  | Input Voltage                | -0.5 to min ( $V_{CC}+0.5$ , 4.6) | V     | 1     |
| $V_{OUT}$ | Output Voltage               | -0.5 to min ( $V_{CC}+0.5$ , 4.6) | V     | 1     |
| $T_{OPR}$ | Operating Temperature        | 0 to +70                          | °C    | 1     |
| $T_{STG}$ | Storage Temperature          | -55 to +150                       | °C    | 1     |
| $P_D$     | Power Dissipation            | 1.0                               | W     | 1     |
| $I_{OUT}$ | Short Circuit Output Current | 50                                | mA    | 1     |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended DC Operating Conditions ( $T_A=0$ to $70^\circ\text{C}$ )

| Symbol   | Parameter          | Min. | Typ. | Max.           | Units | Notes |
|----------|--------------------|------|------|----------------|-------|-------|
| $V_{CC}$ | Supply Voltage     | 3.0  | 3.3  | 3.6            | V     | 1     |
| $V_{IH}$ | Input High Voltage | 2.0  | —    | $V_{CC} + 0.3$ | V     | 1,2   |
| $V_{IL}$ | Input Low Voltage  | -0.3 | —    | 0.8            | V     | 1,2   |

1. All voltages referenced to  $V_{SS}$ .  
 2.  $V_{IH}$  may overshoot to  $V_{CC} + 2.0\text{V}$  for pulse widths of  $\leq 4.0\text{ns}$  with 3.3 Volt.  $V_{IL}$  may undershoot to  $-2.0\text{V}$  for pulse widths  $\leq 4.0\text{ns}$  with 3.3 Volt. Pulse widths measured at 50% points with amplitude measured peak to DC reference

## Capacitance ( $T_A=0$ to $+70^\circ\text{C}$ , $V_{CC}=3.3 \pm 0.3\text{V}$ , $f=1\text{MHz}$ )

| Symbol   | Parameter  | Min. | Max. | Units |
|----------|--|------|------|-------|
| $C_{I1}$ | Input Capacitance (A0 - A11)   | —    | 5    | pF    |
| $C_{I2}$ | Input Capacitance ( $\overline{\text{RAS}}$ , $\text{CAS}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ ) | —    | 7    | pF    |
| $C_{I3}$ | Data I/O Capacitance (I/O0 - I/O3)   | —    | 7    | pF    |



**DC Electrical Characteristics** ( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.3 \pm 0.3\text{V}$ )

| Symbol     | Parameter   | Min.       | Max. | Units         | Notes         |         |
|------------|---|------------|------|---------------|---------------|---------|
| $I_{CC1}$  | Operating Current<br>Average Power Supply Operating Current<br>( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , Address Cycling: $t_{RC} = t_{RC \text{ min}}$ )   | -50        | —    | 140           | mA            | 1, 2, 3 |
|            |   | -60        | —    | 115           |               |         |
| $I_{CC2}$  | Standby Current (TTL)<br>Power Supply Standby Current<br>( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$ )   | —          | 2    | mA            |               |         |
| $I_{CC3}$  | $\overline{\text{RAS}}$ Only Refresh Current<br>Average Power Supply Current, $\overline{\text{RAS}}$ Only Mode<br>( $\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} = V_{IH}$ : $t_{RC} = t_{RC \text{ min}}$ )  | -50        | —    | 130           | mA            | 1, 3    |
|            |   | -60        | —    | 110           |               |         |
| $I_{CC4}$  | EDO (Hyper Page) Mode Current<br>Average Power Supply Current, Hyper Page Mode<br>( $\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{CAS}}$ , Address Cycling: $t_{PC} = t_{PC \text{ min}}$ )   | -50        | —    | 100           | mA            | 1, 2, 3 |
|            |   | -60        | —    | 80            |               |         |
| $I_{CC5}$  | Standby Current (CMOS)<br>Power Supply Standby Current<br>( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{CC} - 0.2\text{V}$ )  | LP version | —    | 200           | $\mu\text{A}$ |         |
|            |   | SP version | —    | 1             | mA            |         |
| $I_{CC6}$  | $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Current<br>Average Power Supply Current, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Mode<br>( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , Cycling: $t_{RC} = t_{RC \text{ min}}$ )   | -50        | —    | 140           | mA            | 1, 2    |
|            |   | -60        | —    | 115           |               |         |
| $I_{CC7}$  | Self Refresh Current (LP version only)<br>Average Power Supply Current during Self Refresh<br>CBR cycle with $\overline{\text{RAS}} \geq t_{RASS}$ (min); $\overline{\text{CAS}}$ held low;<br>$\overline{\text{WE}} = V_{CC} - 0.2\text{V}$ ; Addresses and $D_{IN} = V_{CC} - 0.2\text{V}$ or $0.2\text{V}$ . | —          | 400  | $\mu\text{A}$ |               |         |
| $I_{I(L)}$ | Input Leakage Current<br>Input Leakage Current, any input<br>( $0.0 \geq V_{IN} \geq V_{CC}$ ), All Other Pins Not Under Test = $0\text{V}$   | -2         | +2   | $\mu\text{A}$ |               |         |
| $I_{O(L)}$ | Output Leakage Current<br>( $D_{OUT}$ is disabled, $0.0 \geq V_{OUT} \geq V_{CC}$ )   | -2         | +2   | $\mu\text{A}$ |               |         |
| $V_{OH}$   | Output High Level (TTL)<br>Output "H" Level Voltage ( $I_{OUT} = -2\text{mA}$ )   | 2.4        | —    | V             |               |         |
| $V_{OL}$   | Output Low Level (TTL)<br>Output "L" Level Voltage ( $I_{OUT} = +2\text{mA}$ )  | —          | 0.4  | V             |               |         |

1.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ ,  $I_{CC6}$  depend on cycle rate.  
 2.  $I_{CC1}$ ,  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.  
 3. Column address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$  and  $\overline{\text{CAS}} = V_{IH}$ .



### AC Characteristics ( $T_A=0$ to $+70^\circ\text{C}$ , $V_{CC}=3.3 \pm 0.3\text{V}$ )

1. An initial pause of 100 $\mu\text{s}$  is required after power-up followed by 8  $\overline{\text{RAS}}$  only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycles instead of 8  $\overline{\text{RAS}}$  only refresh cycles is required.
2. AC measurements assume  $t_T=2\text{ns}$ .
3.  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
4. Valid column addresses are only A0 through A11.

### Read, Write, Read-Modify-Write and Refresh Cycle (Common Parameters)

| Symbol    | Parameter   | -50  |      | -60  |      | Units | Notes |
|-----------|---|------|------|------|------|-------|-------|
|           |   | Min. | Max. | Min. | Max. |       |       |
| $t_{RC}$  | Random Read or Write Cycle Time                                   | 84   | —    | 104  | —    | ns    | 1     |
| $t_{RP}$  | $\overline{\text{RAS}}$ Precharge Time                            | 30   | —    | 40   | —    | ns    |       |
| $t_{CP}$  | $\overline{\text{CAS}}$ Precharge Time                            | 8    | —    | 10   | —    | ns    |       |
| $t_{RAS}$ | $\overline{\text{RAS}}$ Pulse Width                               | 50   | 100k | 60   | 100k | ns    | 1     |
| $t_{CAS}$ | $\overline{\text{CAS}}$ Pulse Width                               | 8    | 100k | 10   | 100k | ns    | 1     |
| $t_{ASR}$ | Row Address Setup Time  | 0    | —    | 0    | —    | ns    |       |
| $t_{RAH}$ | Row Address Hold Time   | 7    | —    | 10   | —    | ns    |       |
| $t_{ASC}$ | Column Address Setup Time   | 0    | —    | 0    | —    | ns    |       |
| $t_{CAH}$ | Column Address Hold Time  | 7    | —    | 10   | —    | ns    |       |
| $t_{RCD}$ | $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time     | 11   | 37   | 14   | 45   | ns    | 2     |
| $t_{RAD}$ | $\overline{\text{RAS}}$ to Col. Address Delay Time                | 9    | 25   | 12   | 30   | ns    | 3     |
| $t_{RSH}$ | $\overline{\text{RAS}}$ Hold Time                                 | 8    | —    | 10   | —    | ns    |       |
| $t_{CSH}$ | $\overline{\text{CAS}}$ Hold Time                                 | 40   | —    | 50   | —    | ns    | 1     |
| $t_{CRP}$ | $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time | 5    | —    | 5    | —    | ns    | 1     |
| $t_{DZO}$ | $\overline{\text{OE}}$ Delay Time From $D_{IN}$                   | 0    | —    | 0    | —    | ns    | 5     |
| $t_{DZC}$ | $\overline{\text{CAS}}$ Delay Time From $D_{IN}$                  | 0    | —    | 0    | —    | ns    | 5     |
| $t_T$     | Transition Time (Rise and Fall)                                   | 1    | 50   | 1    | 50   | ns    | 6     |

1. In a Test Mode Read cycle, the value of  $t_{RAC}$ ,  $t_{AA}$ ,  $t_{CAC}$  and  $t_{CPA}$  are delayed by 5ns from the specified value. These parameters must be adjusted in Test Mode cycles by adding 5ns to the specified value. Associated timings must also be adjusted by 5ns.
2. Operation within the  $t_{RCD}(\text{max.})$  limit ensures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
3. Operation within the  $t_{RAD}(\text{max.})$  limit ensures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled by  $t_{AA}$ .
4. Either  $t_{ODD}$  or  $t_{ODD}$  must be satisfied.
5. Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.
6. AC measurements assume  $t_T = 2\text{ns}$ .

## Write Cycle

| Symbol    | Parameter                                   | -50  |      | -60  |      | Units | Notes |
|-----------|---|------|------|------|------|-------|-------|
|           |   | Min. | Max. | Min. | Max. |       |       |
| $t_{WCS}$ | Write Command Set Up Time                   | 0    | —    | 0    | —    | ns    | 1     |
| $t_{WCH}$ | Write Command Hold Time                     | 7    | —    | 10   | —    | ns    |       |
| $t_{WP}$  | Write Command Pulse Width                   | 7    | —    | 10   | —    | ns    |       |
| $t_{RWL}$ | Write Command to $\overline{RAS}$ Lead Time | 8    | —    | 10   | —    | ns    |       |
| $t_{CWL}$ | Write Command to $\overline{CAS}$ Lead Time | 8    | —    | 10   | —    | ns    |       |
| $t_{OED}$ | $\overline{OE}$ to $D_{IN}$ Delay Time      | 13   | —    | 15   | —    | ns    | 4     |
| $t_{DS}$  | $D_{IN}$ Setup Time                         | 0    | —    | 0    | —    | ns    | 3     |
| $t_{DH}$  | $D_{IN}$ Hold Time                          | 7    | —    | 10   | —    | ns    | 3     |

- $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$ ,  $t_{AWD} \geq t_{AWD}(\text{min.})$ , and  $t_{CPWD} \geq t_{CPWD}(\text{min.})$  (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
- Either  $t_{CDD}$  or  $t_{OED}$  must be satisfied.
- These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WE}$  leading edge in Read-Modify-Write cycles.



## Read Cycle

| Symbol    | Parameter   | -50  |      | -60  |      | Units | Notes      |
|-----------|---|------|------|------|------|-------|------------|
|           |   | Min. | Max. | Min. | Max. |       |            |
| $t_{RAC}$ | Access Time from $\overline{RAS}$                                     | —    | 50   | —    | 60   | ns    | 1, 2, 3, 5 |
| $t_{CAC}$ | Access Time from $\overline{CAS}$                                     | —    | 13   | —    | 15   | ns    | 1, 2, 5    |
| $t_{AA}$  | Access Time from Address  | —    | 25   | —    | 30   | ns    | 1, 2, 5    |
| $t_{OEA}$ | Access Time From $\overline{OE}$                                      | —    | 13   | —    | 15   | ns    | 1, 5       |
| $t_{RCS}$ | Read Command Setup Time   | 0    | —    | 0    | —    | ns    |            |
| $t_{RCH}$ | Read Command Hold Time to $\overline{CAS}$                            | 0    | —    | 0    | —    | ns    | 4          |
| $t_{RRH}$ | Read Command Hold Time to $\overline{RAS}$                            | 0    | —    | 0    | —    | ns    |            |
| $t_{RAL}$ | Column Address to $\overline{RAS}$ Lead Time                          | 25   | —    | 30   | —    | ns    | 1          |
| $t_{CLZ}$ | $\overline{CAS}$ to Output in Low-Z                                   | 0    | —    | 0    | —    | ns    | 5          |
| $t_{OEZ}$ | Output Buffer Turn-Off Delay From $\overline{OE}$                     | 0    | 13   | 0    | 15   | ns    | 7          |
| $t_{CDD}$ | $\overline{CAS}$ to $D_{IN}$ Delay Time                               | 13   | —    | 15   | —    | ns    | 4          |
| $t_{OFF}$ | Output Buffer Turn-Off Delay  | 0    | 13   | 0    | 15   | ns    | 7          |
| $t_{OES}$ | $\overline{OE}$ Setup Time Prior to $\overline{CAS}$                  | 5    | —    | 5    | —    | ns    |            |
| $t_{ORD}$ | $\overline{OE}$ Setup Time Prior to $\overline{RAS}$ (Hidden Refresh) | 0    | —    | 0    | —    | ns    |            |

1. In a Test Mode Read cycle, the value of  $t_{RAC}$ ,  $t_{AA}$ ,  $t_{CAC}$  and  $t_{CPA}$  are delayed by 5ns from the specified value. These parameters must be adjusted in Test Mode cycles by adding 5ns to the specified value. Associated timings must also be adjusted by 5ns.
2. Operation within the  $t_{RCD(max)}$  limit ensures that  $t_{RAC(max)}$  can be met.  $t_{RCD(max)}$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD(max)}$  limit, then access time is controlled by  $t_{CAC}$ .
3. Operation within the  $t_{RAD(max)}$  limit ensures that  $t_{RAC(max)}$  can be met.  $t_{RAD(max)}$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD(max)}$  limit, then access time is controlled by  $t_{AA}$ .
4. Either  $t_{CDD}$  or  $t_{OED}$  must be satisfied.
5. Measured with the specified current load and 100pF.
6. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
7.  $t_{OFF(max)}$  and  $t_{OEZ(max)}$  define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

## Read-Modify-Write Cycle

| Symbol    | Parameter                                      | -50  |      | -60  |      | Units | Notes |
|-----------|--|------|------|------|------|-------|-------|
|           |  | Min. | Max. | Min. | Max. |       |       |
| $t_{RWC}$ | Read-Modify-Write Cycle Time                   | 109  | —    | 135  | —    | ns    |       |
| $t_{RWD}$ | $\overline{RAS}$ to $\overline{WE}$ Delay Time | 65   | —    | 79   | —    | ns    | 1     |
| $t_{CWD}$ | $\overline{CAS}$ to $\overline{WE}$ Delay Time | 28   | —    | 34   | —    | ns    | 1     |
| $t_{AWD}$ | Column Address to $\overline{WE}$ Delay Time   | 40   | —    | 49   | —    | ns    | 1     |
| $t_{OEH}$ | $\overline{OE}$ Command Hold Time              | 7    | —    | 10   | —    | ns    |       |

1.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$ ,  $t_{AWD} \geq t_{AWD}(\text{min.})$ , and  $t_{CPWD} \geq t_{CPWD}(\text{min.})$  (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

## Extended Data Out (Hyper Page) Mode Cycle

| Symbol      | Parameter  | -50  |      | -60  |      | Units | Notes |
|-------------|--|------|------|------|------|-------|-------|
|             |  | Min. | Max. | Min. | Max. |       |       |
| $t_{HCAS}$  | $\overline{CAS}$ Pulse Width (Hyper Page Mode)                         | 8    | 100K | 10   | 10K  | ns    |       |
| $t_{HPC}$   | Hyper Page Mode Cycle Time (Read/Write)                                | 20   | —    | 25   | —    | ns    |       |
| $t_{HPRWC}$ | Hyper Page Mode Read Modify Write Cycle Time                           | 54   | —    | 66   | —    | ns    |       |
| $t_{DOH}$   | Data-out Hold Time from $\overline{CAS}$                               | 5    | —    | 5    | —    | ns    |       |
| $t_{WHZ}$   | Output buffer Turn-Off Delay from $\overline{WE}$                      | 0    | 10   | 0    | 10   | ns    |       |
| $t_{WPZ}$   | $\overline{WE}$ Pulse Width to Output Disable at $\overline{CAS}$ High | 7    | —    | 10   | —    | ns    |       |
| $t_{CPRH}$  | $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge             | 27   | —    | 35   | —    | ns    |       |
| $t_{CPA}$   | Access Time from $\overline{CAS}$ Precharge                            | —    | 27   | —    | 35   | ns    | 1     |
| $t_{RASP}$  | Hyper Page Mode $\overline{RAS}$ Pulse Width                           | 50   | 200K | 60   | 200K | ns    |       |
| $t_{OEP}$   | $\overline{OE}$ High Pulse Width                                       | 5    | —    | 10   | —    | ns    |       |
| $t_{OEHC}$  | $\overline{OE}$ High Hold Time from $\overline{CAS}$ High              | 5    | —    | 10   | —    | ns    |       |

1. Measured with the specified current load and 100pF at  $V_{OL} = 0.8V$  and  $V_{OH} = 2.0V$ .



## Self Refresh Cycle - Low Power Version Only

| Symbol     | Parameter                                       | -50  |      | -60  |      | Units   | Notes |
|------------|---|------|------|------|------|---------|-------|
|            |   | Min. | Max. | Min. | Max. |         |       |
| $t_{RASS}$ | RAS Pulse Width<br>During Self Refresh Cycle    | 100  | —    | 100  | —    | $\mu$ s | 1     |
| $t_{RPS}$  | RAS Precharge Time<br>During Self Refresh Cycle | 84   | —    | 104  | —    | ns      | 1     |
| $t_{CHS}$  | CAS Hold Time<br>During Self Refresh Cycle      | -50  | —    | -50  | —    | ns      | 1     |

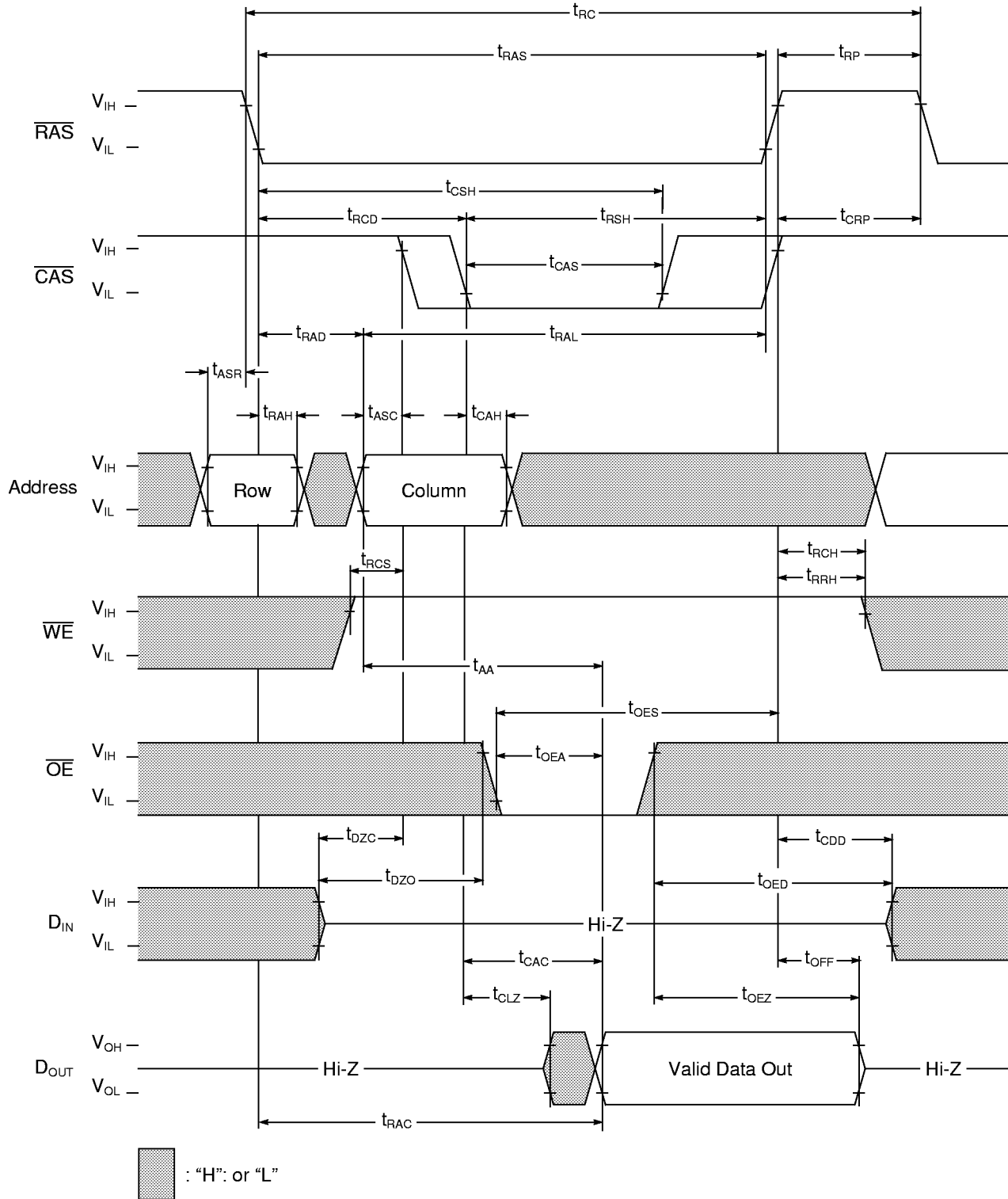
- When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:  
 If row addresses are being refreshed in an EVENLY DISTRIBUTED manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.  
 If row addresses are being refreshed in any other manner (ROR- Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.

## Refresh Cycle

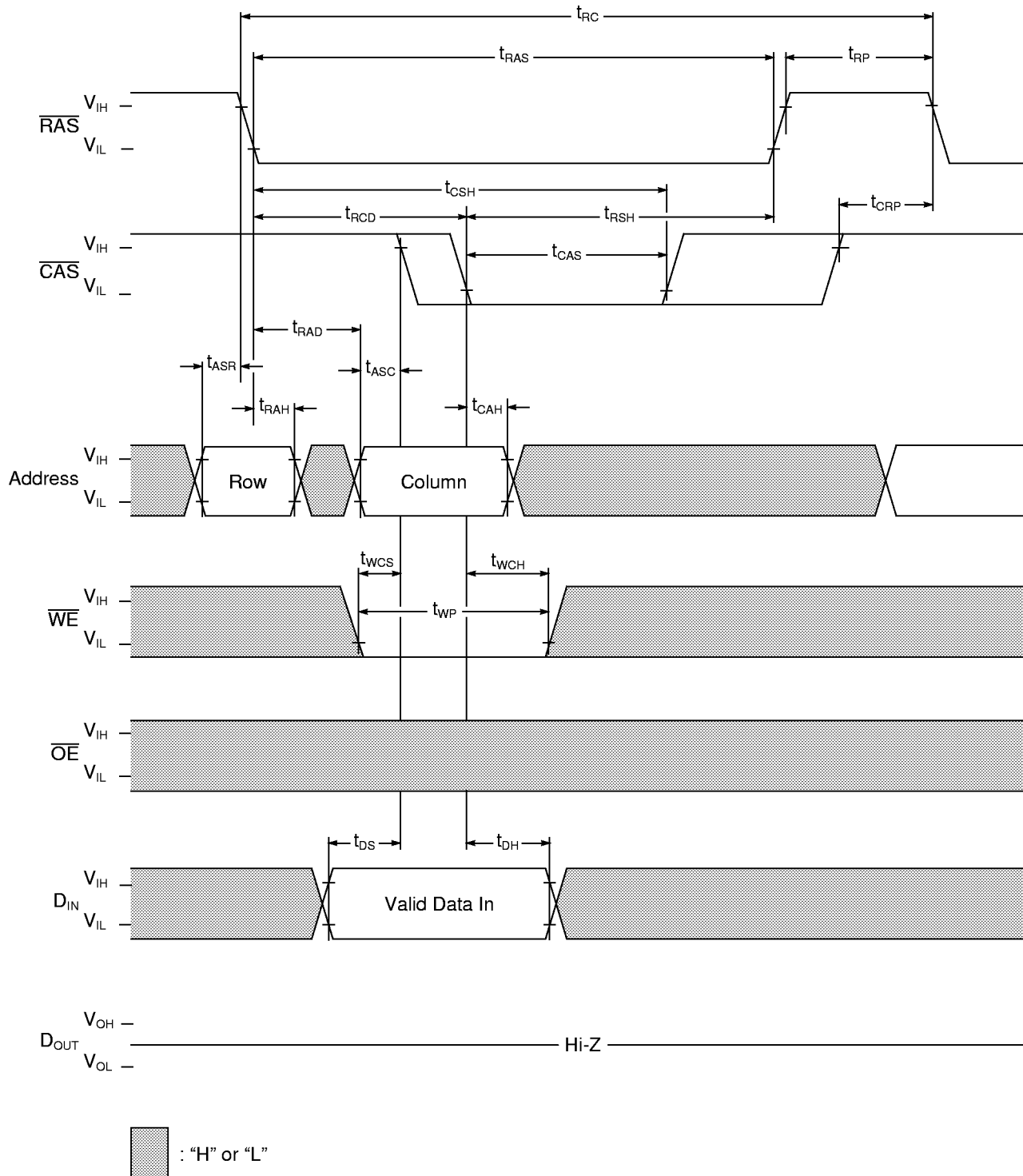
| Symbol    | Parameter  | -50        |      | -60  |      | Units | Notes |   |
|-----------|--|------------|------|------|------|-------|-------|---|
|           |  | Min.       | Max. | Min. | Max. |       |       |   |
| $t_{CSR}$ | CAS Setup Time<br>(CAS before RAS Refresh Cycle) | 5          | —    | 5    | —    | ns    |       |   |
| $t_{CHR}$ | CAS Hold Time<br>(CAS before RAS Refresh Cycle)  | 5          | —    | 10   | —    | ns    |       |   |
| $t_{WRP}$ | WE Setup Time<br>(CAS before RAS Refresh Cycle)  | 5          | —    | 10   | —    | ns    |       |   |
| $t_{WRH}$ | WE Hold Time<br>(CAS before RAS Refresh Cycle)   | 5          | —    | 10   | —    | ns    |       |   |
| $t_{RPC}$ | RAS Precharge to CAS Hold Time                   | 5          | —    | 5    | —    | ns    |       |   |
| $t_{REF}$ | Refresh Period                                   | SP version | —    | 64   | —    | 64    | ms    | 1 |
|           |  | LP version | —    | 256  | —    | 256   |       |   |

- 8192 cycles for RAS Only Refresh; 4096 cycles for CBR Refresh.

### Read Cycle

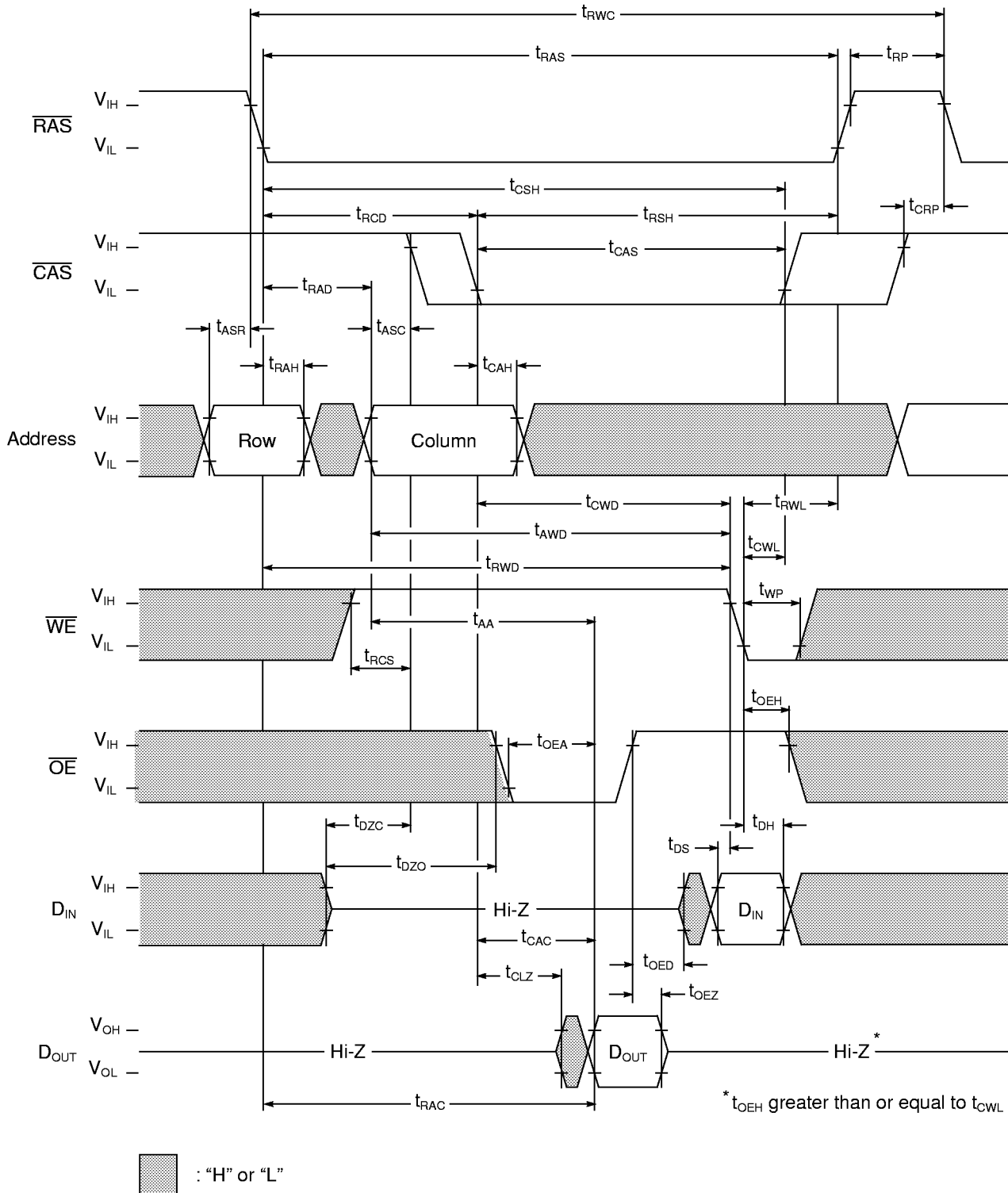


### Write Cycle (Early Write)

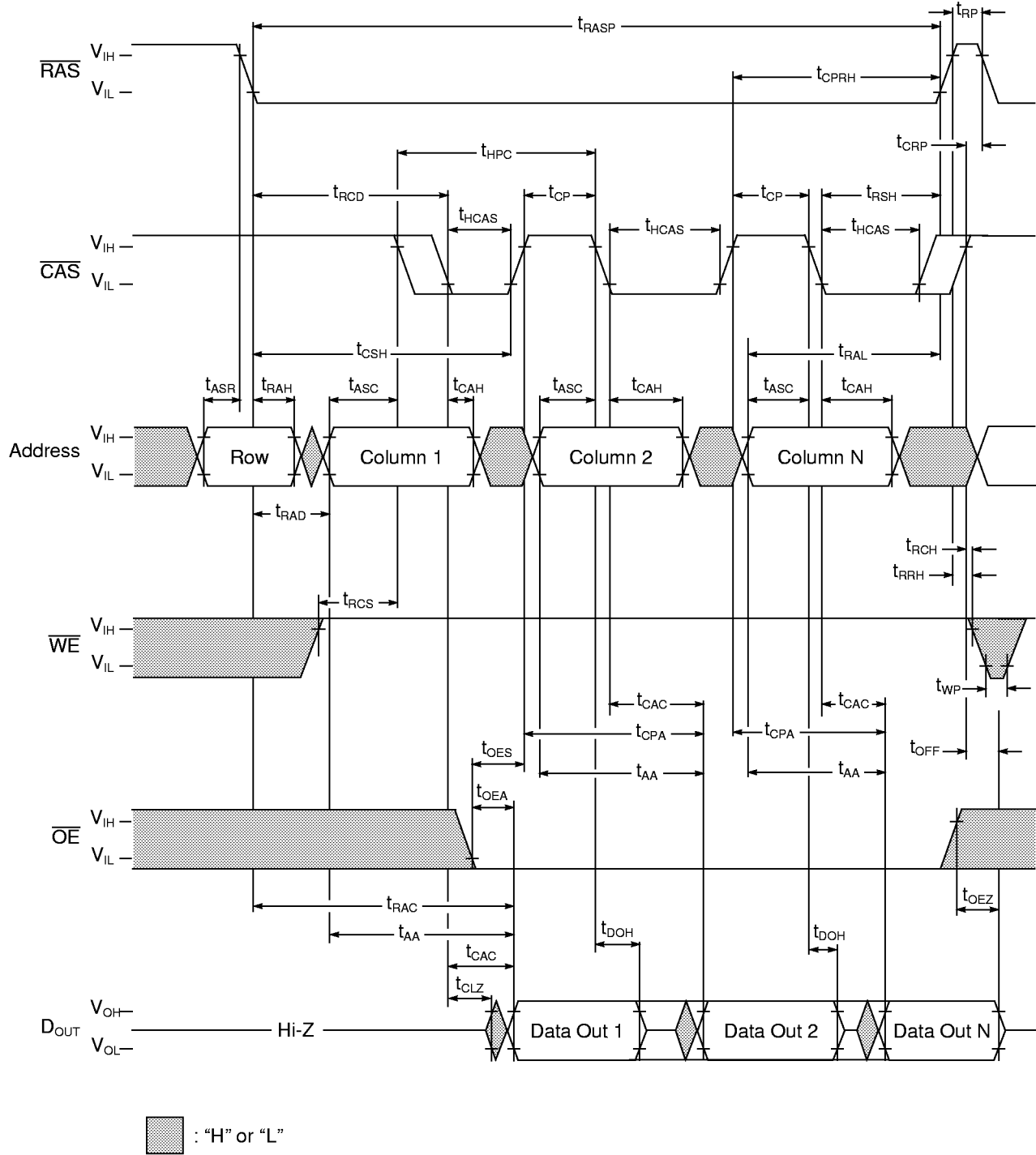




### Read-Modify-Write Cycle

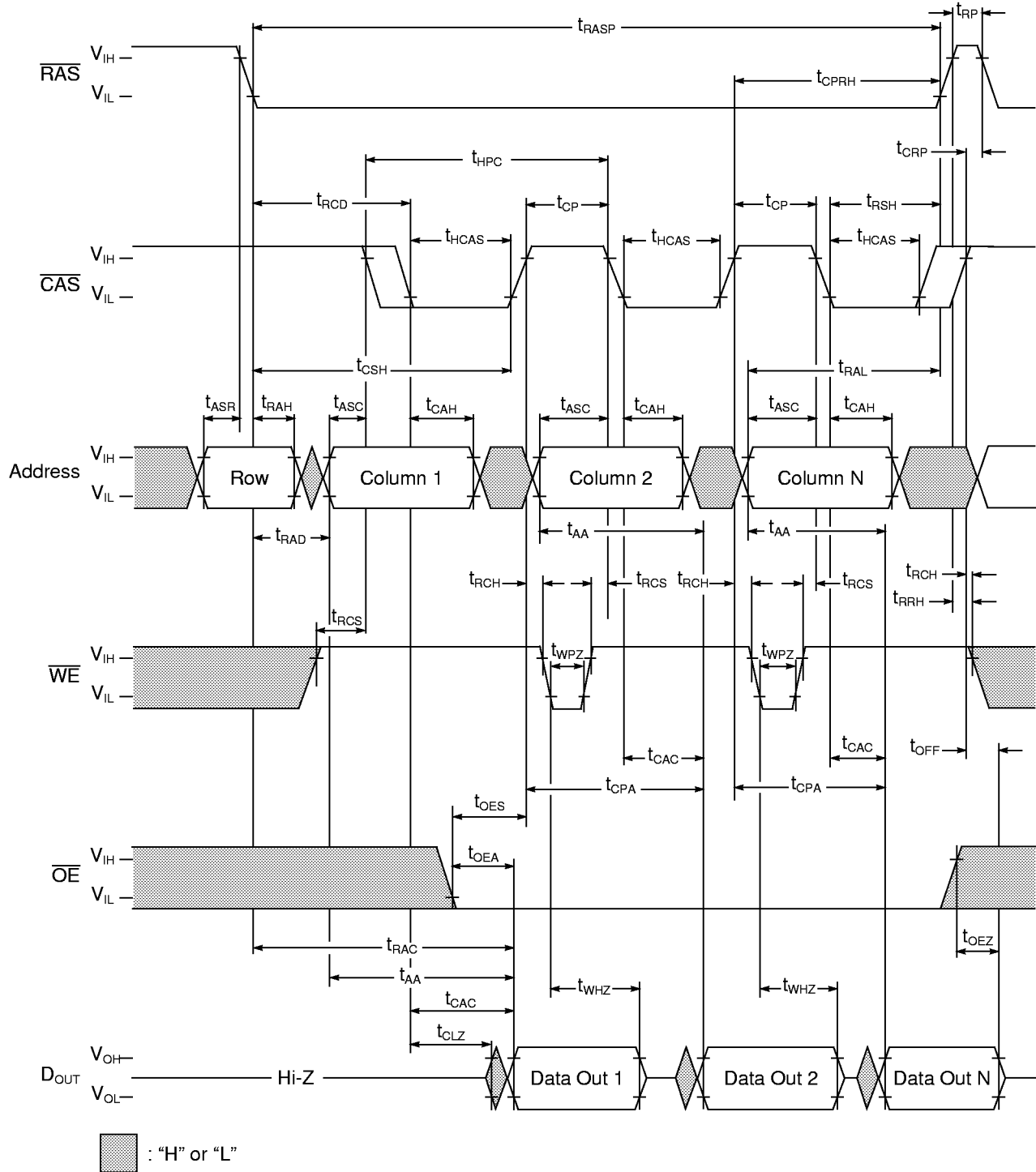


### EDO (Hyper Page) Mode Read Cycle

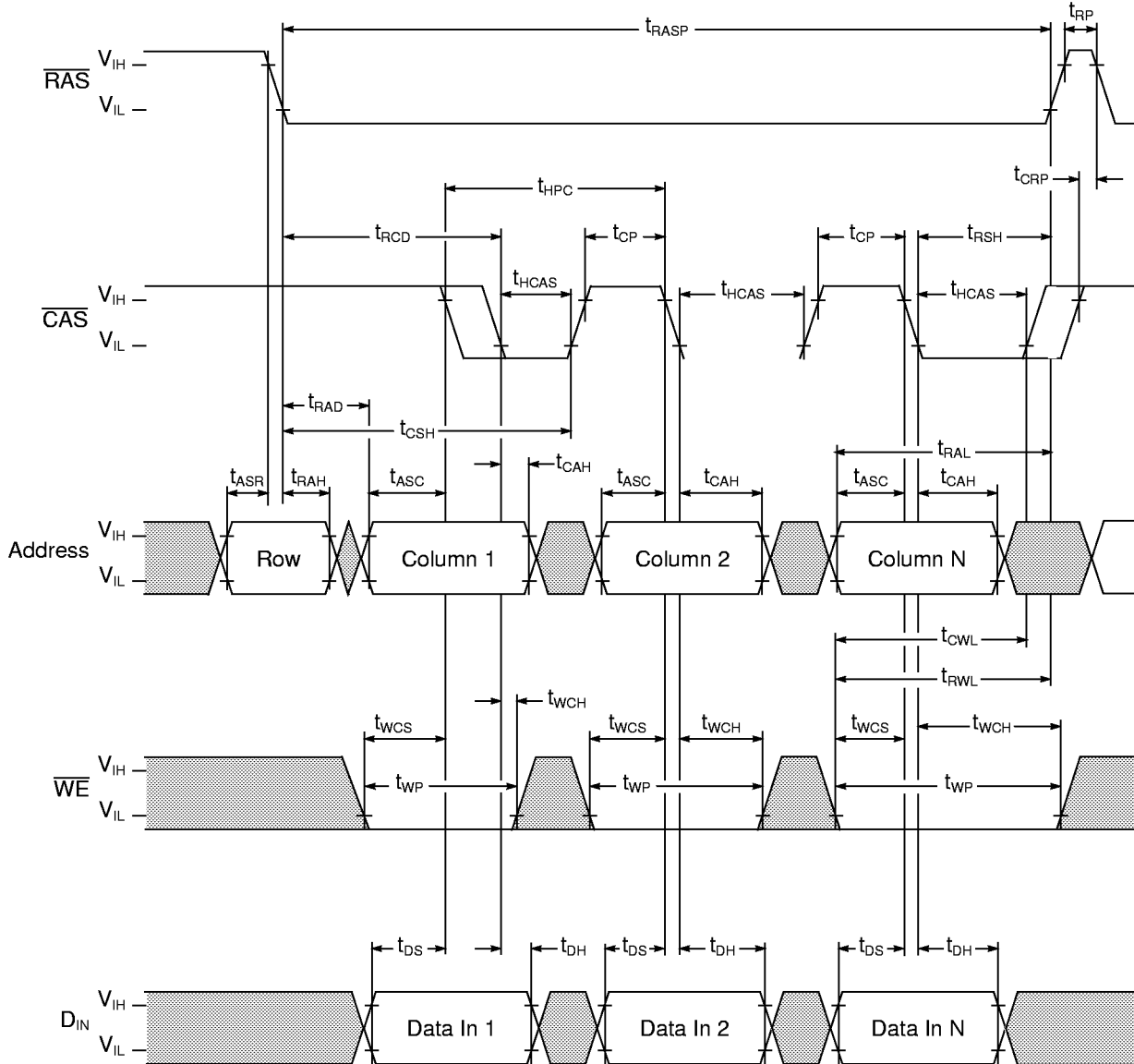




### EDO (Hyper Page) Mode Read Cycle ( $\overline{WE}$ Control)



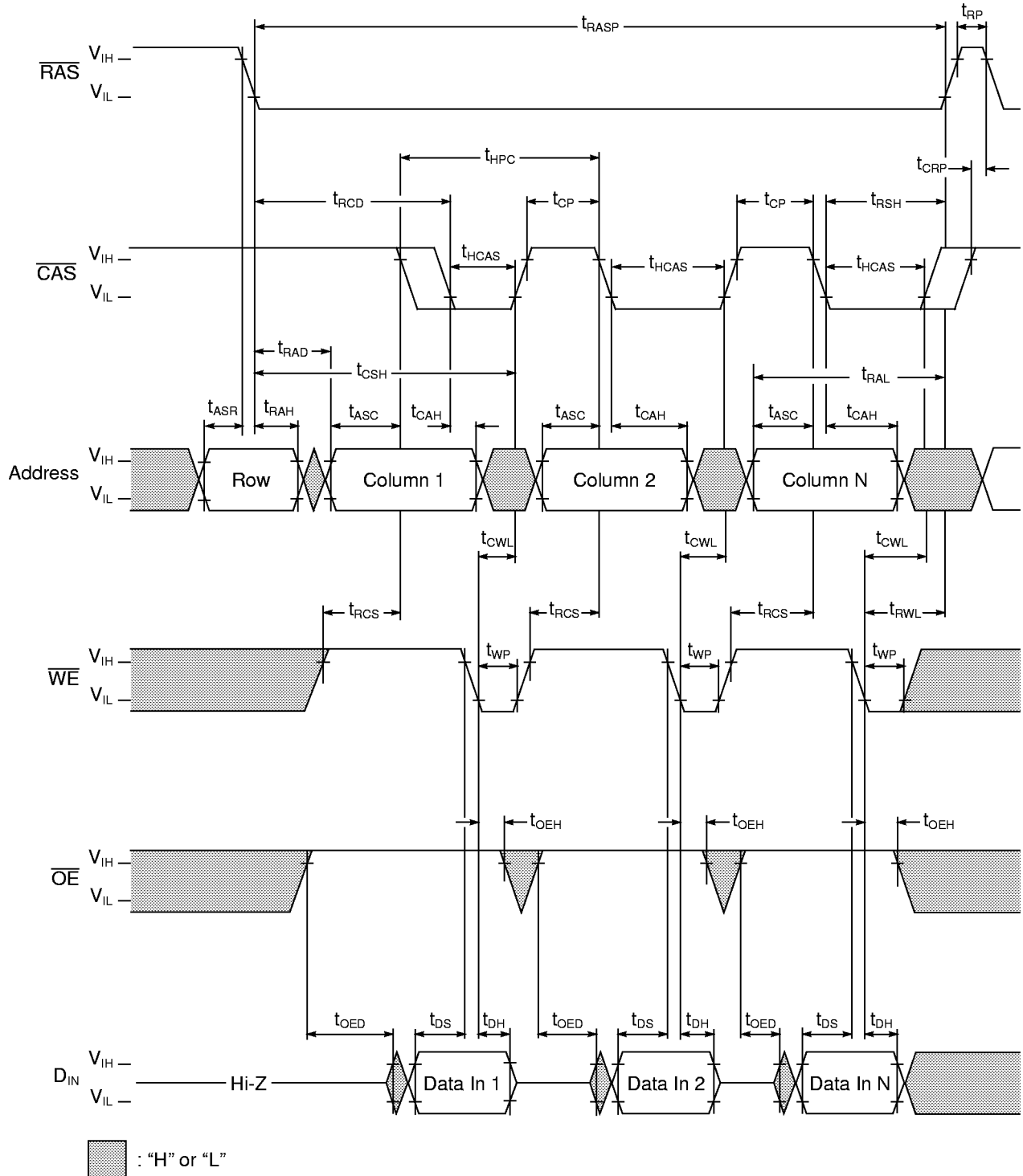
### EDO (Hyper Page) Mode Early Write Cycle



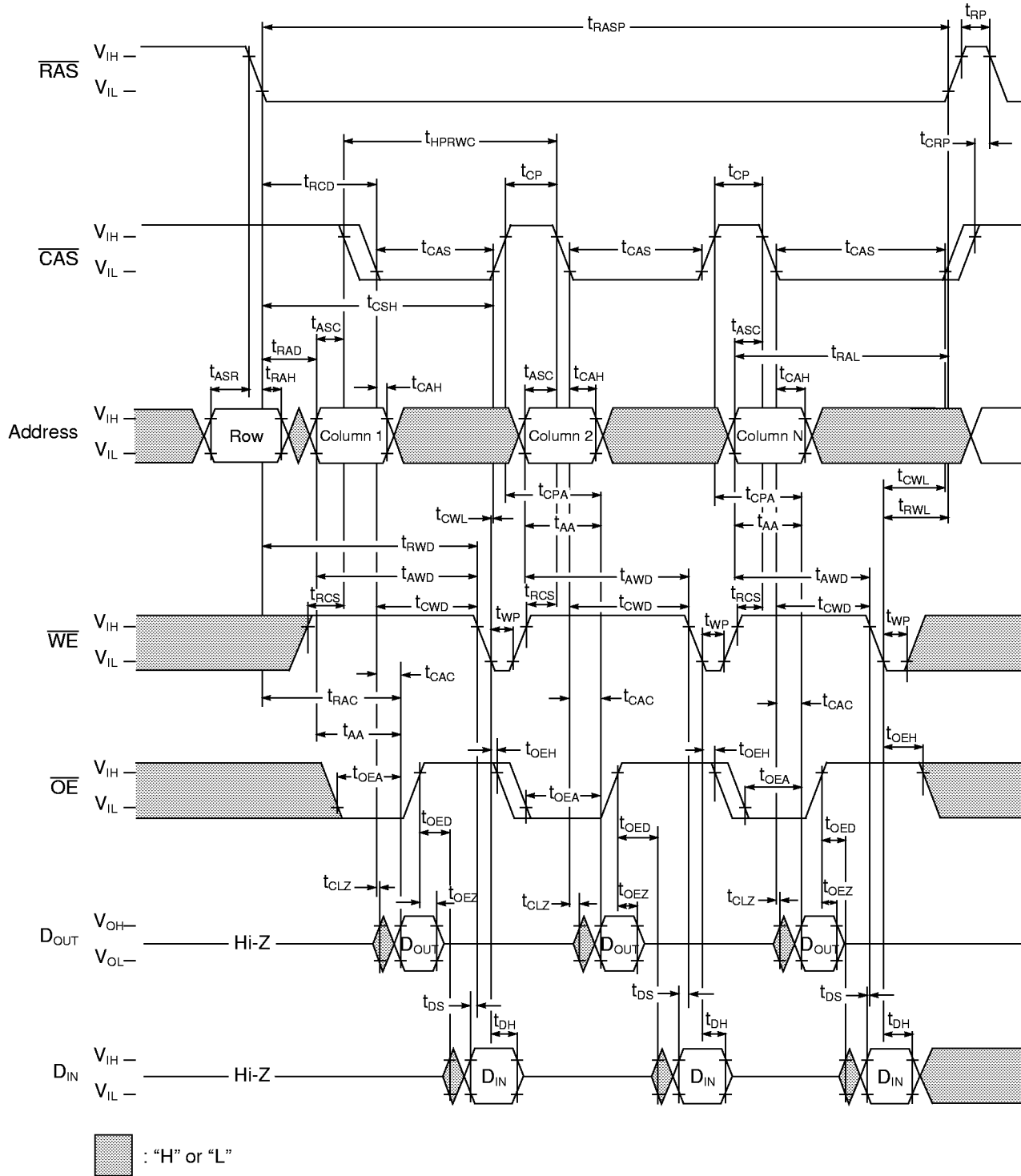
: "H" or "L"

$\overline{OE}$  = Don't care

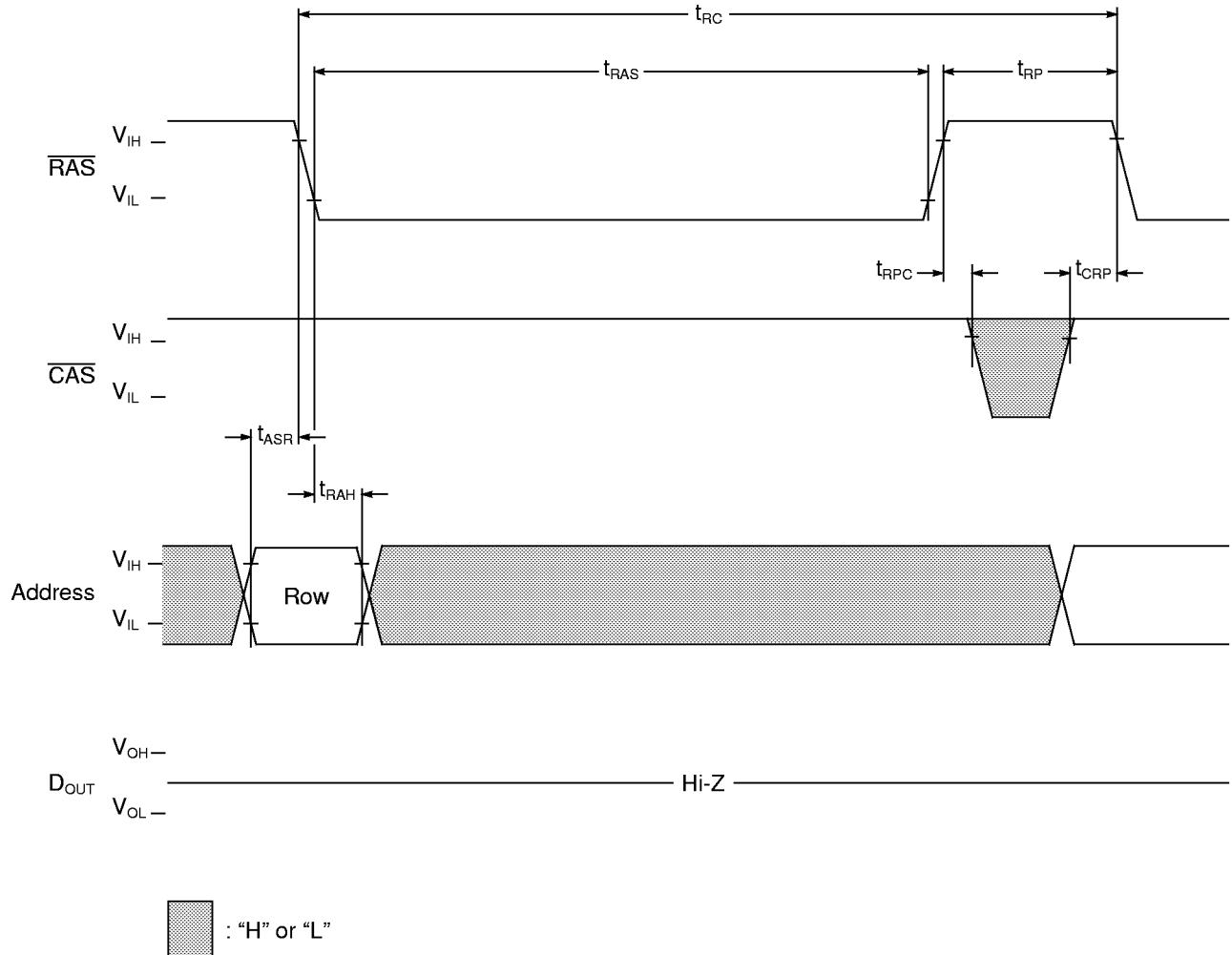
### EDO (Hyper Page) Mode Late Write Cycle



### EDO (Hyper Page) Mode Read Modify Write Cycle

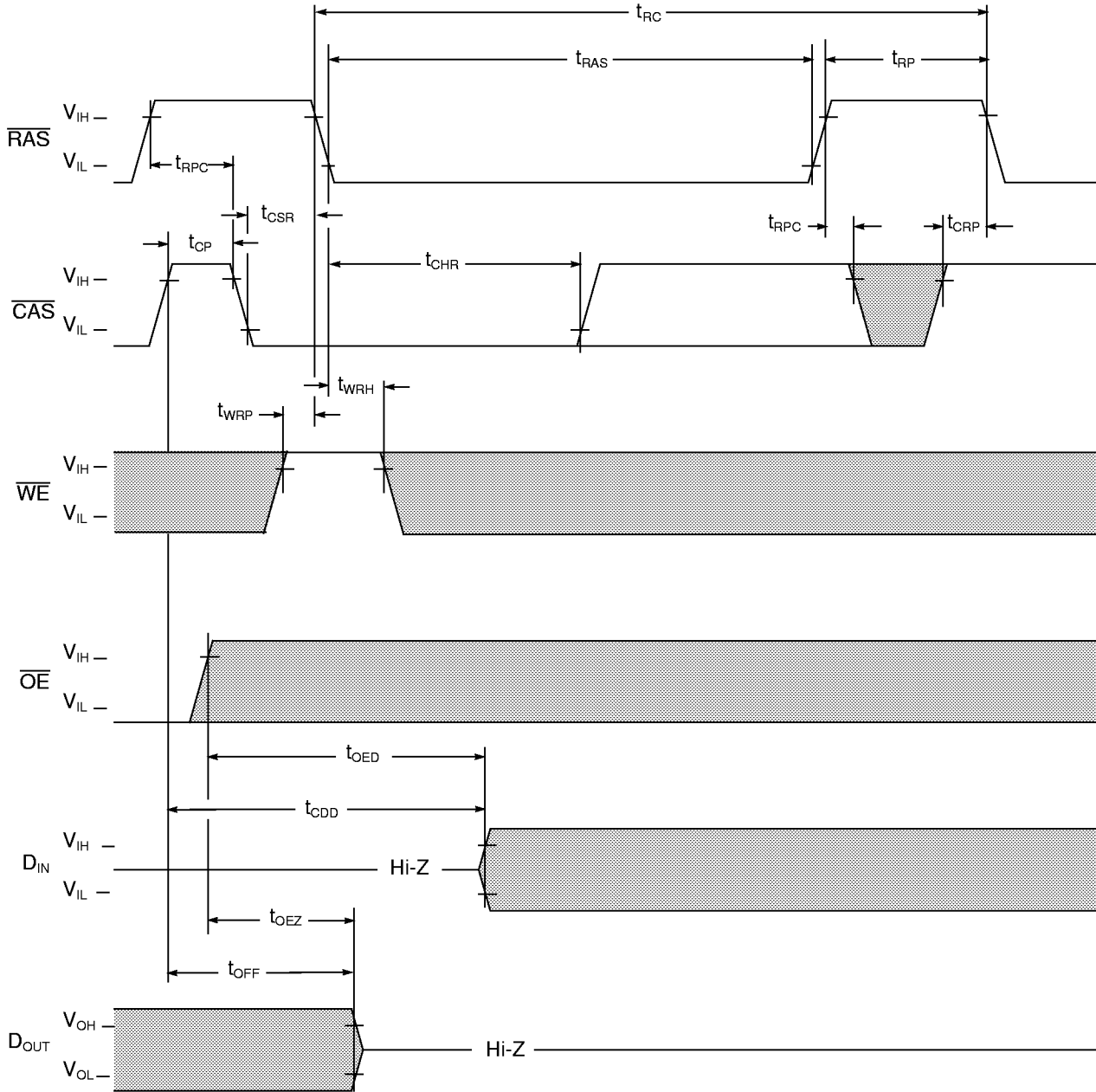


### RAS Only Refresh Cycle



NOTE:  $\overline{WE}$ ,  $\overline{OE}$  and  $D_{IN}$  are "H" or "L"

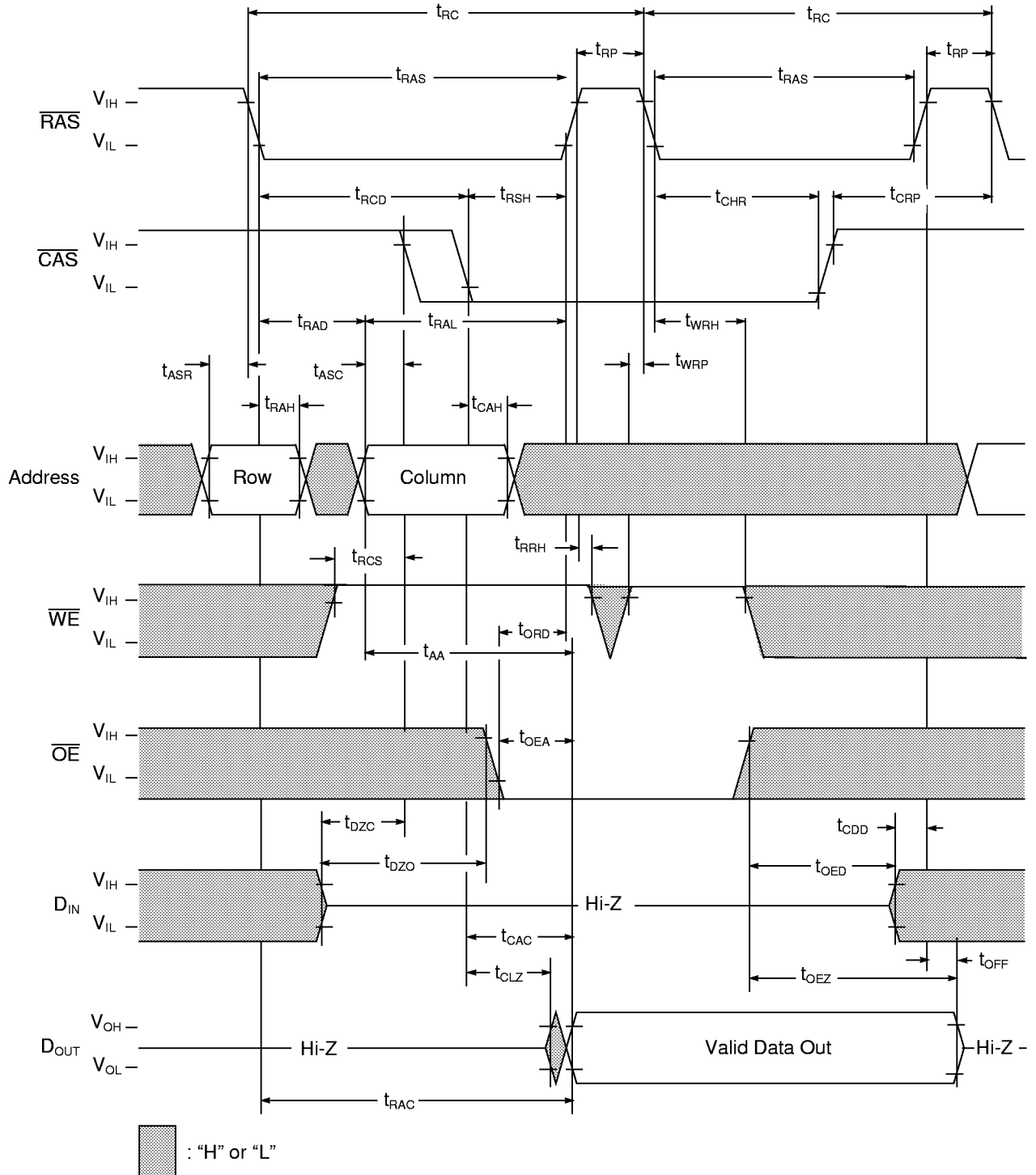
### CAS Before RAS Refresh Cycle



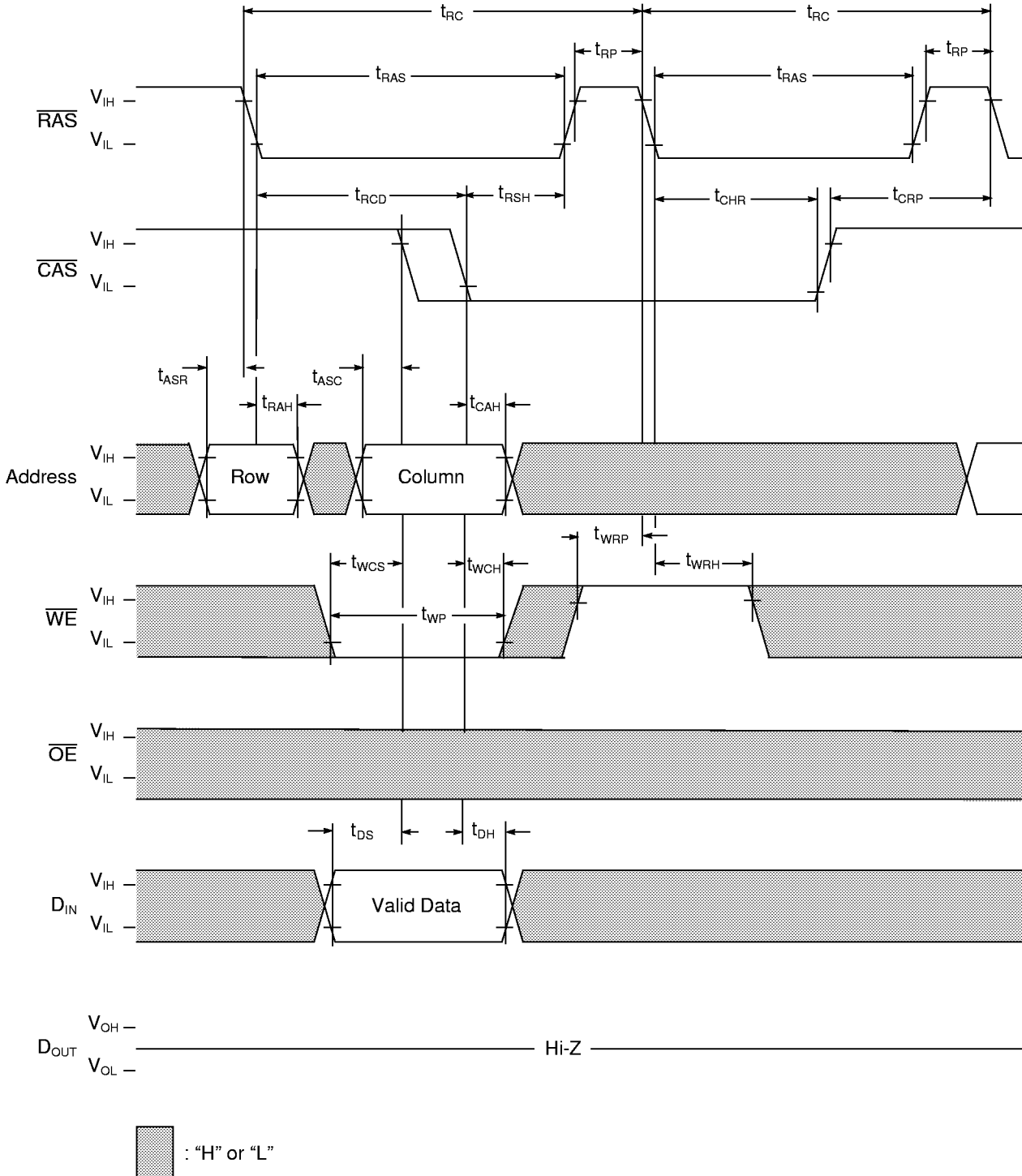
: "H" or "L"

NOTE: Address is "H" or "L"

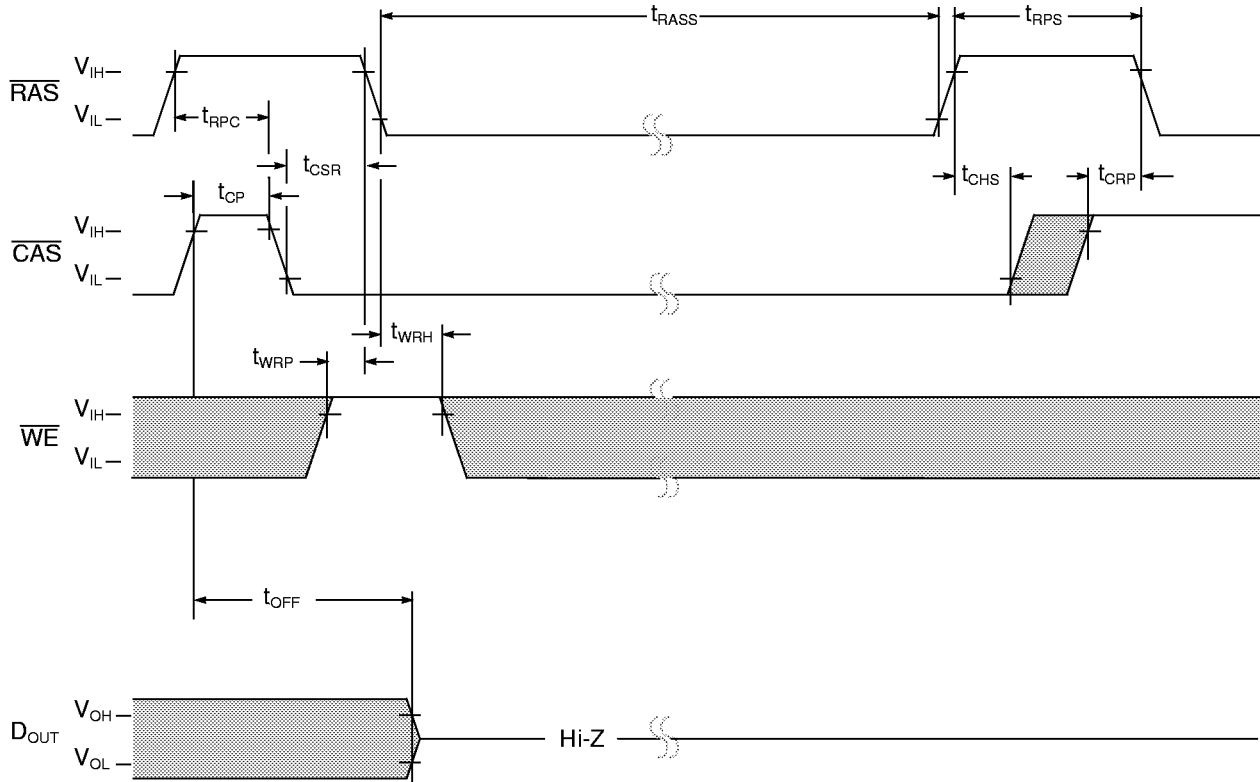
### Hidden Refresh Cycle (Read)



### Hidden Refresh Cycle (Write)



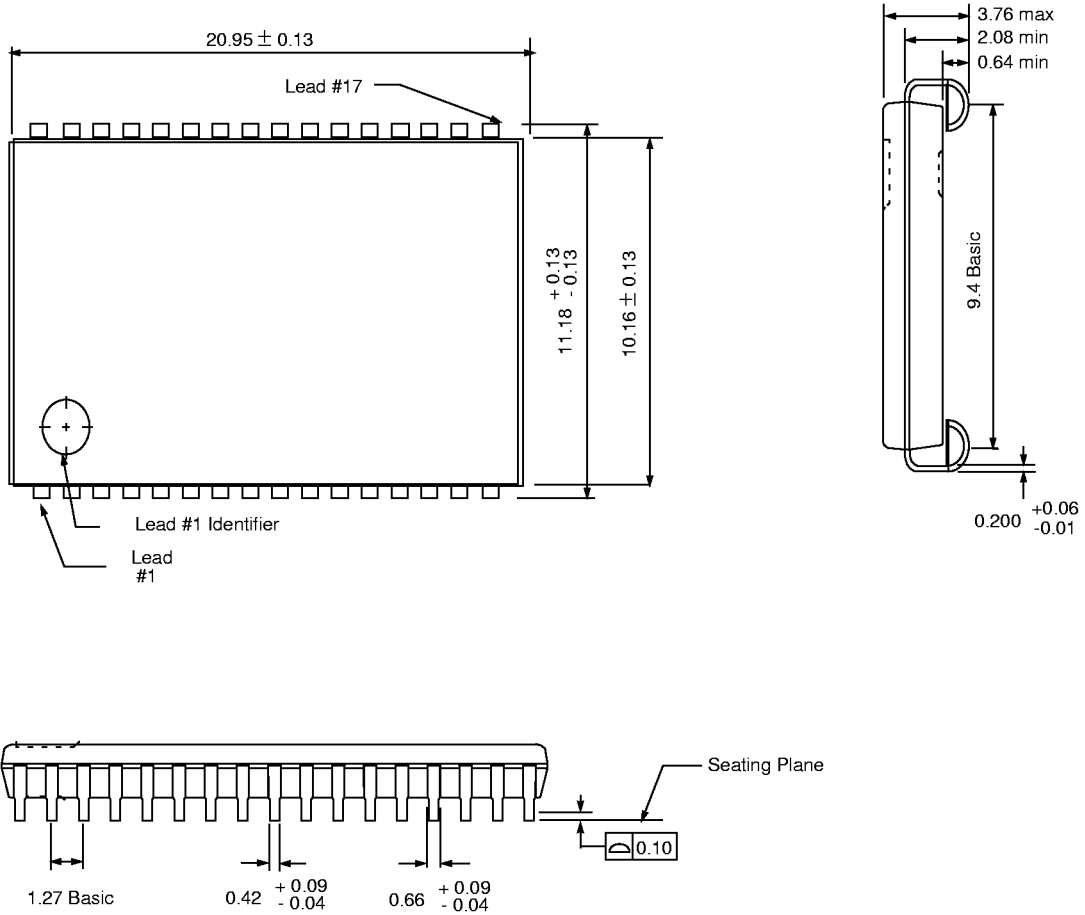
**Self Refresh Cycle (Sleep Mode) - Low Power version only**



: "H" or "L"

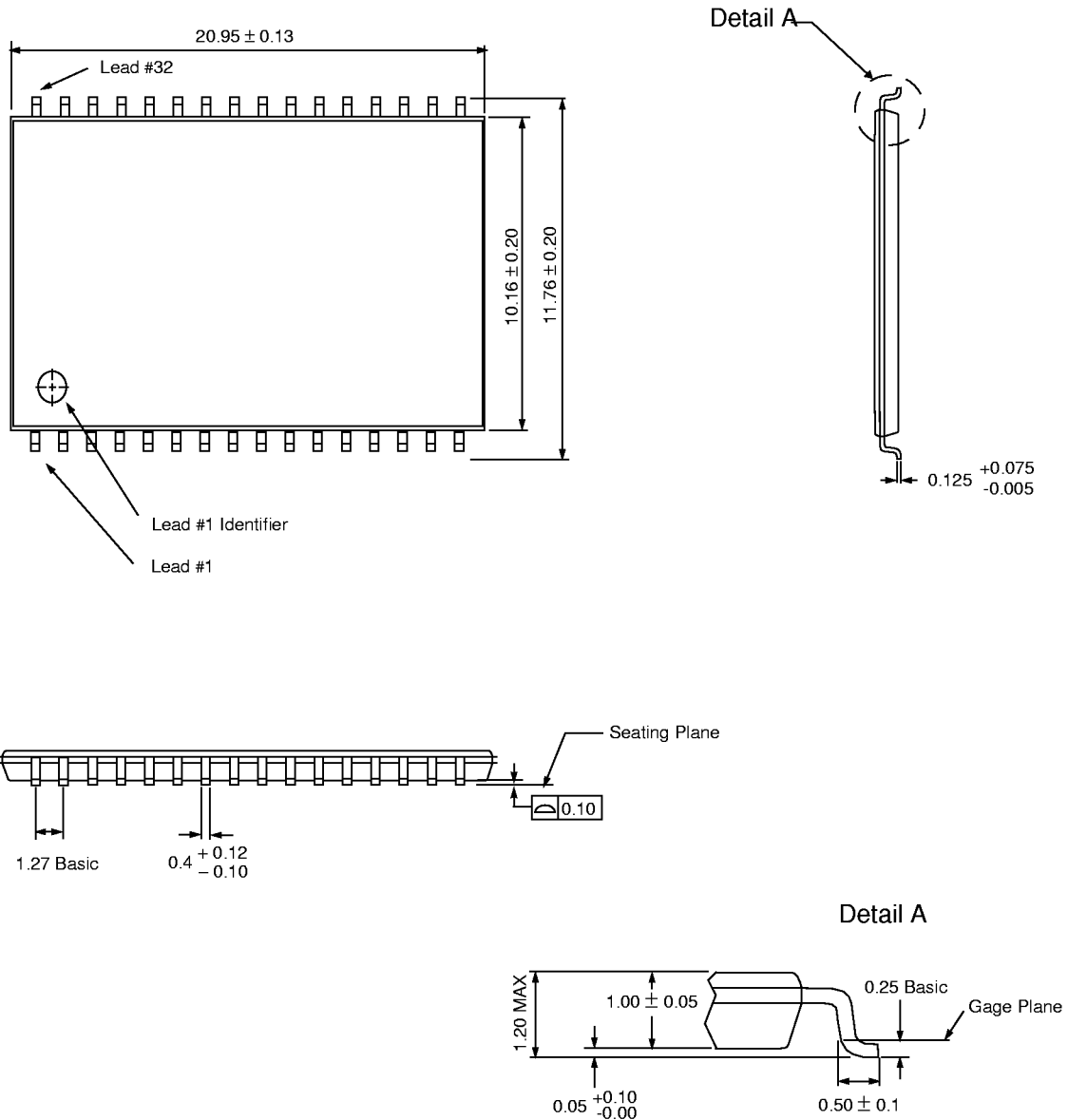
NOTE: Address and OE are "H" or "L"  
 Once  $t_{RASS}$  (min) is provided and RAS remains low, the DRAM will be in Self Refresh, commonly known as "Sleep Mode."

**Package Dimensions** (400 mil; 32 lead; Small Outline J-Lead)



**NOTE:** All dimensions are in millimeters. Reference JEDEC Standard MS-027

**Package Dimensions** (400 mil; 32 lead; Thin Small Outline Package)



**NOTE:** All dimensions are in millimeters. Reference JEDEC Standard MS-024



## Revision Log

| Revision | Contents of Modification   |
|----------|--|
| 1/2/97   | Initial specification release.   |
| 03/19/97 | <ol style="list-style-type: none"> <li>1. <math>\overline{WE}</math> for the Hidden Refresh Write cycle in the Truth Table was changed from "H" to "L→H".</li> <li>2. <math>t_{OED}</math> was moved from the Common Parameters table to the Write Cycle Parameters Table.</li> <li>3. The note "Implementing <math>\overline{WE}</math> at <math>\overline{RAS}</math> time during a Read or Write cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs." was removed from all of the Read and Write timing diagrams.</li> <li>4. <math>t_{ODD}</math> was changed to <math>t_{OED}</math> in notes in the Write Cycle and Read Cycle Parameters tables.</li> <li>5. "Hyper Page Mode" was changed to "EDO (Hyper Page) Mode" in the timing diagram titles.</li> <li>6. Removed the Test Mode parameters and timing diagrams.</li> <li>7. LVTTTL/LVCMOS changed to TTL/CMOS.</li> <li>8. LVCMOS currents were removed.</li> <li>9. Power numbers on the spec cover were recalculated.</li> </ol> |