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TMC216K/TMC217K

CMOS Multiplier

16 x 16 Bit, 35, 45, 60ns

The TRW TMC216K and TMC217K are high-speed 16 x 16 bit parallel multipliers which operate at minimum cycle times of 35, 45 and 60ns (28.6, 22.2 and 16.7MHz).

The individually clocked output registers of the TMC216K maximize system throughput and simplify interfacing. These registers are positive-edge-triggered D-type flip-flops.

The TMC217K has a single clock input and makes use of three register enables which control the X and Y input registers and the Most Significant Product (MSP) and Least Significant Product (LSP) output registers. This allows the TMC217K to excel in microprogrammed systems.

In both devices, the LSP shares a bidirectional port with the Y input and is also available multiplexed at the MSP output. All outputs are three-state.

The TMC216K is pin and function compatible with the TRW TMC216H and MPY016K. The TMC217K is pin and function compatible with the LMU17/217, IDT7217 and AM29517.

Features

- Fully TTL Compatible
- 35, 45, 60ns Multiply Times (Worst Case)
- Low Power CMOS Technology
- Single +5V Power Supply
- Output Registers Can Be Made Transparent
- Three-State Outputs
- Two's Complement, Unsigned Magnitude, Or Mixed Mode Multiplication
- Available In 68 Pin Grid Array And 68 Lead Plastic J-Leaded Chip Carriers
- Available In Commercial And MIL-STD-883C Grades

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

TRW LSI Products Inc.
P.O. Box 2472
La Jolla, CA 92038

Phone: (619) 457-1000
FAX: (619) 455-6314

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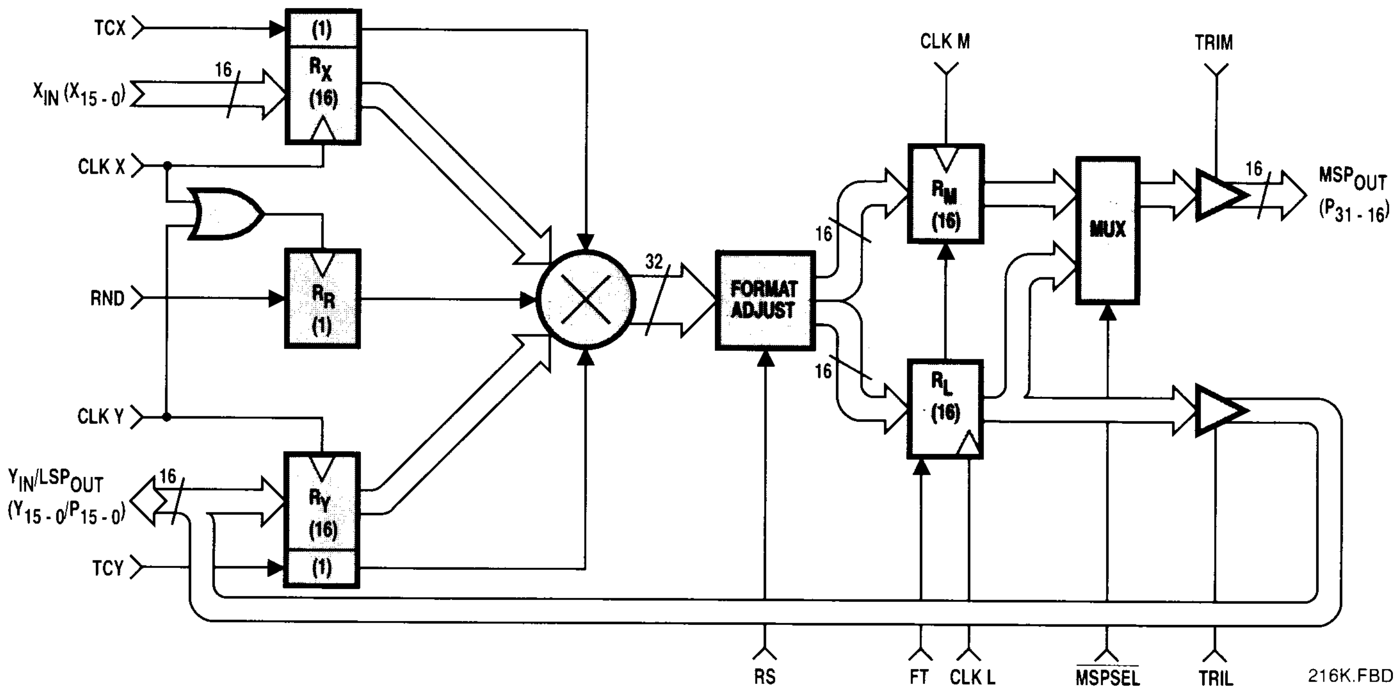
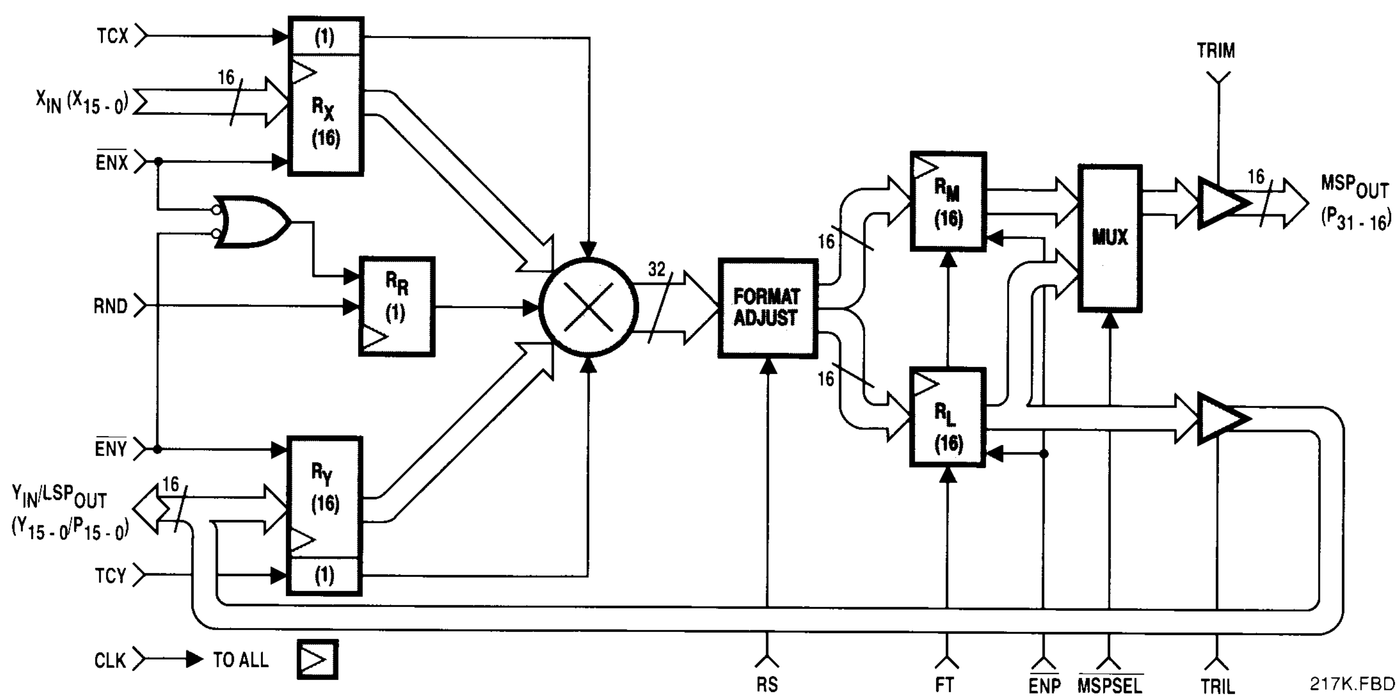
TMC216K Functional Block Diagram



TMC217K Functional Block Diagram



Functional Description

General Information

The TMC216K/TMC217K have three functional sections: input registers, an asynchronous multiplier array, and output registers. The input registers store the two 16-bit numbers which are to be multiplied and the instruction which controls the output rounding. The rounding control is used when a single-word output is desired. Each input operand is stored independently, simplifying multiplication by a constant. The asynchronous multiplier array is a network of AND gates and adders, designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 16-bit words, the Most Significant Product (MSP) and the Least Significant Product (LSP). Three-state output drivers allow the TMC216K/TMC217K to be used on a bus, or allow the Y input, least and most significant outputs to be multiplexed over the same 16-bit input/output lines. The Least Significant Product (LSP) is multiplexed with the Y input.

Power

The TMC216K/TMC217K operate from a single +5 Volt supply. All power and ground lines must be connected. Note that the TMC216K is pin and function compatible with the MPY016K.

Data Inputs

The TMC216K/TMC217K have two 16-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{15} and Y_{15}, carry the sign information for the two's complement notation. The remaining bits are denoted X_0 through X_{14} and Y_0 through Y_{14} (with X_0 and Y_0 the Least Significant Bits). The input and output formats for fractional two's complement, fractional unsigned magnitude, fractional mixed mode, integer two's complement, integer unsigned magnitude, and integer mixed mode notation are shown in *Figures 1 through 6*, respectively. The Y inputs are multiplexed with the LSP outputs, and hence can only be used when the TRIL control is in a HIGH state.

Data Outputs

The TMC216K/TMC217K have a 32-bit two's complement or unsigned magnitude output which is the product of the two input data values. This output is divided into two 16-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP). The Most Significant Bit (MSB) of both the MSP and the LSP is the sign bit if fractional two's complement notation is used (TCX=TCY=1, RS=0). The input and output formats for fractional two's complement, fractional unsigned magnitude, fractional mixed mode, integer two's complement, integer unsigned magnitude, and integer mixed mode notation are shown in *Figures 1 through 6*, respectively.

The LSP output can be taken from the Y input pins only when TRIL is LOW. Care must be taken to enable these shared input lines only at the proper time. For an output from the MSP lines to be read, the TRIM control must be LOW.

When $\overline{\text{MSPSEL}}$ is HIGH the LSP is available at the dedicated pins which provide the MSP when $\overline{\text{MSPSEL}}$ is LOW.

RS is an output format control. A HIGH on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, or integer two's complement operation.

Clocks

The TMC216K has four clock lines, one for each input register and one for each product register. Data and format controls present at the inputs of the registers are loaded into the registers on the rising edge of the appropriate clock.

The RND input of the TMC216K is registered on the rising edge of the logical OR of CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. TRW recommends the use of normally LOW clocks.

The TMC217K will load all enabled registers on the rising edge of its single clock (CLK).

The RND input of the TMC217K is registered on the rising edge of CLK if and only if the logical NAND of $\overline{\text{ENY}}$ and $\overline{\text{ENX}}$ is HIGH.

Controls

The TMC216K and TMC217K both have these seven control lines:

FT: Feedthrough. A control line which makes the output register transparent if it is HIGH.

$\overline{\text{MSPSEL}}$: Output Multiplexer Control. When this control is LOW, the MSP is available for output at the dedicated output port, and the LSP is available at the Y-input/LSP output port. (Identical function to TMC216H and MPY016H.) When $\overline{\text{MSPSEL}}$ is HIGH, the LSP is available at both ports, and the MSP is not available.

TRIM, TRIL: Three-state enable lines for the MSP and the LSP. The output driver is in the high-impedance state when TRIM or TRIL is HIGH, and enabled when the appropriate control is LOW. TRIM is equivalent to $\overline{\text{OEP}}$ and TRIL is equivalent to $\overline{\text{OEL}}$ on other devices.

RS: Register Shift. RS is an output format control. A HIGH level on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, and two's complement integer operations. RS is also called $\overline{\text{FA}}$ on similar devices.

RND: Round. When RND is HIGH, a one is added to the MSB of the LSP. Note that this bit depends on the state of the RS control. If RS is LOW when RND is HIGH, a one will be added to the 2^{-16} bit (P_{14}). If RS is HIGH when RND is HIGH, a one will be added to the 2^{-15} bit (P_{15}). In either case, the LSP output will reflect this addition when RND is HIGH. Note also that rounding always occurs in the positive direction; in some systems this may introduce a systematic bias.

TCX, TCY: Control how the device interprets data on the X and Y inputs. A HIGH on TCX or TCY forces the TMC216H to consider the appropriate input as a two's complement number, while a LOW forces the TMC216H to consider the appropriate input as a magnitude only number. TCX and TCY are called X_M and Y_M on similar devices.

FT, RS, TRIM, and TRIL are not registered. The TCX input is registered, and clocked in at the rising edge of the X clock signal, CLK X. The TCY input is also registered, and clocked in at the rising edge of the Y clock signal, CLK Y. The RND input is registered, and clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading these control signals can be avoided by the use of normally LOW clocks.

The TMC217K has three additional control lines:

$\overline{\text{ENX}}$: X-Register Enable. When $\overline{\text{ENX}}$ is LOW, the X-register is enabled; X-input data and TCX will be latched on the rising edge of CLK. When $\overline{\text{ENX}}$ is HIGH, the X-register value is unchanged.

$\overline{\text{ENY}}$: Y-Register Enable. When $\overline{\text{ENY}}$ is LOW, the Y-register is enabled; Y-input data and TCY will be latched on the rising edge of CLK. When $\overline{\text{ENY}}$ is HIGH, the Y-register value is unchanged.

$\overline{\text{ENP}}$: Product Register Enable. When $\overline{\text{ENP}}$ is LOW, both MSP and LSP product registers are enabled and data from the format adjust section of the multiplier will be loaded on the rising edge of CLK. When $\overline{\text{ENP}}$ is HIGH, the product register values are unchanged.

Package Interconnections

Signal Type	Signal Name	Function	Value	G8, H8 Package Pins	R1 Package Pins
Power	V_{DD}	Positive Supply Voltage	+5.0V	F10, G11	1, 68
	GND	Ground	0.0V	H11, G10	2, 3
Data Inputs	X_{15}	X Data MSB	TTL	D11	63
	X_{14}		TTL	C10	62
	X_{13}		TTL	C11	61
	X_{12}		TTL	B10	59
	X_{11}		TTL	A10	58
	X_{10}		TTL	B10	57
	X_9		TTL	B9	56
	X_8		TTL	B8	55
	X_7		TTL	A8	54
	X_6		TTL	B7	53
	X_5		TTL	A7	52
	X_4		TTL	B6	51
	X_3		TTL	A6	50
	X_2		TTL	B5	49
	X_1		TTL	A5	48
	X_0	X Data LSB	TTL	B4	47
	Y_{15}	Y Data MSB	TTL	J1	27
	Y_{14}		TTL	J2	28
	Y_{13}		TTL	H1	29
	Y_{12}		TTL	H2	30
	Y_{11}		TTL	G1	31
	Y_{10}		TTL	G2	32
	Y_9		TTL	F1	33
	Y_8		TTL	F2	34
	Y_7		TTL	E1	35
	Y_6		TTL	E2	36
	Y_5		TTL	D1	37
	Y_4		TTL	D2	38
	Y_3		TTL	C1	39
	Y_2		TTL	C2	40
	Y_1		TTL	B1	41
	Y_0	Y Data LSB	TTL	B2	42
Clocks	CLK X	Clock, Data Input X (TMC216K)	TTL	D10	64
	CLK Y	Clock, Data Input Y (TMC216K)	TTL	A3	44
	CLK L	Clock, LSP Register (TMC216K)	TTL	B3	45
	CLK M	Clock, MSP Register (TMC216K)	TTL	K10	8
	CLK	Clock (TMC217K)	TTL	B3	45

Package Interconnections (cont.)

Signal Type	Signal Name	Function	Value	G8, H8 Package Pins[1,2]	R1 Package Pins[1,2]
Data Outputs	P_{31}	Product MSB, MSP MSB	TTL	L9 (N/A)	10 (N/A)
	P_{30}		TTL	K9 (N/A)	11 (N/A)
	P_{29}		TTL	L8 (N/A)	12 (N/A)
	P_{28}		TTL	K8 (N/A)	13 (N/A)
	P_{27}		TTL	L7 (N/A)	14 (N/A)
	P_{26}		TTL	K7 (N/A)	15 (N/A)
	P_{25}		TTL	L6 (N/A)	16 (N/A)
	P_{24}		TTL	K6 (N/A)	17 (N/A)
	P_{23}		TTL	L5 (N/A)	18 (N/A)
	P_{22}		TTL	K5 (N/A)	19 (N/A)
	P_{21}		TTL	L4 (N/A)	20 (N/A)
	P_{20}		TTL	K4 (N/A)	21 (N/A)
	P_{19}		TTL	L3 (N/A)	22 (N/A)
	P_{18}		TTL	K3 (N/A)	23 (N/A)
	P_{17}		TTL	L3 (N/A)	24 (N/A)
	P_{16}	MSP LSB	TTL	K2 (N/A)	25 (N/A)
	P_{15}	LSP MSB	TTL	J1 (L9)	27 (10)
	P_{14}		TTL	J2 (K9)	28 (11)
	P_{13}		TTL	H1 (L8)	29 (12)
	P_{12}		TTL	H2 (K8)	30 (13)
	P_{11}		TTL	G1 (L7)	31 (14)
	P_{10}		TTL	G2 (K7)	32 (15)
	P_9		TTL	F1 (L6)	33 (16)
	P_8		TTL	F2 (K6)	34 (17)
	P_7		TTL	E1 (L5)	35 (18)
	P_6		TTL	E2 (K5)	36 (19)
	P_5		TTL	D1 (L4)	37 (20)
	P_4		TTL	D2 (K4)	38 (21)
	P_3		TTL	C1 (L3)	39 (22)
	P_2		TTL	C2 (K3)	40 (23)
	P_1		TTL	B1 (L2)	41 (24)
	P_0	Product LSB, LSP LSB	TTL	B2 (K2)	42 (25)
Controls	RND	Round Control	TTL	E11	65
	TCX	X Input Two's Complement (X_M)	TTL	E10	66
	TCY	Y Input Two's Complement (Y_M)	TTL	F11	67
	FT	Output Register Feedthrough (FA Or $\overline{\text{FA}}$)	TTL	J11	5
	RS	Output Register Shift	TTL	J10	6
	$\overline{\text{MSPSEL}}$	Output Multiplexer Control	TTL	H10	4
	TRIM	MSP Three-State Control ($\overline{\text{OEP}}$)	TTL	K11	7
	TRIL	LSP Three-State Control ($\overline{\text{OEL}}$)	TTL	A4	46
	$\overline{\text{ENX}}$	X-Register Enable (TMC217K)	TTL	D10	64
	$\overline{\text{ENY}}$	Y-Register Enable (TMC217K)	TTL	A3	44
	$\overline{\text{ENP}}$	Product Register Enable (TMC217K)	TTL	K10	8
Not Connected	NC	No Internal Connection	Open	A2, B11, K1, L10	9, 26, 43, 60

Notes: 1. Pin numbers are for $\overline{\text{MSPSEL}}$ = LOW. Pin numbers for $\overline{\text{MSPSEL}}$ = HIGH are in parenthesis.
2. N/A = Not Available.

Figure 1. Fractional Two's Complement Notation

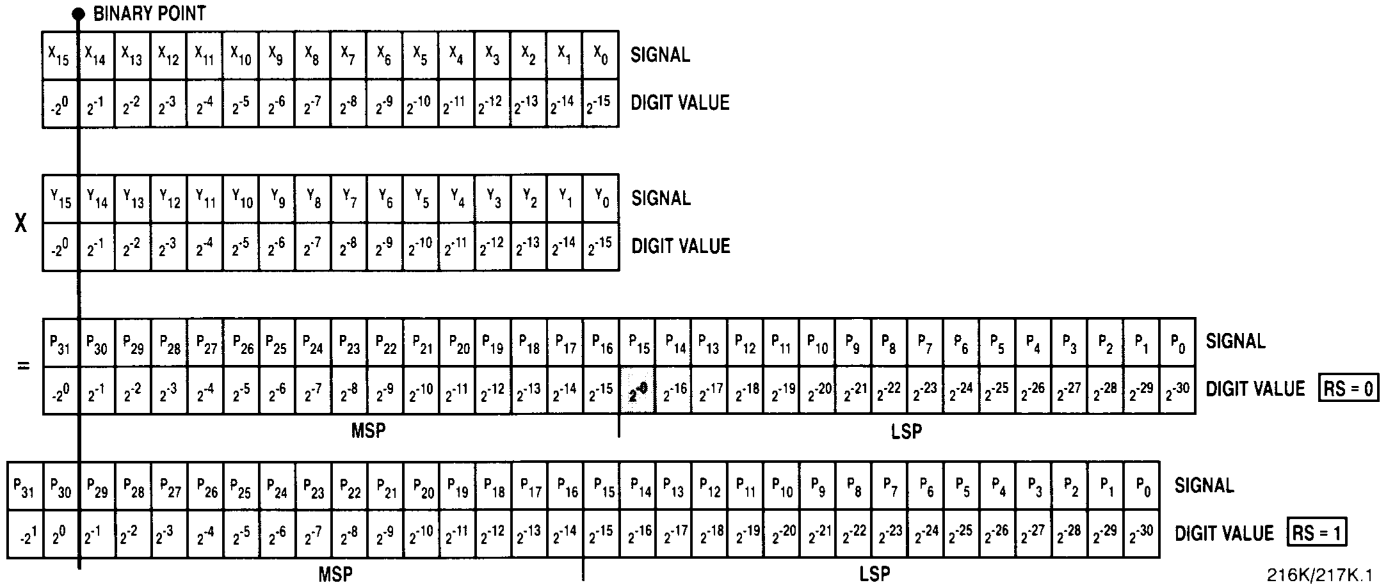


Figure 2. Fractional Unsigned Magnitude Notation

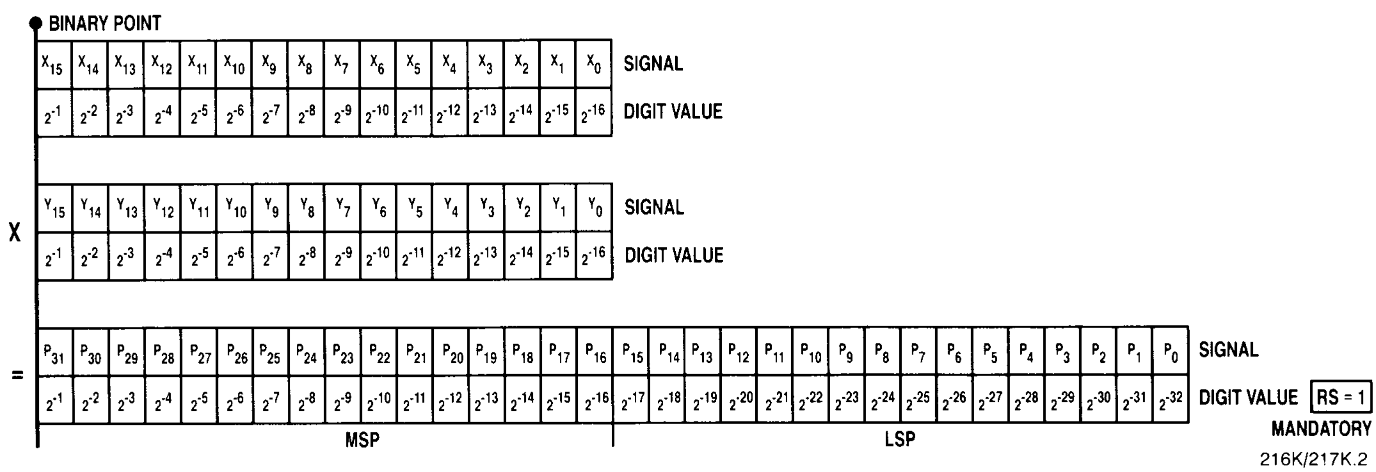


Figure 3. Fractional Mixed Mode Notation

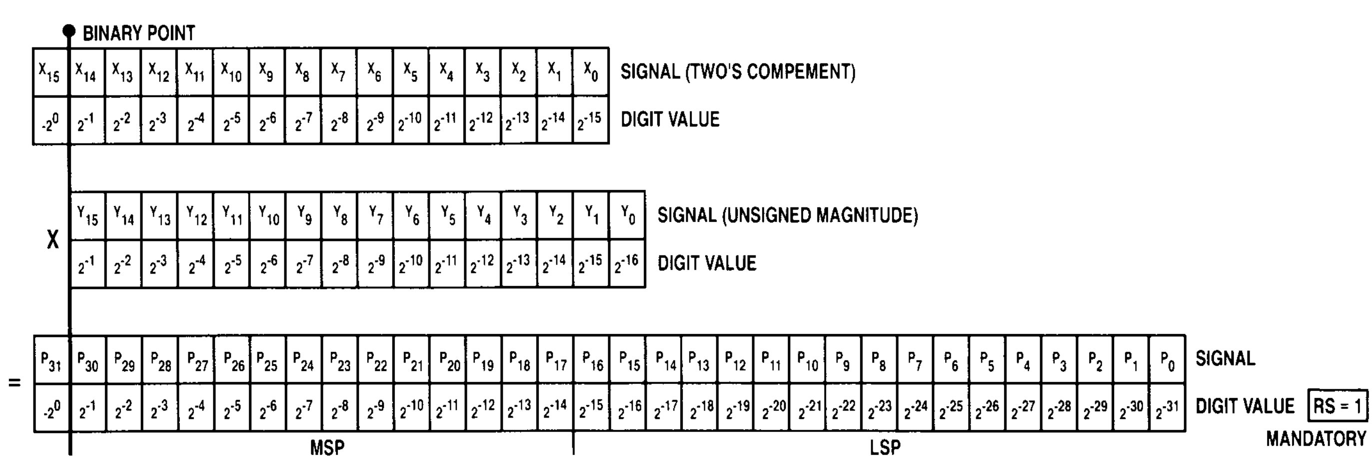


Figure 4. Integer Two's Complement Notation

BINARY POINT

X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	SIGNAL
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE

X

Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	SIGNAL
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE

=

P_{31}	P_{30}	P_{29}	P_{28}	P_{27}	P_{26}	P_{25}	P_{24}	P_{23}	P_{22}	P_{21}	P_{20}	P_{19}	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	P_{12}	P_{11}	P_{10}	P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0	SIGNAL
-2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	-2^{30}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE RS = 0

MSP LSP

=

P_{31}	P_{30}	P_{29}	P_{28}	P_{27}	P_{26}	P_{25}	P_{24}	P_{23}	P_{22}	P_{21}	P_{20}	P_{19}	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	P_{12}	P_{11}	P_{10}	P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0	SIGNAL
-2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE RS = 1

MSP LSP

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Figure 5. Integer Unsigned Magnitude Notation

BINARY POINT

X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	SIGNAL
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE

X

Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	SIGNAL
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE

=

P_{31}	P_{30}	P_{29}	P_{28}	P_{27}	P_{26}	P_{25}	P_{24}	P_{23}	P_{22}	P_{21}	P_{20}	P_{19}	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	P_{12}	P_{11}	P_{10}	P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0	SIGNAL
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE RS = 1 MANDATORY

MSP LSP

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Figure 6. Integer Mixed Mode Notation

BINARY POINT

X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	SIGNAL
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE

X

Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	SIGNAL
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE

=

P_{31}	P_{30}	P_{29}	P_{28}	P_{27}	P_{26}	P_{25}	P_{24}	P_{23}	P_{22}	P_{21}	P_{20}	P_{19}	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	P_{12}	P_{11}	P_{10}	P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0	SIGNAL
-2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE RS = 1 MANDATORY

MSP LSP

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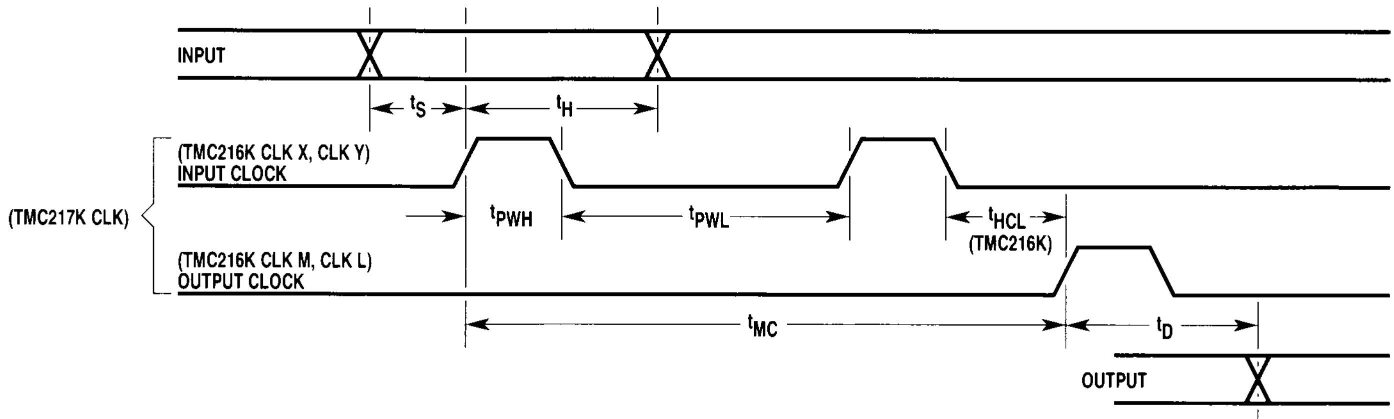
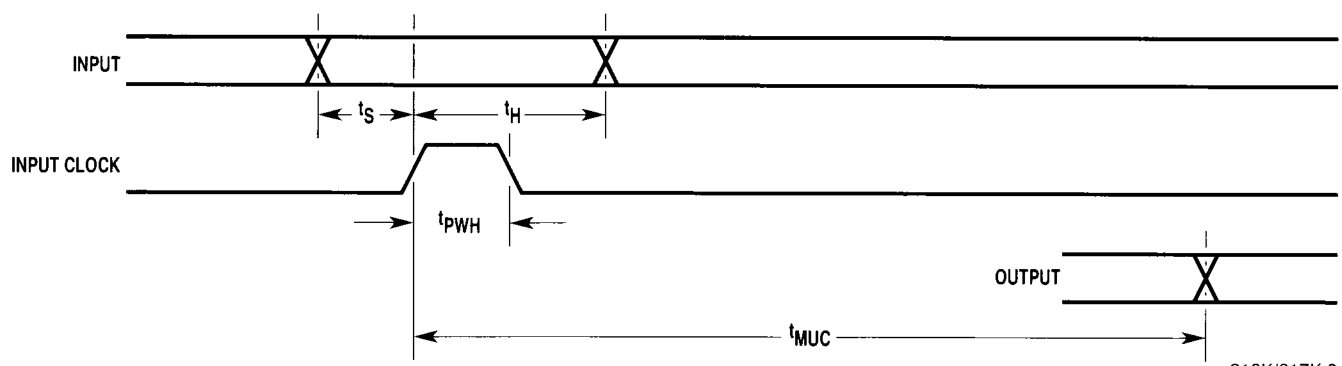
Figure 7. Timing Diagram, Clocked Mode



216K/217K.7

Figure 8. Timing Diagram, Unclocked Mode (FT=HIGH)



216K/217K.8

Figure 9. Timing Diagram, Both Modes

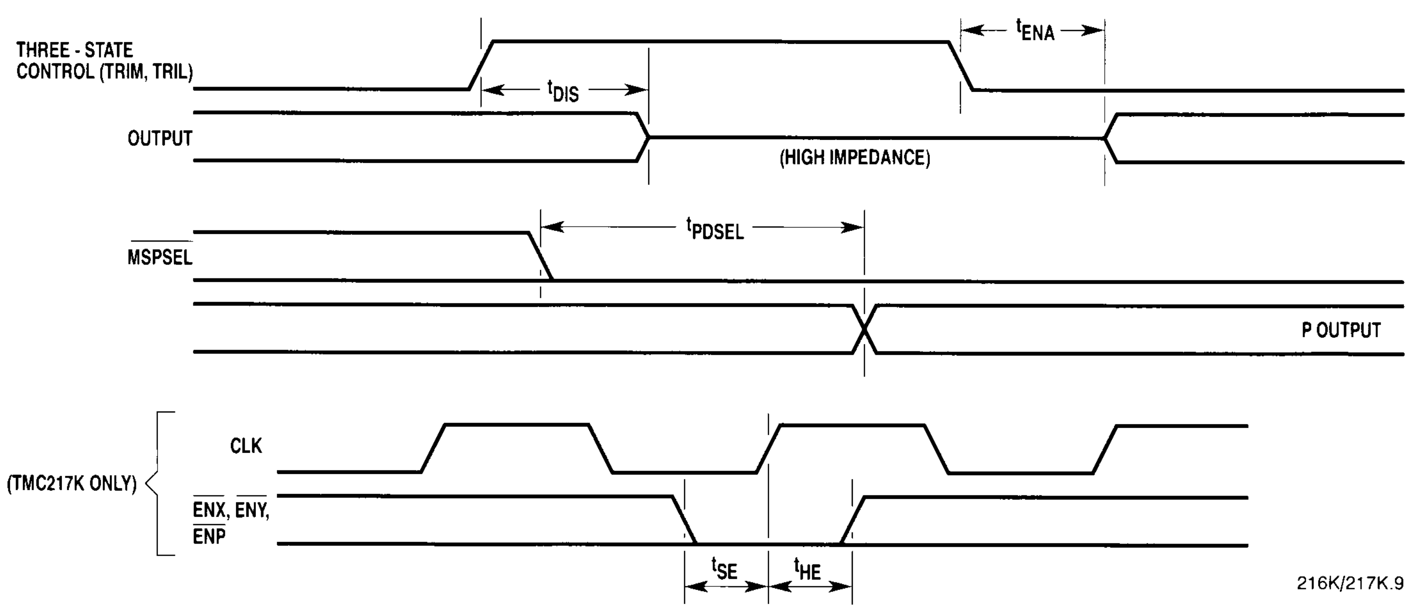


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Figure 10. Equivalent Input Circuit

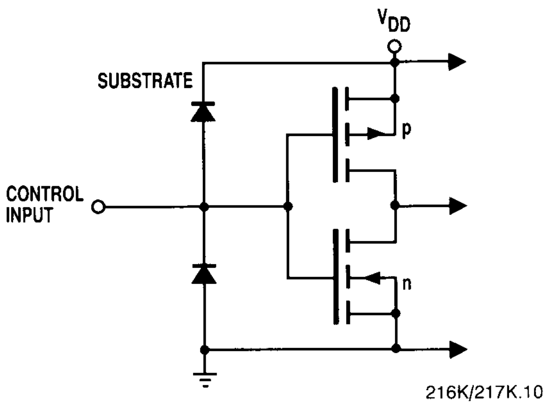


Figure 11. Equivalent Output Circuit

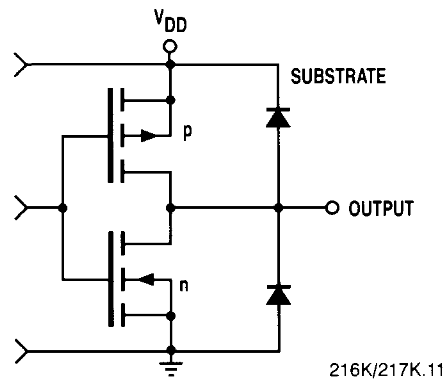


Figure 12. Test Load

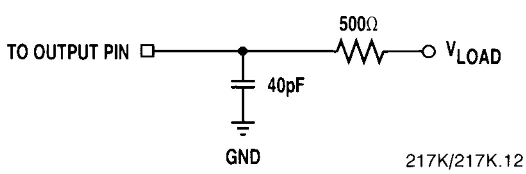


Figure 13. Transition Levels for Three-State Measurements

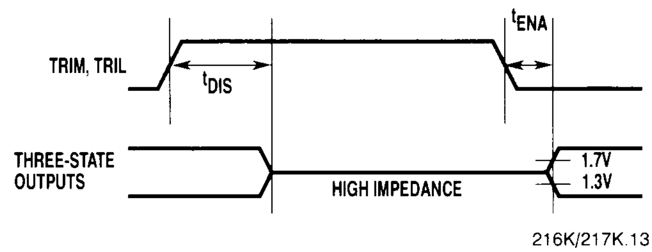
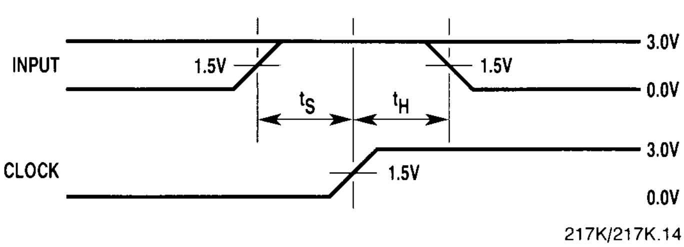


Figure 14. Transition Levels for Timing Measurements



Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltage	8.0V
Input Voltage	−0.5 to $(V_{DD}+0.5)$V
Outputs Applied Voltage	−0.5 to $(V_{DD}+0.5)$V
Temperature	
Operating, junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltages are measured with respect to GND.

Reliability Information

Θ_{ja}, G8 Package	43°C/W
Θ_{jc}, G8 Package	10°C/W
Gate Count	4500 Gates
Maximum Package Power Dissipation at +125°C, G8 Package	1.17W
ESD Classification (883 Devices)	Class 1

Operating conditions

Parameter		Temperature Range: Commercial Min	Commercial Max	Military Min	Military Max	Units
V_{DD}	Supply Voltage	4.75	5.25	4.5	5.5	V
t_{PWL}	Clock Pulse Width, LOW					
	35ns	10				ns
	45ns	15		15		ns
	60ns			20		ns
t_{PWH}	Clock Pulse Width, HIGH					
	35ns	10				ns
	45ns	15		15		ns
	60ns			20		ns
t_S	Input Setup Time; X, Y and RND Inputs					
	35ns	15				ns
	45ns	18		18		ns
	60ns			20		ns
t_H	Input Hold Time; X, Y and RND Inputs					
	Commercial (C Grade)	2				ns
	MIL-883C (V Grade)			3		ns
V_{IL}	Input Voltage, Logic LOW	2.0		2.2[1]		V
V_{IH}	Input Voltage, Logic HIGH		0.8		0.8[2]	V
T_A	Ambient Temperature	0	70	−55	+125	°C

Notes:
1. V_{DD} = Max
2. V_{DD} = Min

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Commercial Min	Commercial Max	Military Min	Military Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = V_{DD} or GND, Outputs Open		500		500	μA
I_{DDO}	Supply Current, Operating [2]	V_{DD} = Max, V_{IN} = V_{DD} or GND, f = 1.0MHz		7.0		7.0	mA
I_I	Digital Input Current	V_{DD} = Max, V_{IN} = V_{DD} or GND	−10	+10	−10	+10	μA
V_{OL}	Output Voltage, Logic LOW	I_{OL} = +4.0mA		0.4		0.4 [2]	V
V_{OH}	Output Voltage, Logic HIGH	I_{OH} = −400μA	2.6		2.6 [3]		V
I_{OZ}	Output Leakage Current	V_{DD} = Max, V_{OUT} = V_{DD} or GND	−10	10	−10	10	μA
C_I	Input Capacitance	f = 1.0MHz, T_A = 25°C		15 [4]		15 [5]	pF
C_O	Output Capacitance	f = 1.0MHz, T_A = 25°C		10 [4]		10 [5]	pF
$C_{I/O}$	I/O Capacitance	f = 1.0MHz, T_A = 25°C		10 [4]		10 [5]	pF

Notes:
1. V_{DD} = 5.0V + 5%, T_A = 0° to 70°C (TMC216K-C) or T_A = −55° to +125°C (TMC216K-V).
2. Supply current is proportional to f_{CLK}, typically 5mA per MHz.
3. V_{DD} = 4.5V
4. Typical.
5. V_{DD} = Open

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Commercial Min	Commercial Max	Military Min	Military Max	Units
t_{MC}	Multiply Time, Clocked	Loading per Figure 12					
	-35	500Ω, 40pF, V1 = 2.4V		35			ns
	-45	Input Levels = 0.0 and 3.0V		45		45	ns
	-60	t_R = t_F = 1ns.				60	ns
t_{MUC}	Multiply Time, Unclocked	Loading per Figure 12					
	-35	500Ω, 40pF, V1 = 2.4V		55			ns
	-45	Input Levels = 0.0 and 3.0V		70		70	ns
	-60	t_R = t_F = 1ns.				90	ns
t_D	Output Delay, Clock to P or Y	Loading per Figure 12					
	-35	500Ω, 40pF, V1 = 2.4V		22			ns
	-45	Input Levels = 0.0 and 3.0V		25		25	ns
	-60	t_R = t_F = 1ns.				30	ns
t_{PDSEL}	Output Delay, $\overline{MSPSEL}$ to P	Loading per Figure 12					
	-35	500Ω, 40pF, V1 = 2.4V		22			ns
	-45	Input Levels = 0.0 and 3.0V		25		25	ns
	-60	t_R = t_F = 1ns.				30	ns

Note: 1. V_{DD} = 5.0V + 5%, T_A = 0° to 70°C (TMC216K-C) or T_A = −55° to +125°C (TMC216K-V).

Switching characteristics within specified operating conditions [1] (cont.)

Parameter		Test Conditions	Commercial Min	Commercial Max	Military Min	Military Max	Units
t_{ENA}	Three-State Output Enable Delay	Loading per Figure 12					
	-35	500Ω, 40pF, V1 = 1.5V		22			ns
	-45	Transition measured at ±200mV		25		25	ns
	-60	from steady-state voltage.				30	ns
t_{DIS}	Three-State Output Disable Delay	Loading per Figure 12					
	-35	500Ω, 40pF, V1 = 1.5V		22			ns
	-45	Transition measured at ±200mV		25		25	ns
	-60	from steady-state voltage.				30	ns
t_{HCL} [2]	Clock LOW Hold Time, CLK X/CLK Y	Relative to CLK M/CLK L [3] Loading per Figure 12 500Ω, 40pF, V1 = 2.4V Input Levels = 0.0 and 3.0V $t_R = t_F = 1$ns.	0		0		ns
t_{SE} [4]	Clock Enable Setup Time	Loading per Figure 12 500Ω, 40pF, V1 = 2.4V Input Levels = 0.0 and 3.0V $t_R = t_F = 1$ns.	15		15		ns
t_{HE} [4]	Clock Enable Hold Time	Loading per Figure 12 500Ω, 40pF, V1 = 2.4V Input Levels = 0.0 and 3.0V $t_R = t_F = 1$ns.	2		2		ns
t_R	Output Rise Time	From 0.8V to 2.0V		8		10	ns
t_F	Output Fall Time	From 2.0V to 0.8V		8		10	ns

Notes:
1. $V_{DD} = 5.0V \pm 5\%$, $T_A = 0°$ to 70°C (TMC216K-C) or $T_A = -55°$ to +125°C (TMC216K-V).
2. TMC216K only.
3. To ensure the correct product is entered in the output registers, new data may not be entered into the input registers before the output registers have been clocked.
4. TMC217K only.

Application Notes

Mixed Mode Multiplication

There are several applications in which mixed mode multiplication may be advantageous. For example, inputs to a digital signal processor are often generated as unsigned magnitude numbers (e.g., data from an analog-to-digital converter). These numbers are effectively all positive values. In contrast, filter coefficients must often be negative. As a result, either the unsigned magnitude data must be converted to two's complement notation (which requires an additional bit), or the multiplier must be capable of mixed mode operation. The TMC216K and TMC217K provide this capability by independently specifying the mode of the multiplicand (X) and the multiplier (Y) on the TCX and TCY pins. No additional circuitry is required and the resulting product is in two's complement notation.

Multiplication by a Constant

Multiplication by a constant only requires that the constant be loaded into the desired input register, and that the selected register not be loaded again until a new constant is desired. The multiply cycle then consists simply of loading new data and strobing the output register.

Selection of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the TMC216K and TMC217K do not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64.$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in *Figures 1 through 6*.

Register Shift (RS) Control

In two's complement notation, the acceptable range of values for a given word size is not the same for positive and negative numbers. The largest negative number is one LSB larger than the largest positive number. This is true for either fractional or integer notation. A problem can arise when the largest representable negative number is multiplied by itself. This should give a positive number of the same magnitude. However, the largest representable positive number is one LSB less than this value. As a result, this product cannot be correctly represented without using one additional output bit. The TMC216K and TMC217K have a Register Shift (RS) control that permits shifting of the result to provide a correct answer for every two's complement multiplication. When RS is active, the value of all bits in the MSP is doubled (i.e., shifted left one position), which provides the capability to represent the largest possible product. The MSB of the Least Significant Product is changed from a duplicate of the sign bit to the necessary bit to fill in the output word. The effects of this control are illustrated in *Figures 1 and 4*. Note that for unsigned magnitude operation, the RS control must be HIGH.

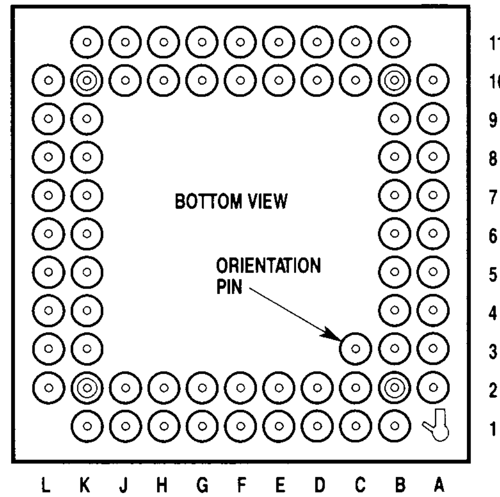
Output Register Transparent Mode

If the FT input is HIGH, the output register is made transparent: i.e., the product will appear at the output drivers as it is generated internally. The clock for the product registers (CLK L, CLK M, TMC216K) is not required in this mode of operation. The clocks for the product registers should be tied HIGH or LOW. The transparent mode is rarely used as it is much slower than the registered mode. It is essentially a special-purpose mode of operation.

Pin Assignments

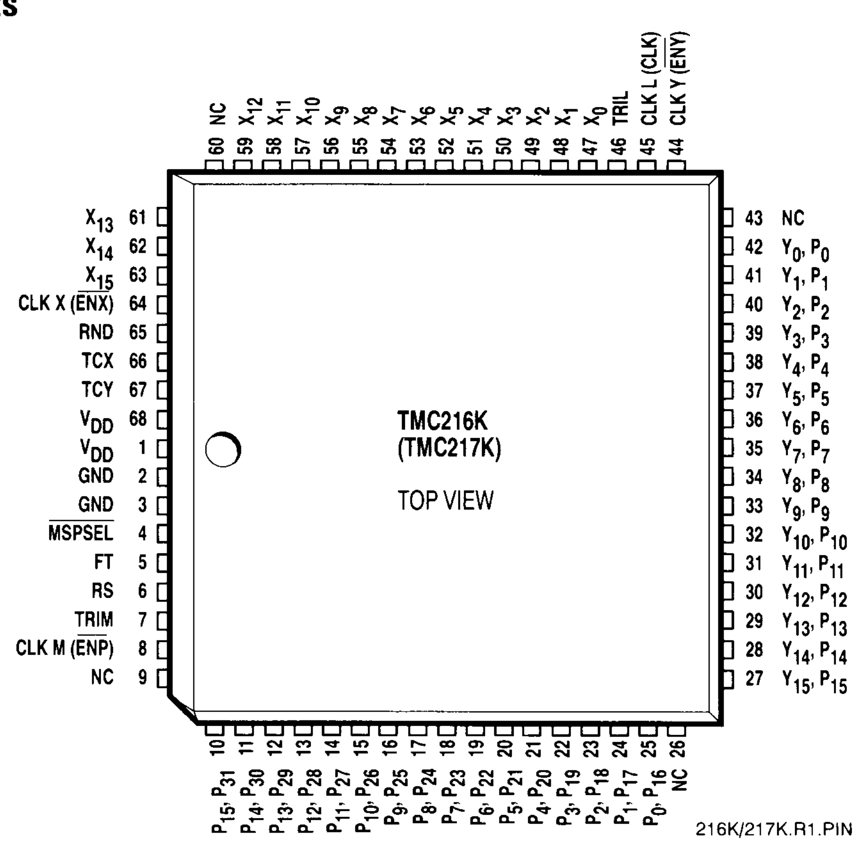
68 Pin Ceramic (G8) or Plastic (H8) Pin Grid Arrays

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A2	NC	B9	X_{10}	F10	V_{DD}	K4	P_{20}, P_4
A3	CLK Y ($\overline{ENY}$)	B10	X_{12}	F11	TCY	K5	P_{22}, P_6
A4	TRIL	B11	NC	G1	Y_{11}, P_{11}	K6	P_{24}, P_8
A5	X_1	C1	Y_3, P_3	G2	Y_{10}, P_{10}	K7	P_{26}, P_{10}
A6	X_3	C2	Y_2, P_2	G10	GND	K8	P_{28}, P_{12}
A7	X_5	C10	X_{14}	G11	V_{DD}	K9	P_{30}, P_{14}
A8	X_7	C11	X_{13}	H1	Y_{13}, P_{13}	K10	CLK M ($\overline{ENP}$)
A9	X_9	D1	Y_5, P_5	H2	Y_{12}, P_{12}	K11	TRIM
A10	X_{11}	D2	Y_4, P_4	H10	$\overline{MSPSEL}$	L2	P_{17}, P_1
B1	Y_1, P_1	D10	CLK X ($\overline{ENX}$)	H11	GND	L3	P_{19}, P_3
B2	Y_0, P_0	D11	X_{15}	J1	Y_{15}, P_{15}	L4	P_{21}, P_5
B3	CLK L (CLK)	E1	Y_7, P_7	J2	Y_{14}, P_{14}	L5	P_{23}, P_7
B4	X_0	E2	Y_6, P_6	J10	RS	L6	P_{25}, P_9
B5	X_2	E10	TCX	J11	FT	L7	P_{27}, P_{11}
B6	X_4	E11	RND	K1	NC	L8	P_{29}, P_{13}
B7	X_6	F1	Y_9, P_9	K2	P_{16}, P_0	L9	P_{15}, P_{31}
B8	X_8	F2	Y_8, P_8	K3	P_{18}, P_2	L10	NC



G8.68PIN

Pin Assignments



216K/217K.R1.PIN

68 Lead Plastic J-Leaded Chip Carrier – R1 Package

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC216KG8V45	EXT:T_A = −55°C to 125°C	MIL-STD-883C	68 Pin Ceramic Pin Grid Array	216KG8V45
TMC216KG8V60	EXT:T_A = −55°C to 125°C	MIL-STD-883C	68 Pin Ceramic Pin Grid Array	216KG8V60
TMC216KH8C35	STD:T_A = 0°C to 70°C	Commercial	68 Pin Plastic Pin Grid Array	216KH8C35
TMC216KH8C45	STD:T_A = 0°C to 70°C	Commercial	68 Pin Plastic Pin Grid Array	216KH8C45
TMC216KR1C35	STD:T_A = 0°C to 70°C	Commercial	68 Lead Plastic J-Leaded Chip Carrier	216KR1C35
TMC216KR1C45	STD:T_A = 0°C to 70°C	Commercial	68 Lead Plastic J-Leaded Chip Carrier	216KR1C45
TMC217KG8V45	EXT:T_A = −55°C to 125°C	MIL-STD-883C	68 Pin Ceramic Pin Grid Array	217KG8V45
TMC217KG8V60	EXT:T_A = −55°C to 125°C	MIL-STD-883C	68 Pin Ceramic Pin Grid Array	217KG8V60
TMC217KH8C35	STD:T_A = 0°C to 70°C	Commercial	68 Pin Plastic Pin Grid Array	217KH8C35
TMC217KH8C45	STD:T_A = 0°C to 70°C	Commercial	68 Pin Plastic Pin Grid Array	217KH8C45
TMC217KR1C35	STD:T_A = 0°C to 70°C	Commercial	68 Lead Plastic J-Leaded Chip Carrier	217KR1C35
TMC217KR1C45	STD:T_A = 0°C to 70°C	Commercial	68 Lead Plastic J-Leaded Chip Carrier	217KR1C45

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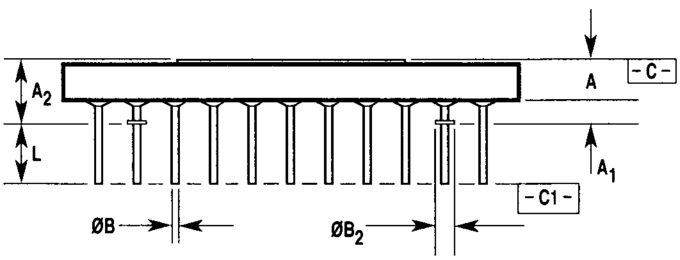
G8 Package
68 Pin Grid Array

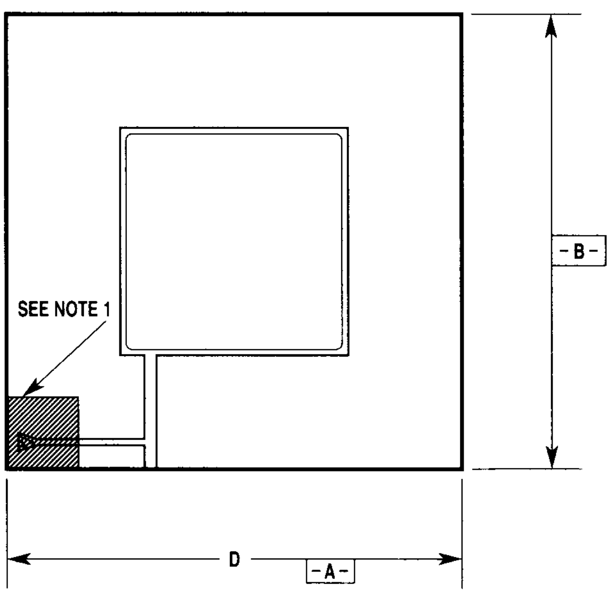
Notes: 1. Pin one identifier shall be within shaded area shown.
2. Dimension M: defines matrix size.
3. Dimension N: defines pin count.
4. Controlling dimension: inch.
5. Optional (TRW option) index pin.

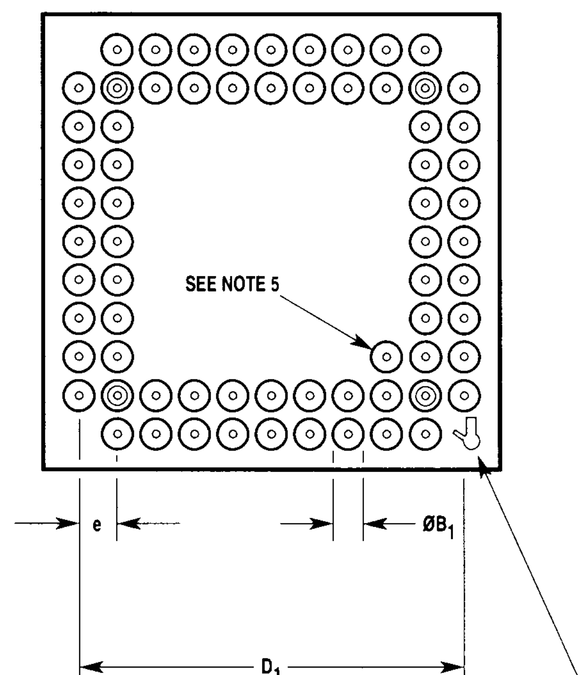


Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.080 (2.03)	.125 (3.18)	
A_1	.040 (1.02)	.060 (1.52)	
A_2	.115 (2.92)	.190 (4.83)	
ϕB	.017 (0.43)	.020 (0.51)	
ϕB_1		.080 (2.03)	
ϕB_2			.050 (1.27) Nominal
D	1.140 (28.96)	1.180 (29.97)	
D_1			1.00 (25.4) Basic
e			.100 (2.54) Basic
L	.120 (3.05)	.150 (3.81)	
M			11, Note 2
N			68, Note 3

Ref. 90X00181





KEY (BOTTOM SIDE) FOR PIN ONE IDENTIFIER

G8.68.PGA.LU

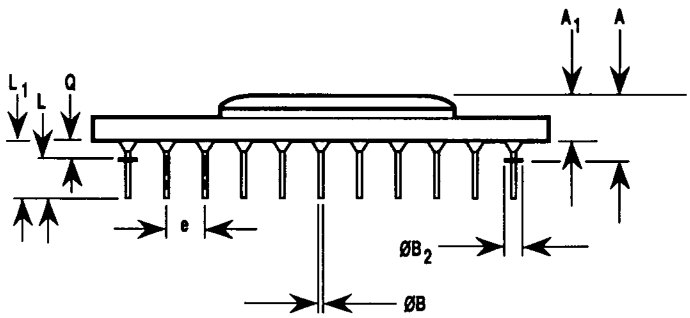
H8 Package
69 Printed Circuit Board
Pin Grid Array, Cavity Up

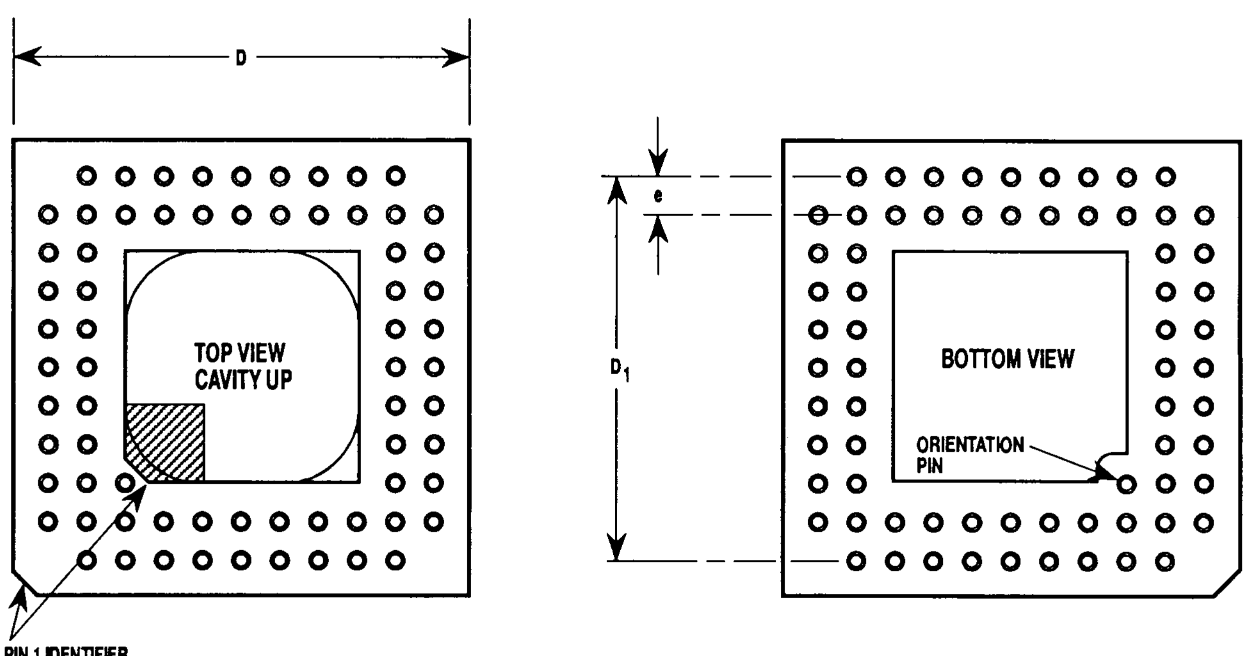
Notes:
1. Pin one identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension M: defines matrix size.
4. Dimension N: defines the maximum possible number of pins. Orientation pin is at supplier's option.
5. Controlling dimension: inch.

Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Notes
A	.125 (3.17)	.215 (5.46)	
A_1	.080 (2.03)	.160 (4.06)	
ϕB	.016 (0.41)	.020 (0.51)	Note 2
ϕB_2			.050 (1.27) Nominal, Note 2
D	1.140 (28.96)	1.180 (29.97)	Square
D_1			1.000 (25.40) Basic
e			.100 (2.54) Basic
L	.110 (2.79)	.145 (3.68)	
L_1	.170 (4.32)	.190 (4.83)	
M			11, Note 3
N			68, Note 4
Q	.040 (1.02)	.060 (1.52)	

Ref. 90X00181

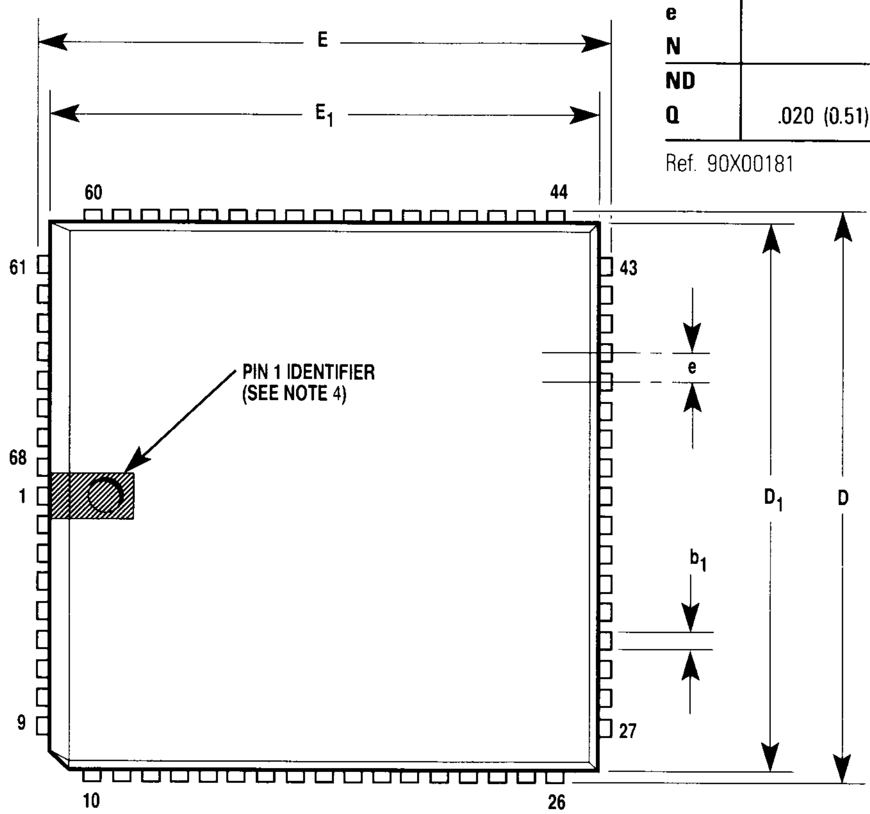


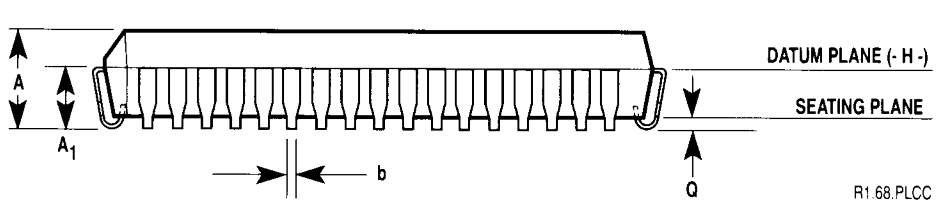


H8.69.PPGA.LU

R1 Package
68 Lead Plastic J-Leaded Chip Carrier

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane (– H –) located at top of mold parting line and coincident with top of lead, where lead exits plastic body.
3. Dimension D_1 and E_1 do not include mold protrusion. Allowable protrusion is .010 inch (0.25mm).
4. Details of pin 1 identifier are optional but must be located within the zone indicated.
5. Dimension N: number of terminals.
6. Dimension ND: number of terminals per package edge.
7. Controlling dimension: inch.





Dimensions

Sym	Inches (Millimeters) Min	Max	Notes
A	.165 (4.20)	.200 (5.08)	
A_1	.090 (2.29)	.130 (3.30)	
b	.013 (0.33)	.021 (0.53)	
b_1	.026 (0.66)	.032 (0.81)	
D	.985 (25.02)	.995 (25.27)	
D_1	.950 (24.13)	.958 (24.33)	Note 3
E	.985 (25.02)	.995 (25.27)	
E_1	.950 (24.13)	.958 (24.33)	Note 3
e			.050 (1.27) Basic
N			68, Note 5
ND			17, Note 6
Q	.020 (0.51)		

Ref. 90X00181